Oversampling Converters

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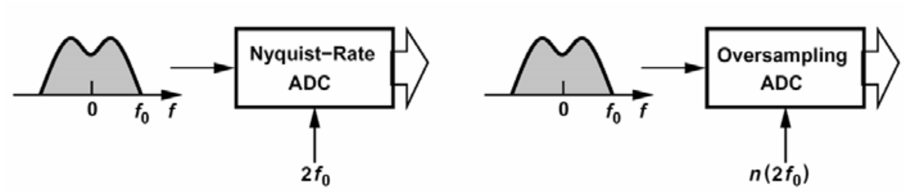
Outline

- **Basic Concepts**
- **First- and Second-Order Loops**
- **Effect of Circuit Nonidealities**
- **Cascaded Modulators**

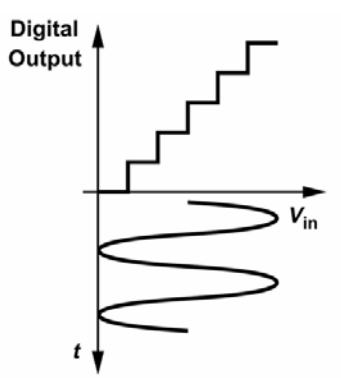
Basic Idea

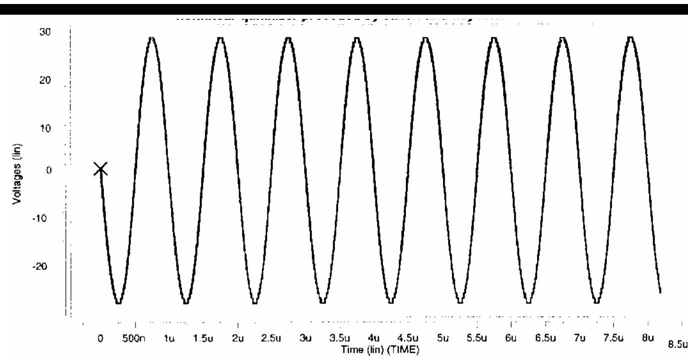


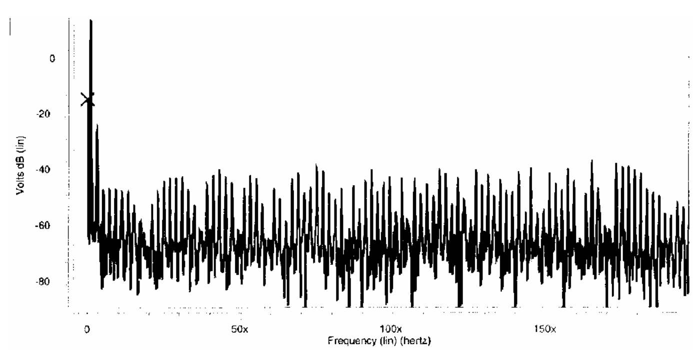
Why oversample?

- **Simplifies design of antialiasing filter**
- **Trades resolution in time for resolution in amplitude**
- **Analog matching and gain requirements substantially relaxed**
- **Spreads op amp and kT/C noise**

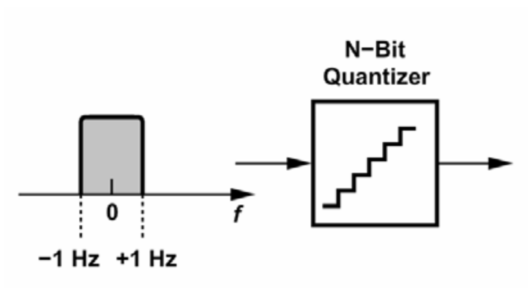
Quantization Noise

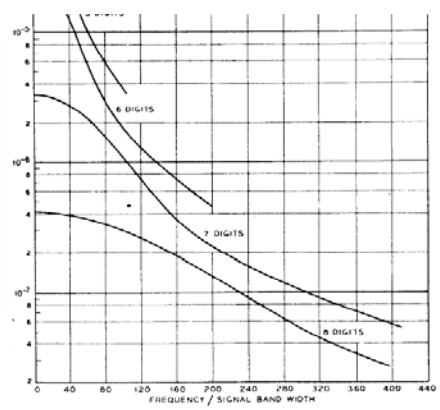






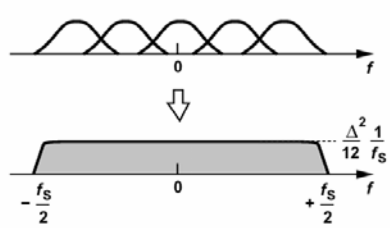
Spectrum of Quantization Noise





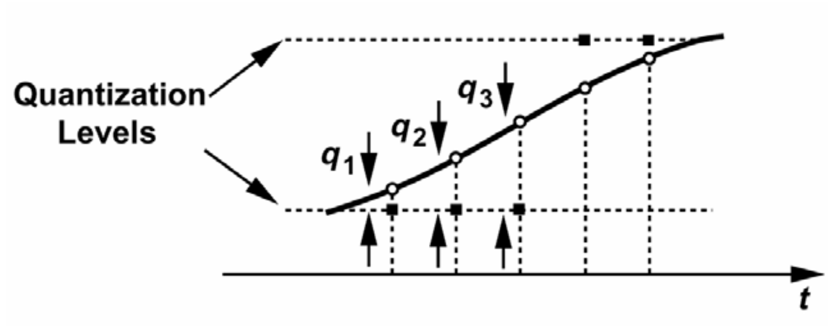
[Bennet, BSTJ, July ’48]

After Sampling:



What happens if the sampling rate is doubled?

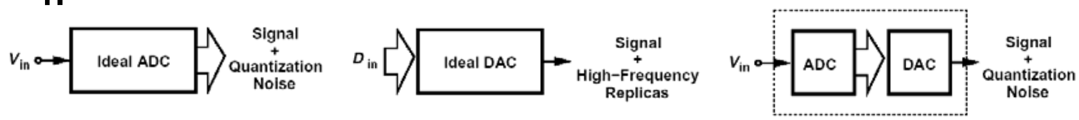
Exploit Correlation Between Samples



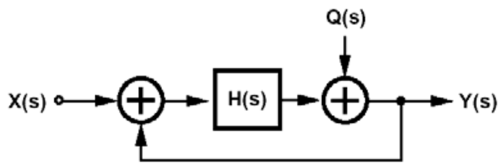
- If sampling rate is higher than Nyquist, the signal changes slowly between samples and quantization noise components are correlated.

Observations

1.



2.

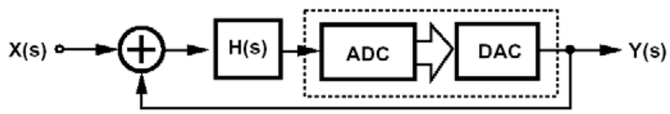


$$H(s) = \frac{1}{s}$$

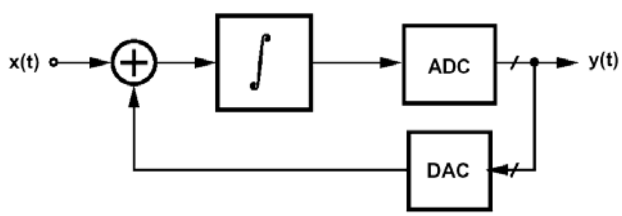
$$\frac{Y}{Q} = \frac{s}{s+1}$$

Noise Transfer Function (NTF)

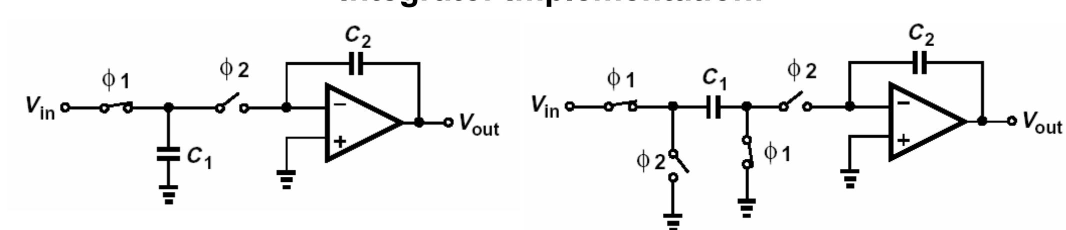
3.



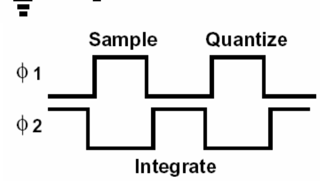
First-Order Modulator



Integrator Implementation:



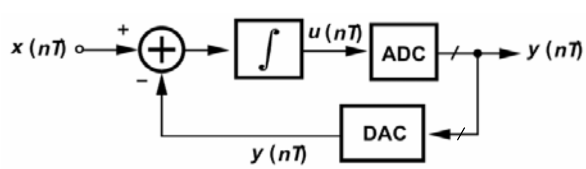
- **Integrator output is delayed by one clock cycle with respect to input.**



Assumptions for Simple Analysis

- Quantization noise is additive and white with a uniform distribution.
- Quantizer gain is equal to unity and constant.

Simple Analysis



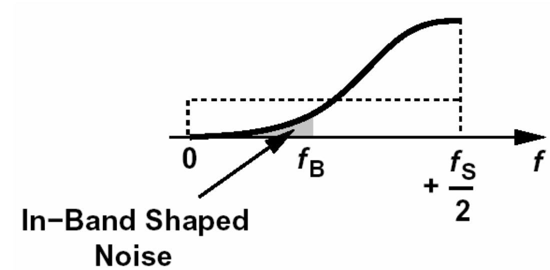
- Find difference equation.
- Take z transform and find NTF.
- Find output noise spectrum.
- Integrate across input signal bandwidth.

$$Y = z^{-1} X + (1 - z^{-1}) Q$$

Noise Shaping

$$S_Y(f) = S_Q(f)\left|\frac{Y}{Q}\right|^2$$

$$S_Y(f) = (2\sin\pi fT)^2\,\frac{\Delta^2}{12}\,\frac{1}{f_S}$$



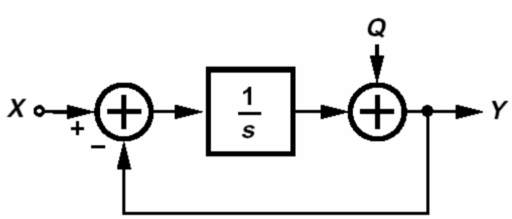
$$P_{tot} = \frac{\pi^2}{3}\left(\frac{2f_B}{f_S}\right)^3\frac{\Delta^2}{12}$$

Oversampling Ratio, *M* (OSR)

For an L-th order modulator:

$$P_{tot} = \frac{\pi^{2L}}{2L+1}\,\frac{1}{M^{2L+1}}\,\frac{\Delta^2}{12}$$

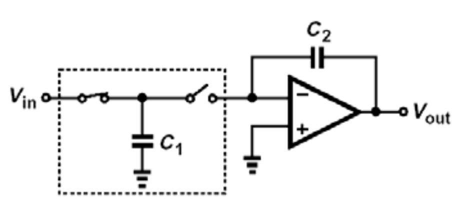
Continuous-Time Approximation



$$\frac{Y}{Q} = \frac{s}{s+1}$$

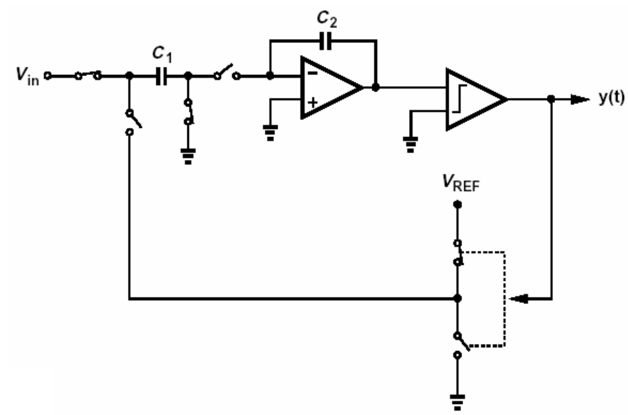
$$S_Y(f) = S_Q(f)\left|\frac{Y}{Q}\right|^2 = \frac{\Delta^2}{12}\,\frac{1}{f_S}\,\frac{\omega^2}{1+\omega^2}$$

$$P_{tot} = \int_{-f_B}^{+f_B}\frac{\Delta^2}{12}\,\frac{1}{f_S}\,\frac{\omega^2}{1+\omega^2}\,d\omega \approx \frac{\pi^2}{3}\left(\frac{2f_B}{f_S}\right)^3\frac{\Delta^2}{12}f_S^2$$



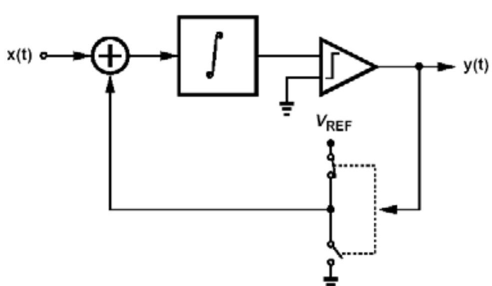
$$R_{eq} = \frac{1}{f_S C_1}$$

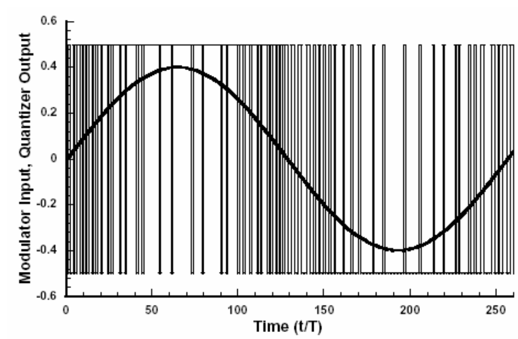
First-Order One-Bit Modulator



- DAC is unconditionally linear.
- Simple, but gradual noise shaping (and tone problems)

Operation of the Loop



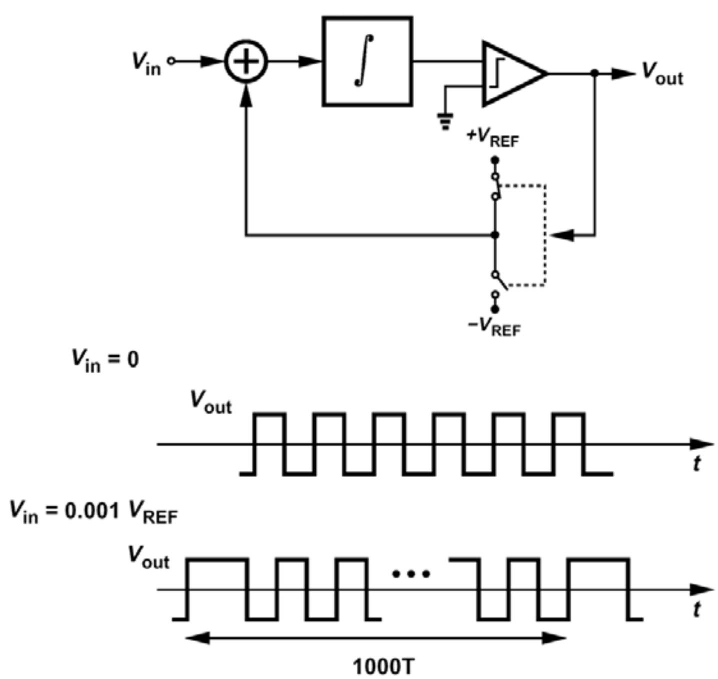


- Each time integrator output crosses zero, quantizer feeds a pulse to integrator to oppose it.
- Since average integrator output must be zero, the loop attempts to minimize the difference between average input and average quantizer output.

Performance Metrics

- Differential and integral nonlinearity not meaningful
- SNR, SNDR, and dynamic range are used.
- Absolute noise floor and spur levels become important in many applications. (A modulator with 90-dB of DR does not necessarily fit into an RF receiver chain.)

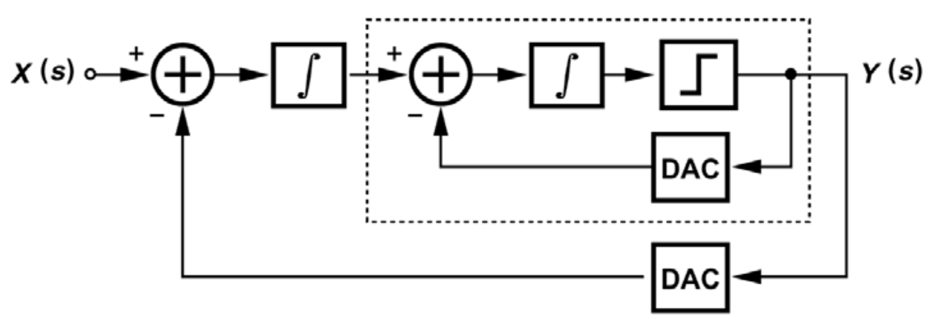
Problem of Tones



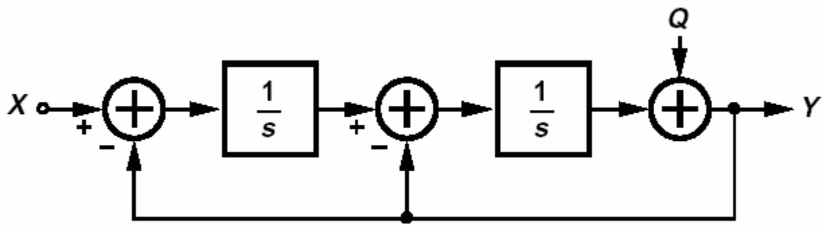
Suppression of Tones

- Higher Oversampling Ratio
- Higher Order
- Dither
- Cascaded Modulator

Second-Order Modulator



Continuous-Time Approximation

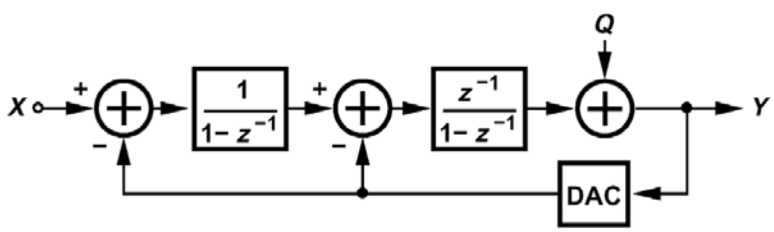


$$\frac{Y}{Q} = \frac{s^2}{s^2 + s + 1}$$

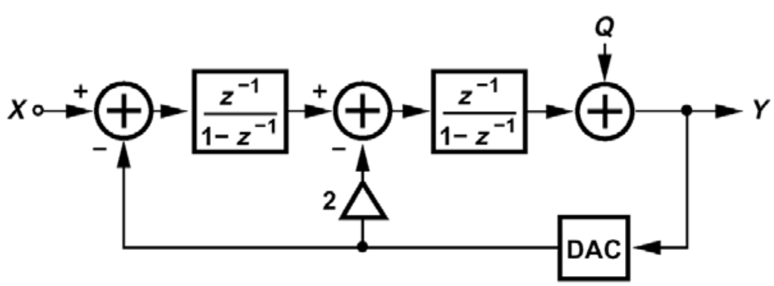
$$S_Y(f) = S_Q(f)\left|\frac{Y}{Q}\right|^2$$

$$= \frac{\Delta^2}{12}\frac{1}{f_S}\left|\frac{-\omega^2}{1-\omega^2+j\omega}\right|^2$$

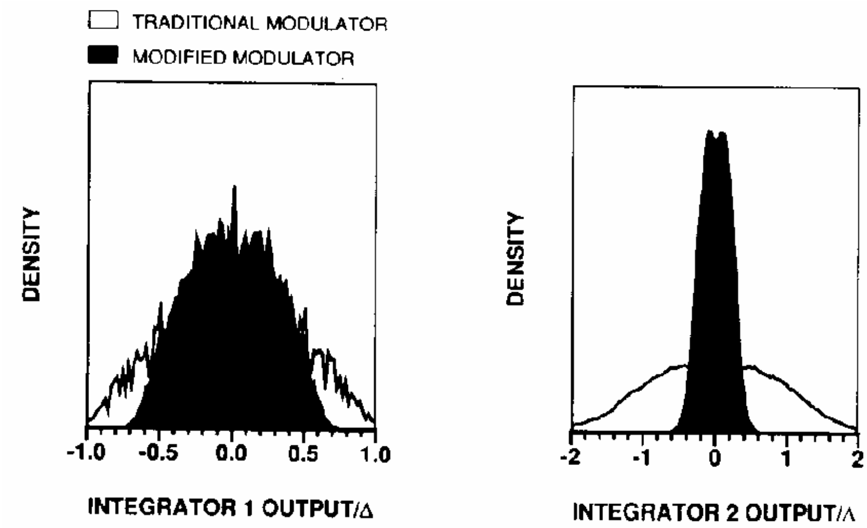
Discrete-Time Model



$$Y = z^{-1}X + (1 - z^{-1})^2 Q$$



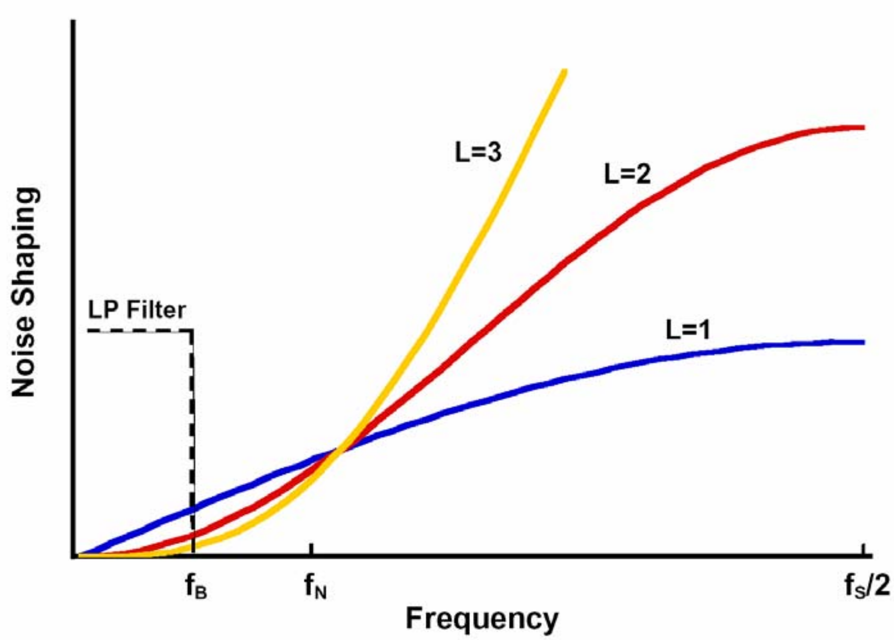
Integrator Output Swings



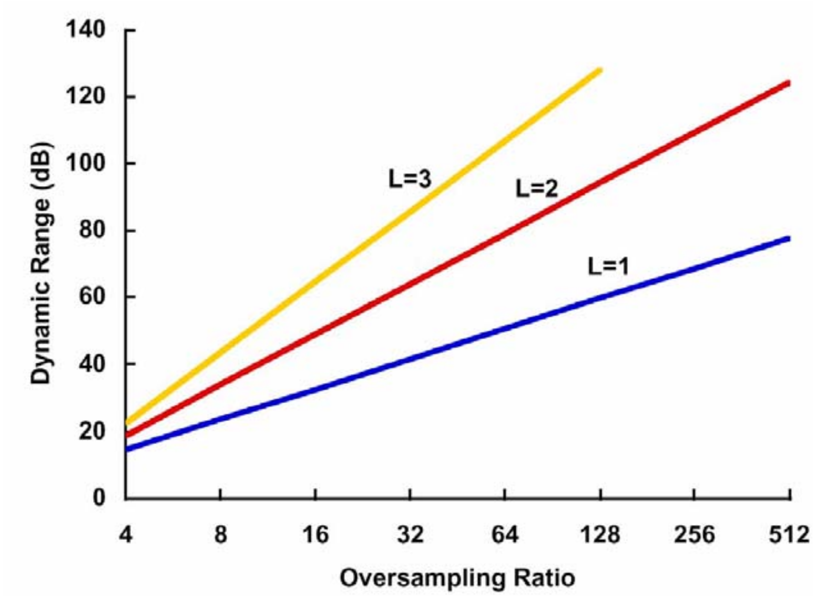
[Boser & Wooley, JSSC, Dec. 88]

Noise-Shaping Properties

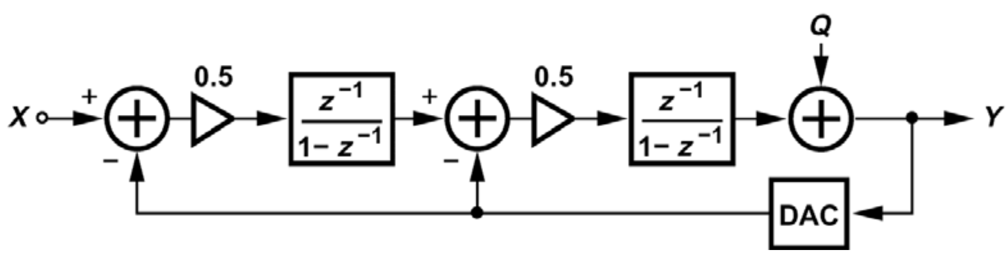
$$Y(z) = z^{-1}X(z) + (1 - z^{-1})^{L}E_Q(z)$$

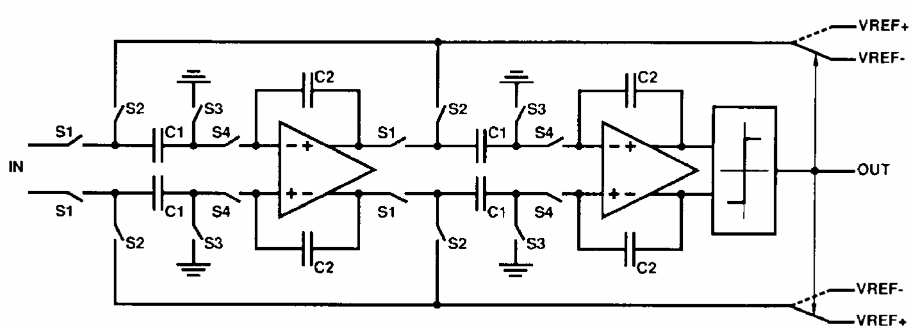


Dynamic Range



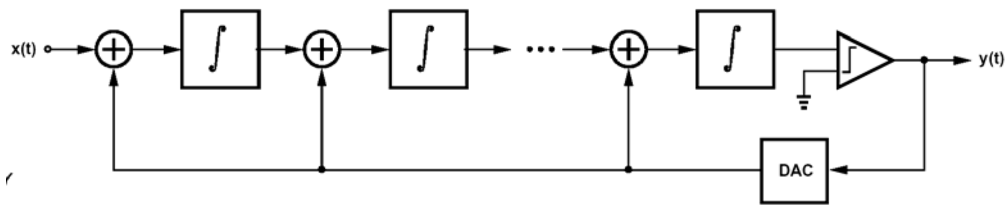
Reduction of Integrator Swings by Scaling





[Boser & Wooley, JSSC, Dec. 88]

Higher-Order Loops



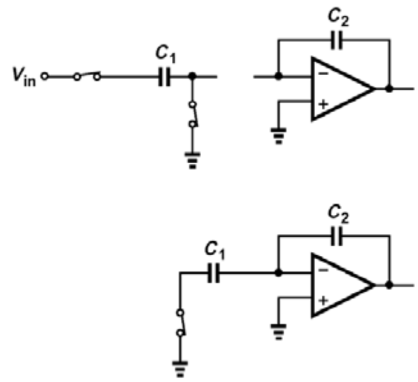
- Difficult to stabilize
- Feedforward with very carefully chosen scaling factors (gains) can stabilize third-order systems.
- But the internal swings tend to be large.

Circuit Nonidealities in One-Bit Modulators

- First Integrator:
  - Noise
  - Leakage
  - Slew Rate
  - Small-Signal Settling
  - Nonlinearity
- Signal Range at Internal Nodes
- Sampling Jitter

Noise Components

- kT/C Noise in Sampling and Integration Modes:



- Op Amp Noise
- Both kT/C noise and op amp noise are reduced by OSR.
- Noise of DAC Reference Voltages

Integrator Leakage

- Only a fraction, P_0, of the previous output of integrator is added to the new input sample:

$$H(z) = \frac{g_0 z^{-1}}{1 - P_0 z^{-1}}$$

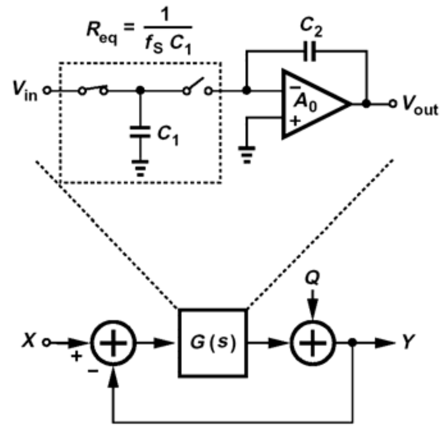
- The dc gain is now $H_0=g_0/(1-P_0)$, degrading the suppression of quantization noise.

Continuous-Time Approximation

$$\frac{Y}{Q} = \frac{\frac{1}{1+A_0} + s R_{eq} C_2}{1 + s R_{eq} C_2}$$

$$S_Y(f) = S_Q(f) \left| \frac{Y}{Q} \right|^2$$

$$S_Y(f) = \frac{\Delta^2}{12} \frac{\left(\frac{1}{1+A_0}\right)^2 + \left(2\pi \frac{f}{f_S}\right)^2}{1 + \left(2\pi \frac{f}{f_S}\right)^2}$$



For Ideal Op Amp:

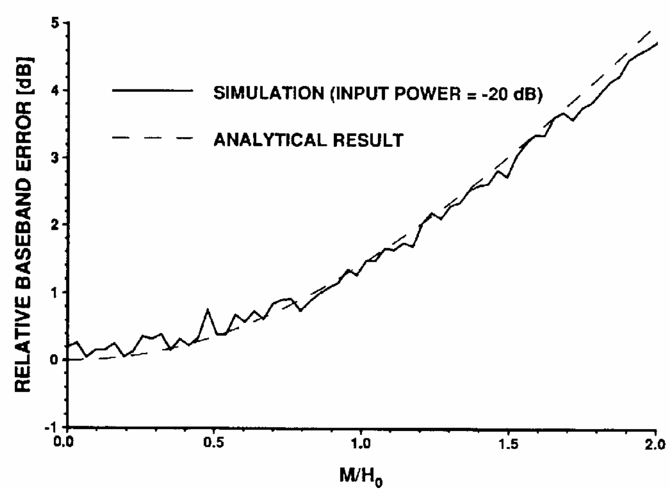
$$P_{tot} \approx \frac{\pi^2}{3} \left(\frac{2 f_B}{f_S}\right)^3 \frac{\Delta^2}{12}$$

If leakage must not raise noise by more than 10%, then:

$$A_0 > \frac{\sqrt{30}}{\pi} \frac{f_S}{2 f_B} - 1$$

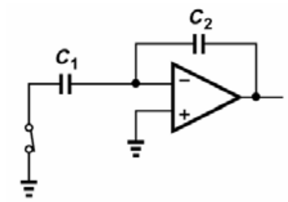
More Accurate Analysis

$$\frac{\Delta S_B}{S_B} = \frac{5}{\pi^4}\left(\frac{M}{H_0}\right)^4 + \frac{10}{3\pi^2}\left(\frac{M}{H_0}\right)^2.$$



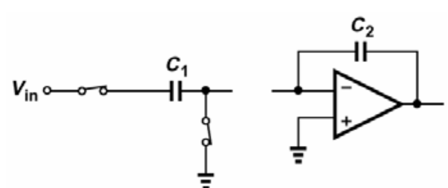
[Boser & Wooley, JSSC, Dec. 88]

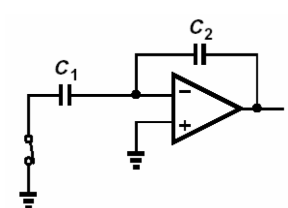
Integrator Speed



- Slow linear settling is quite benign.
- Slewing leads to nonlinear components and must diminish before the output is sampled.
- Speed trades with kT/C noise, op amp gain, and output swings.

Integrator Nonlinearity

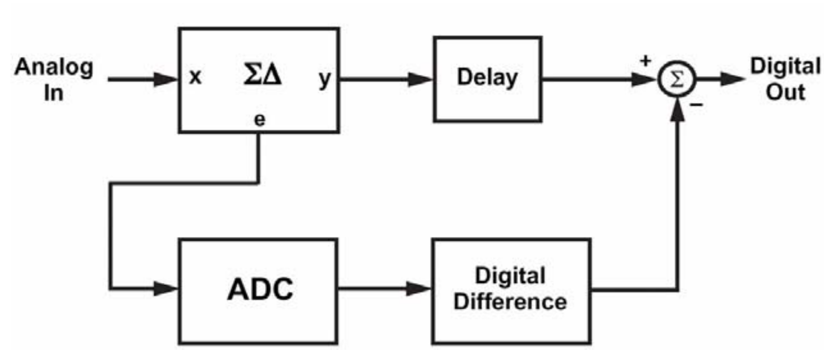




- Switch nonlinearity distorts the signal during sampling → bootstrapping often used.
- Op amp nonlinearity distorts the integrated output.
- Op amp gain must still be high enough to lower the closed-loop nonlinearity.
- Open-loop gain of op amp typically dominated by the linearity requirement rather than by integrator leakage requirement.

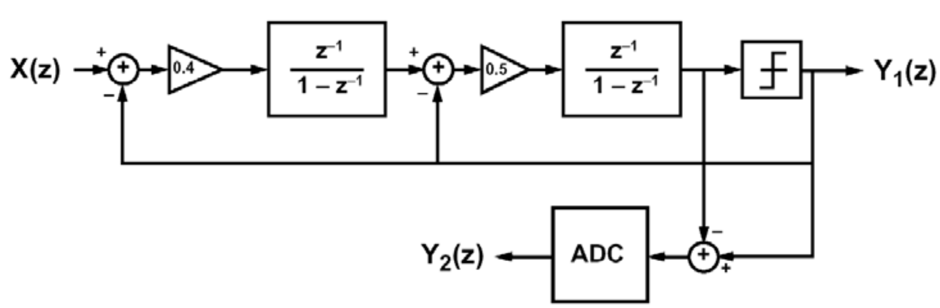
→ Most "16-bit" oversampling converters are only ~14-bit linear!

Cascaded Modulators

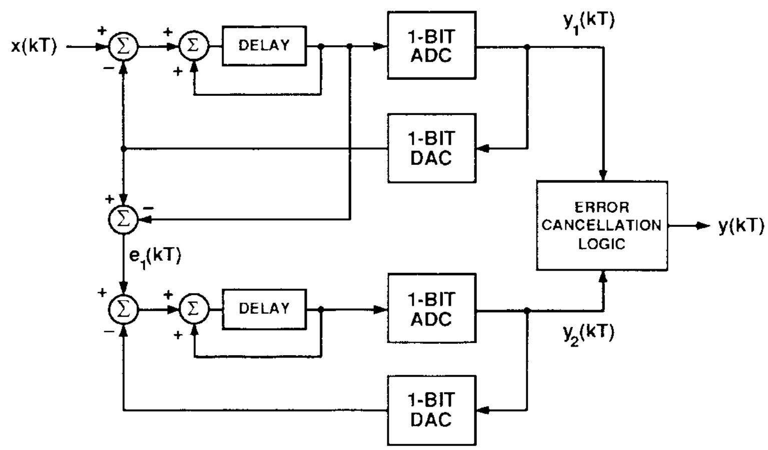


- Stability can be maintained.
- But quantization noise and tones of first modulator leak to the final output because of coefficient mismatches.

Example



Cascaded Modulators: 1-1 Architecture



$$y_1(kT) = x(kT - T) + e_1(kT) - e_1(kT - T)$$

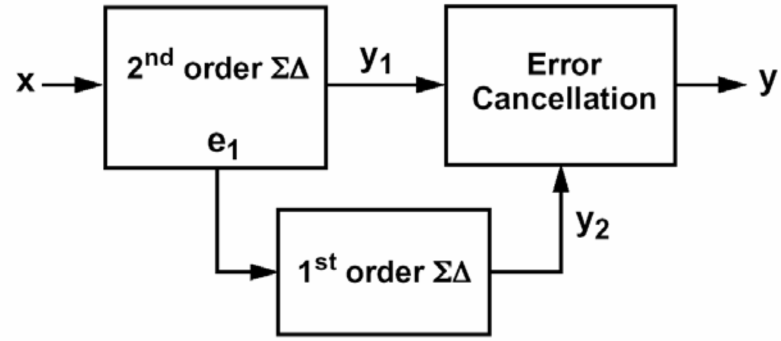
$$y_2(kT) = e_1(kT - T) + e_2(kT) - e_2(kT - T)$$

$$y(kT) = y_1(kT - T) - y_2(kT) + y_2(kT - T)$$

Sources of Mismatch

- **Gain Error in Integrator:**
  - **- Finite Op Amp Gain**
  - **- Capacitor Mismatch**
  - **- Incomplete Settling**
- **Requires minimizing quantization noise of first modulator.**
  - **→ Avoid first-order loop for the first modulator.**
  - **→ Use multibit quantizer in first modulator.**

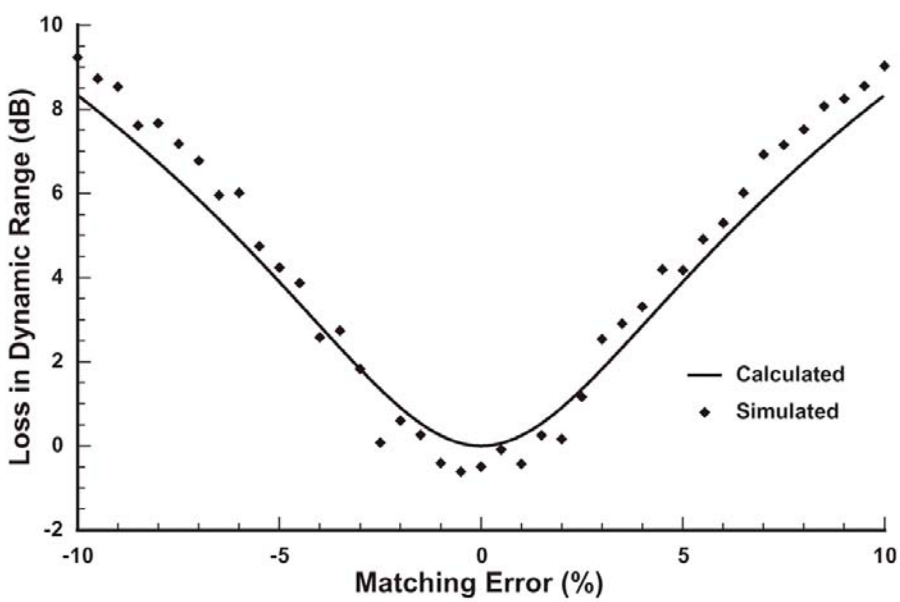
Cascaded Modulators: 2-1 Architecture



$$Y_1 = z^{-2}X + (1 - z^{-1})^2 E_1$$

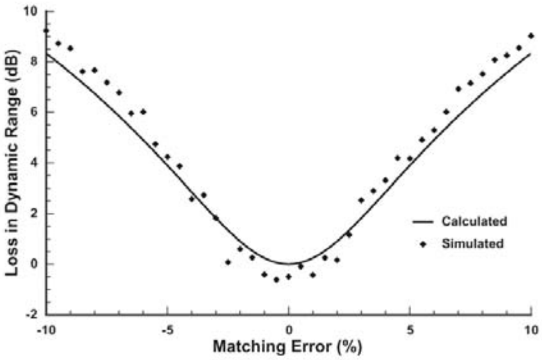
$$Y_2 = z^{-1}E_1 + (1 - z^{-1}) E_2$$

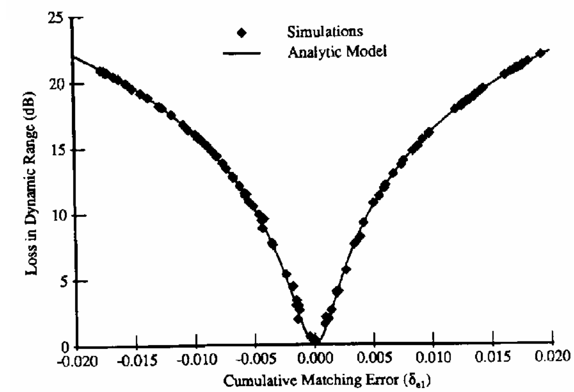
Effect of Coefficient Mismatches



Comparison of Cascades

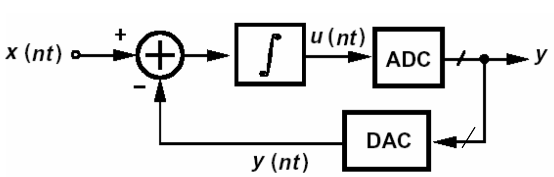
2-1 Cascade | **1-1-1 Cascade**

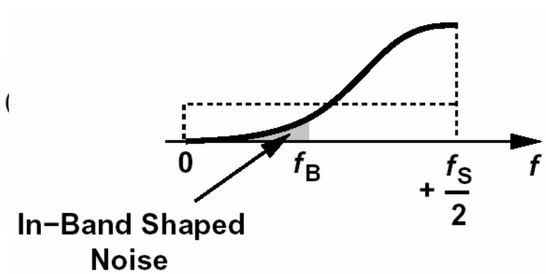




[Williams & Wooley, TCAS, May 91]

Use of Multibit Quantizer and DAC





$$S_Y(f) = S_Q(f)\left|\frac{Y}{Q}\right|^2$$

$$P_{tot} = \frac{\pi^2}{3}\left(\frac{2f_B}{f_S}\right)^3 \frac{\Delta^2}{12}$$

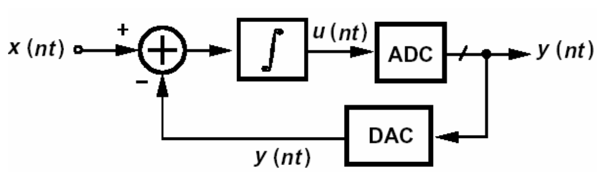
Oversampling Ratio, *M*

- **An N-bit quantizer improves DR by a factor of 2^N-1.**

Advantages of Multibit Quantization

- Direct Increase in DR
- Lower Quantization Noise Leakage in Cascades
  → Mismatch and settling requirements relaxed
- Smaller Steps at Input of Integrator
  → Faster settling
- More Linear Quantizer
  → Higher Stability
  → More aggressive NTF

Problem of DAC Nonlinearity



- DAC nonlinearity in first modulator directly adds to input signal.
- Solutions:
  - Use a multibit DAC only in the latter stages of a cascade.
    → But many advantages vanish.
  - Calibrate DAC.
  - Use dynamic element matching.
  - Shape and move the mismatches to high frequencies