Folding and Interpolating ADCs

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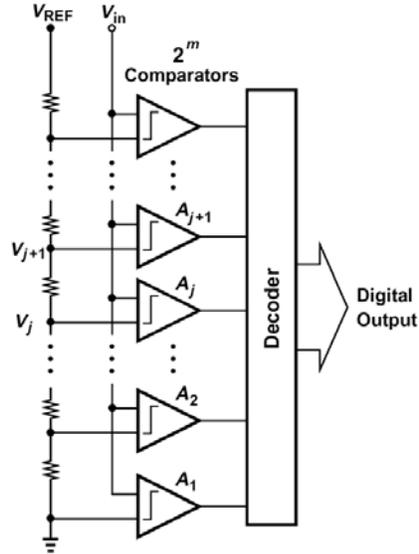
Outline

- **Quantization as Collection of Zero Crossings**
- **Interpolation**
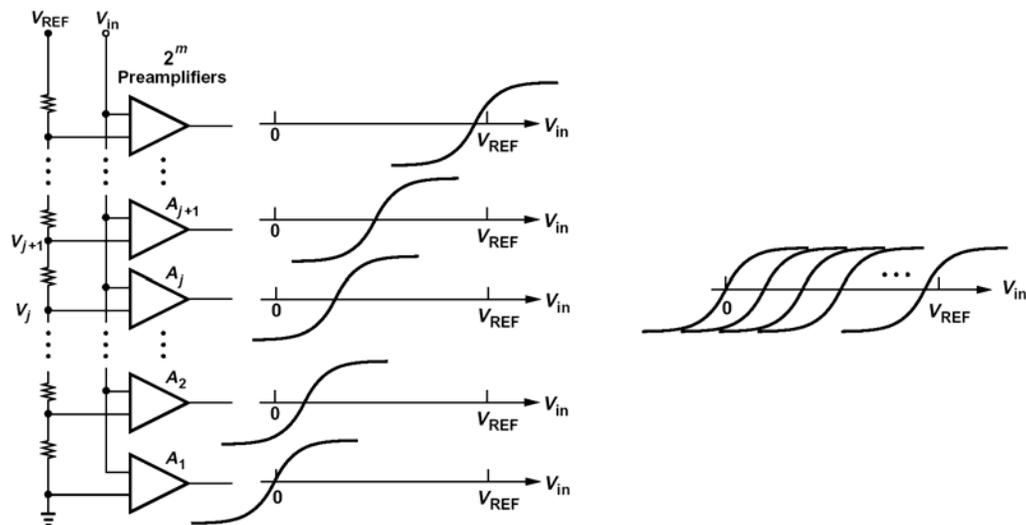- **Folding**
- **Design Issues**

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Flash Architecture

Issues:

- Input Capacitance
- Comparator Offset
- Power Dissipation
- Area and Routing
- Input Feedthrough
- Input−Dependent Delay
- Kickback Noise
- Sparkles (Bubbles)
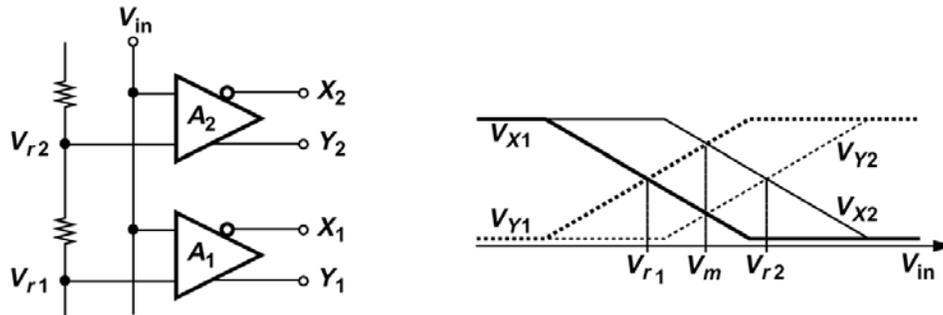- Metastability
- Clock Jitter and Dispersion

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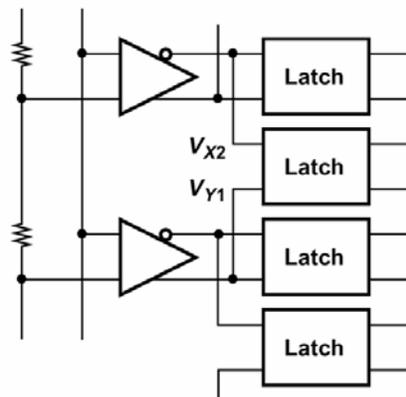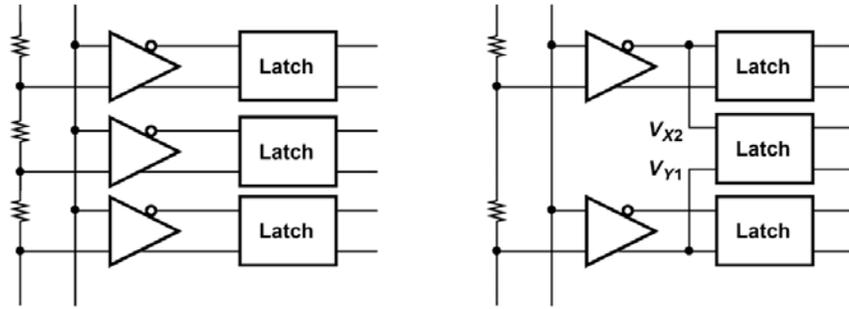# Quantization as a Collection of Zero Crossings

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Interpolation

Flash with 2X Interpolation

- Halves the number of preamps and the input cap.
- But does not reduce the number of latches.
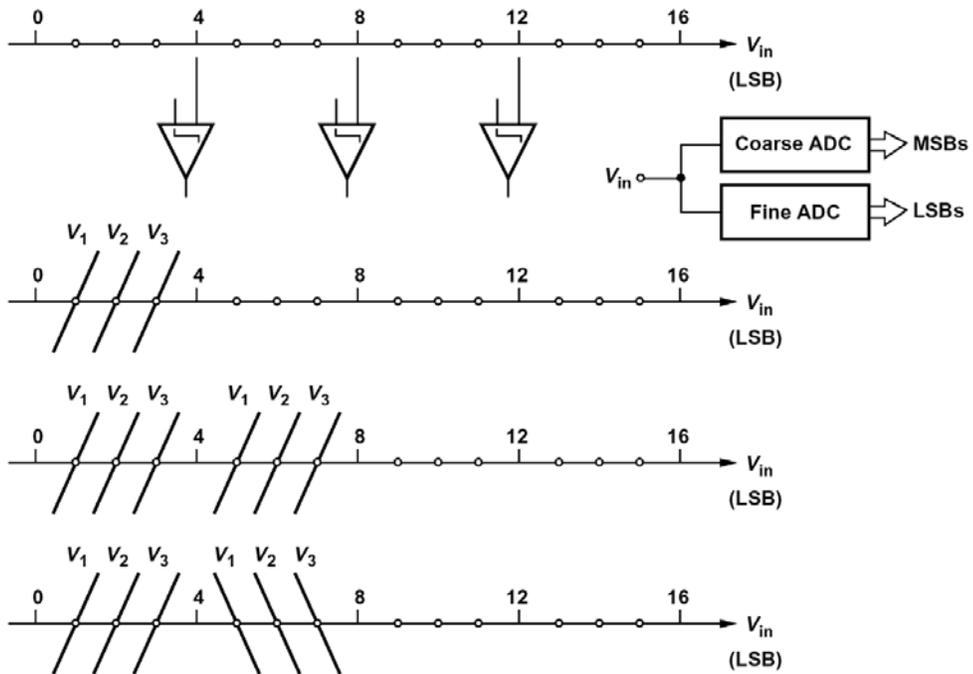
Reduction of DNL
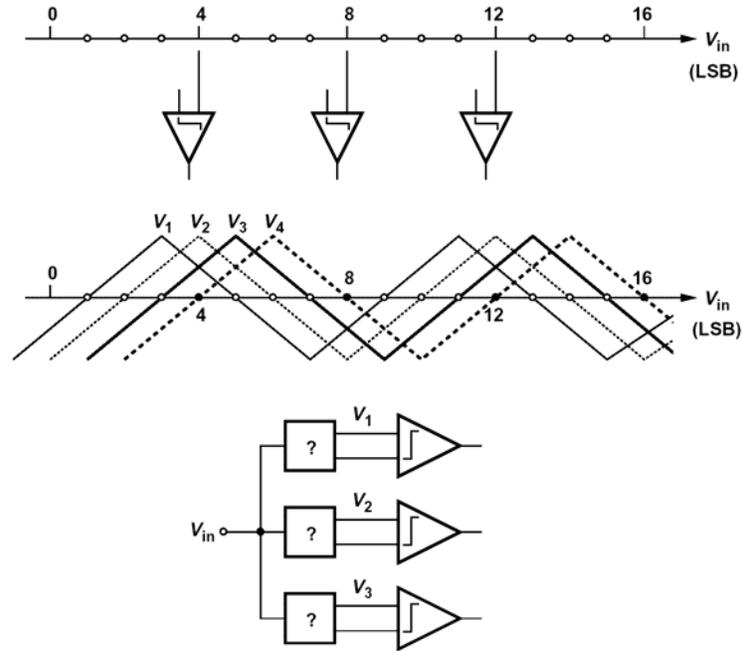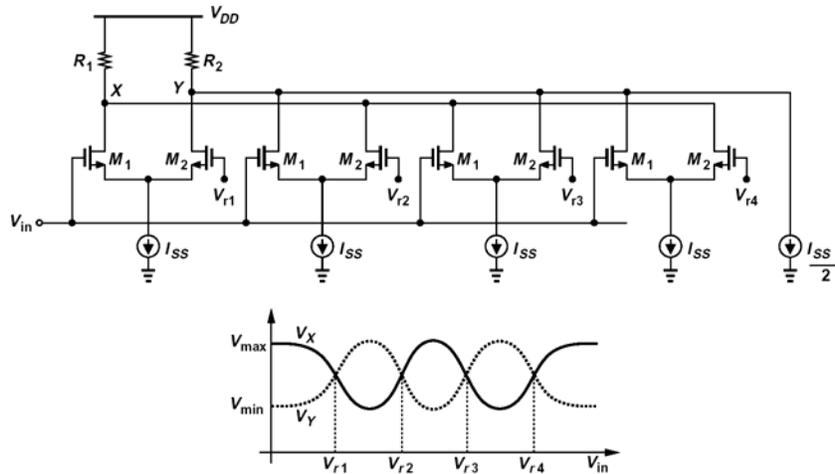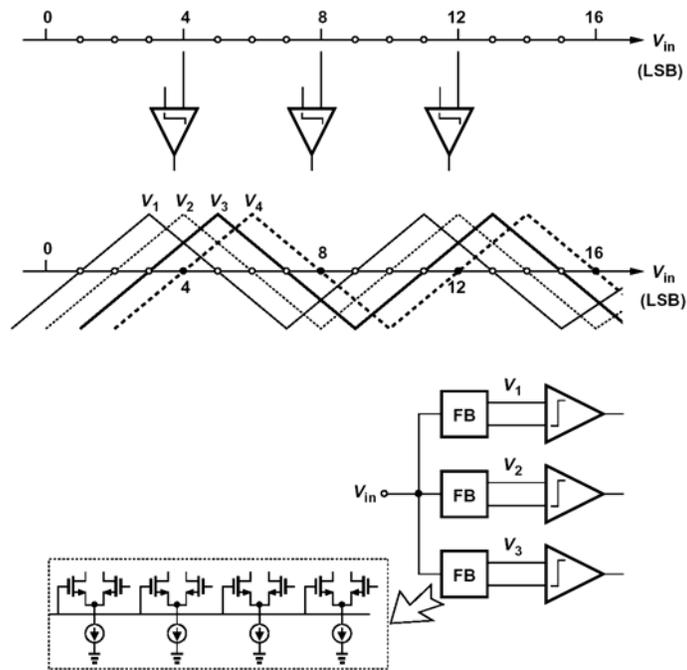
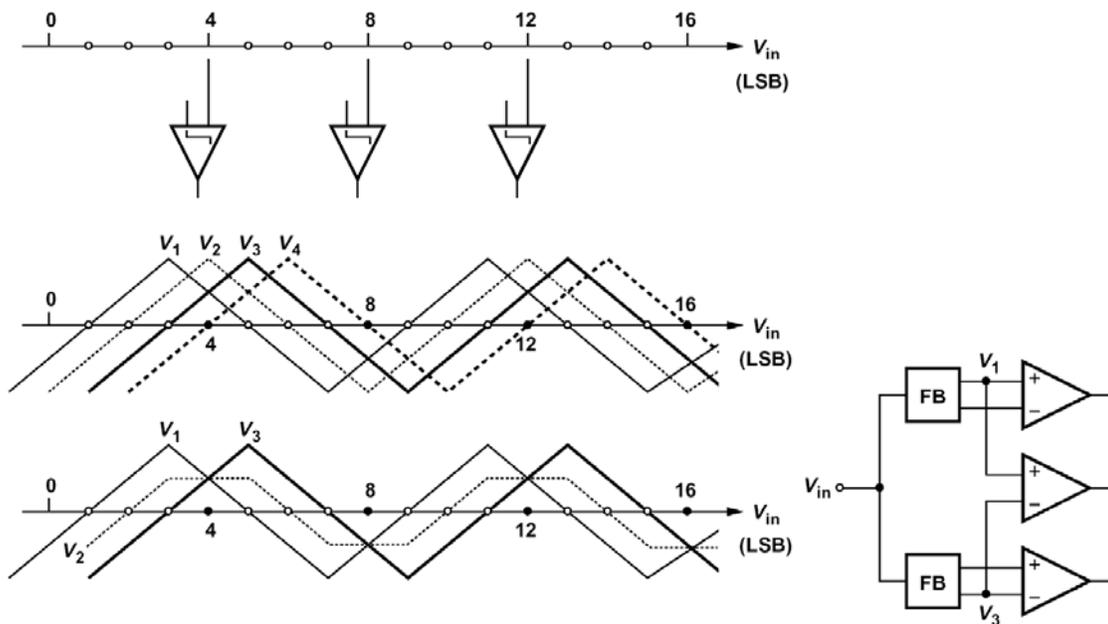# Folding 101

More Details

Implementation
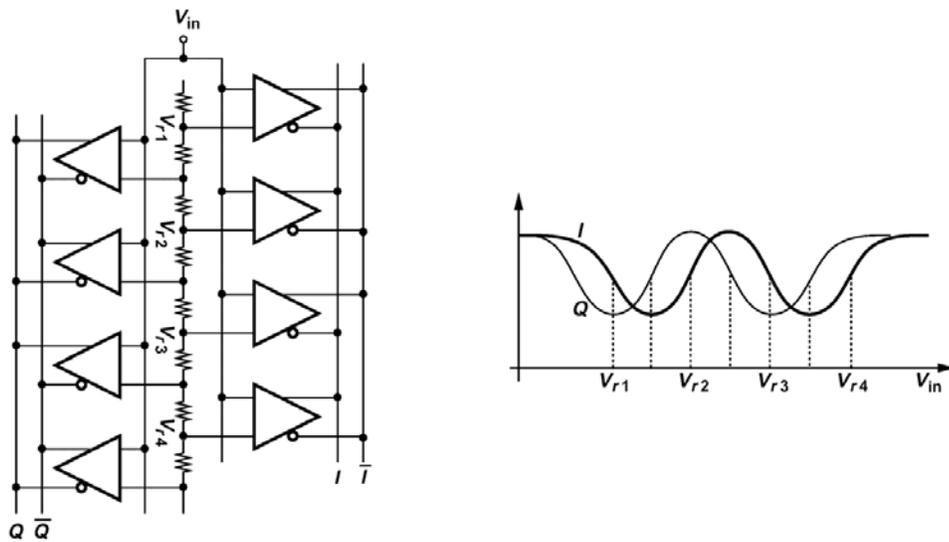
Complete 4-Bit ADC

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Interpolation with Folding
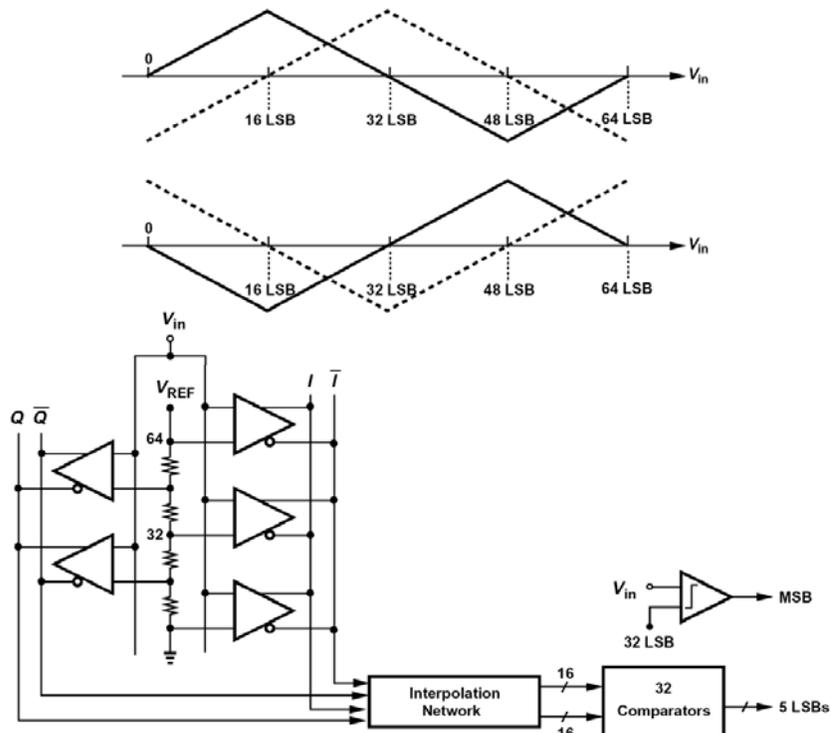

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Folding with Interpolation

- Can interpolate between I and Q outputs.
- Still need a coarse converter.

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6-Bit Example
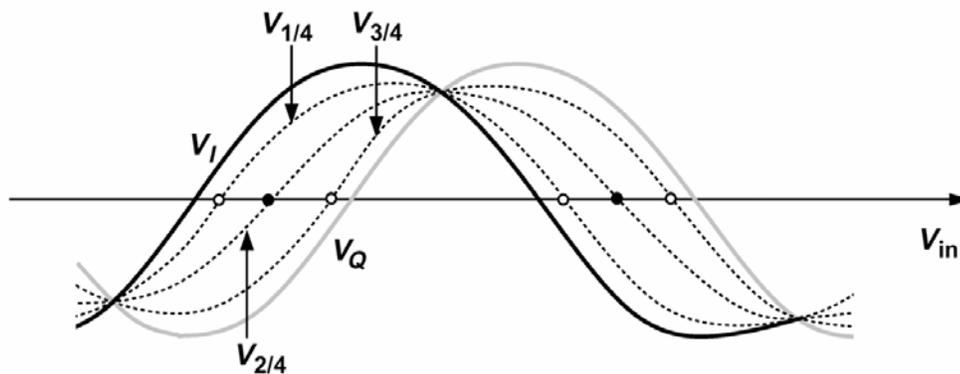

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Advantages of Folding

- **Mantains the "one-step" nature of flash conversion.**
- **No need for interstage DAC, subtractor, residue amp**
- **Extracts information from zero crossings → no need for "linear" processing**
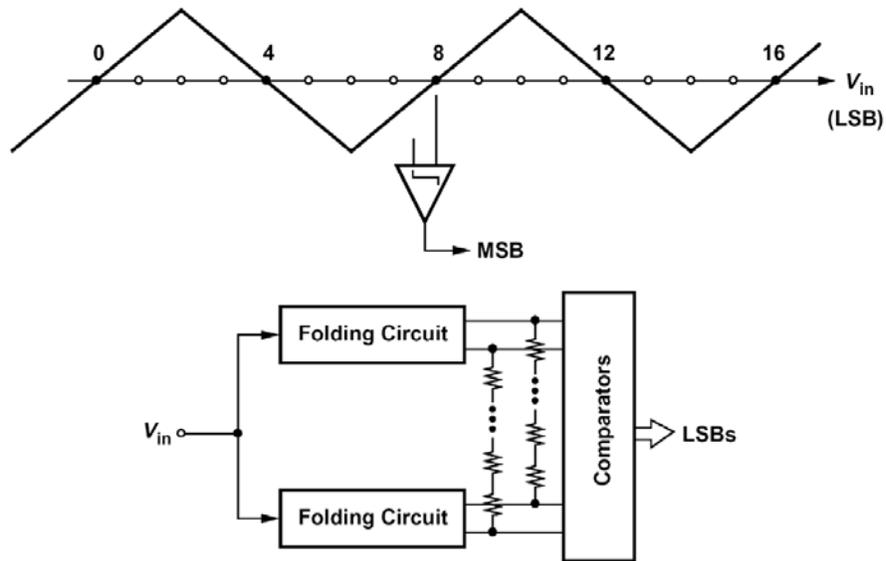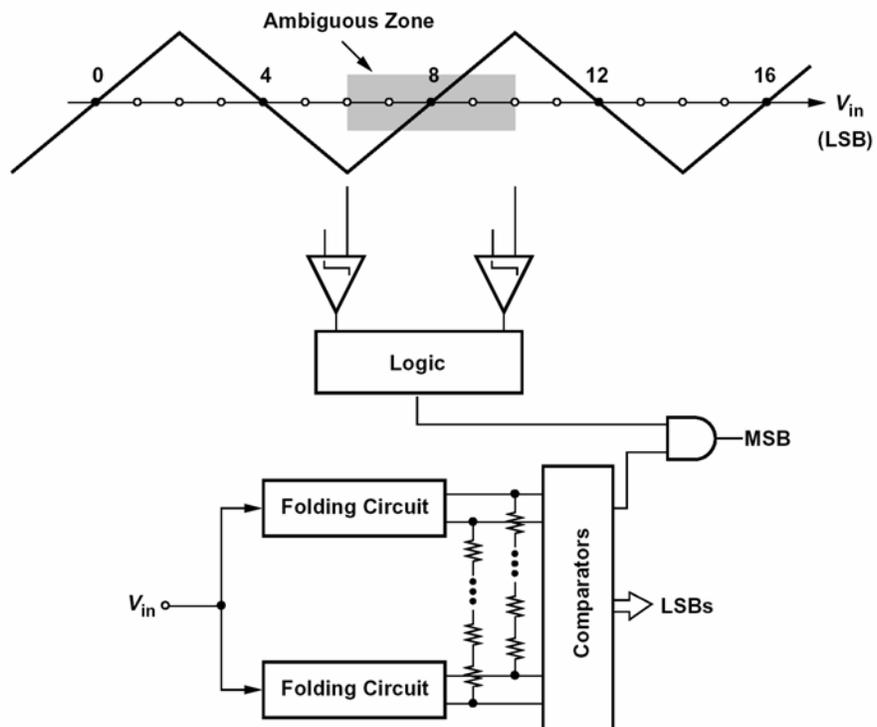- **Compact and efficient**

Problem of Nonlinearity
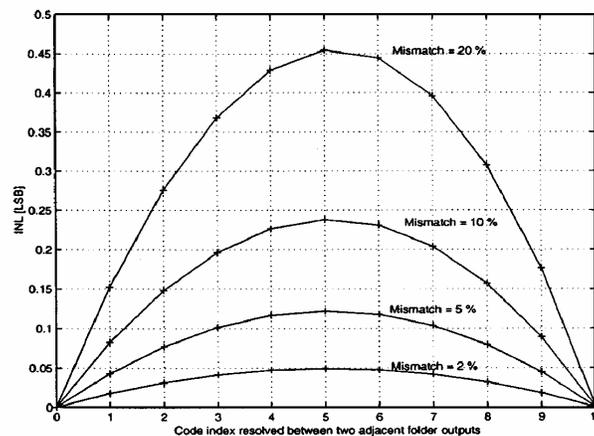
Offset in Coarse Stage
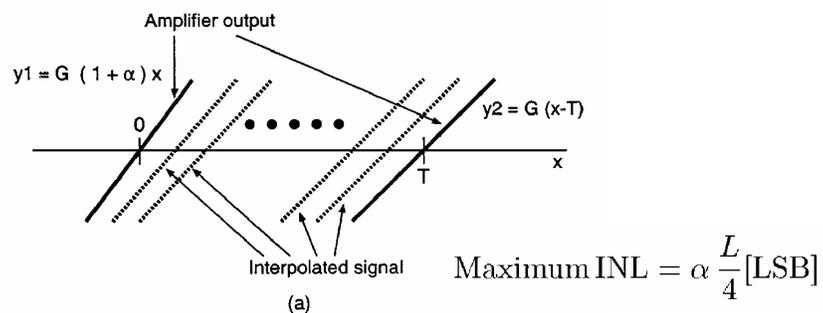
Problem of Ambiguity

Folding Issues

- **Frequency Multiplication at Folding Nodes**
- **Reduced BW at Folding Nodes**
- **Diff Pair Gm Mismatch**
- **Tail Current Mismatch**
- **Trade-Off Between Linearity and Gain**

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Gm Mismatch
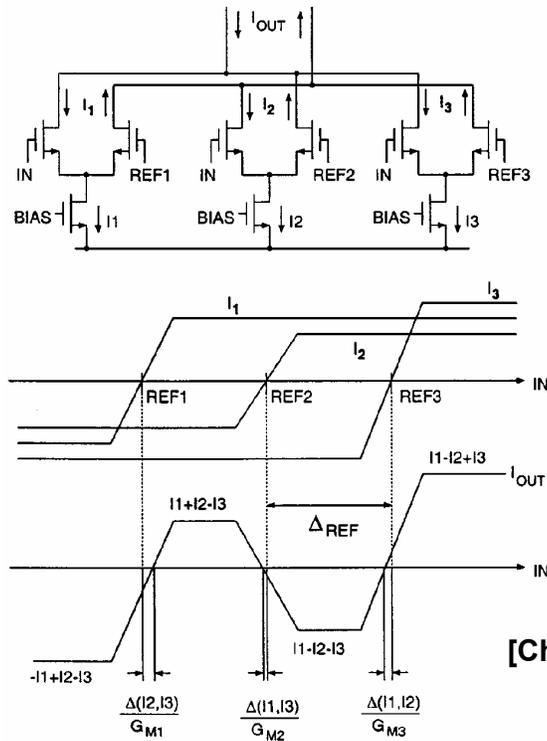

$$\text{Maximum INL} = \alpha \frac{L}{4} [\text{LSB}]$$

[Choe, JSSC, Feb. 01]

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Tail Current Mismatch

[Choe, JSSC, Feb. 01]

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