Folding and Interpolating ADCs

Behzad Razavi

Electrical Engineering Department
University of California, Los Angeles

Outline

- Quantization as Collection of Zero Crossings
- Interpolation
- Folding
- Design Issues
Flash Architecture

Issues:
- Input Capacitance
- Comparator Offset
- Power Dissipation
- Area and Routing
- Input Feedthrough
- Input–Dependent Delay
- Kickback Noise
- Sparkles (Bubbles)
- Metastability
- Clock Jitter and Dispersion

Quantization as a Collection of Zero Crossings
Interpolation

Flash with 2X Interpolation

- Halves the number of preamps and the input cap.
- But does not reduce the number of latches.
Reduction of DNL

Folding 101
More Details

Implementation
Complete 4-Bit ADC

Interpolation with Folding
Folding with Interpolation

- Can interpolate between I and Q outputs.
- Still need a coarse converter.

6-Bit Example
Advantages of Folding

- Maintains the “one-step” nature of flash conversion.
- No need for interstage DAC, subtractor, residue amp
- Extracts information from zero crossings → no need for “linear” processing
- Compact and efficient

Problem of Nonlinearity

[Diagram showing a waveform with markers at V_{1/4}, V_{3/4}, V_{2/4}, V_I, V_Q, V_{in}]

15

16
Offset in Coarse Stage

Problem of Ambiguity
Folding Issues

- Frequency Multiplication at Folding Nodes
- Reduced BW at Folding Nodes
- Diff Pair Gm Mismatch
- Tail Current Mismatch
- Trade-Off Between Linearity and Gain

Gm Mismatch

Maximum INL = $\alpha \frac{L}{4} [\text{LSB}]$

[Choe, JSSC, Feb. 01]
Tail Current Mismatch

[Choe, JSSC, Feb. 01]