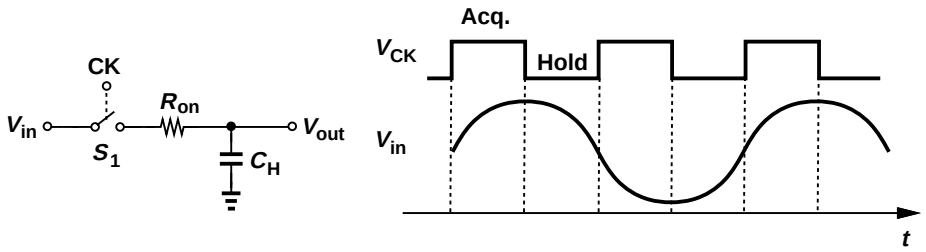
Homework #2

Due Tue., April 24, 2011

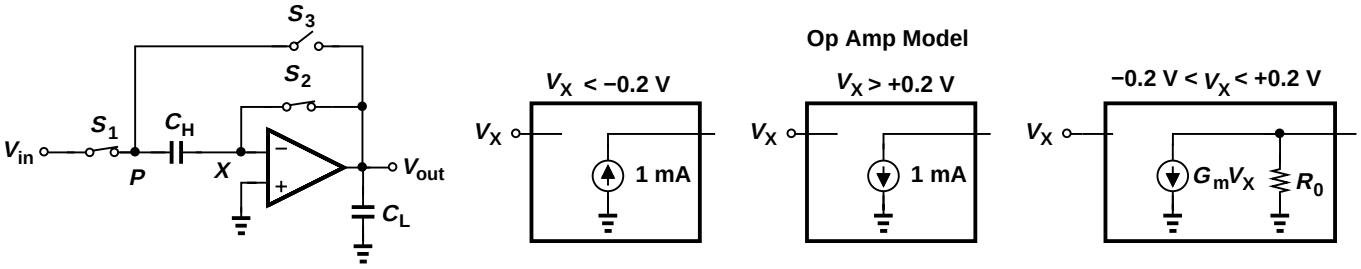
1. Consider the following sampling circuit, where $R_{on} = 400\ \Omega$ and $C_H = 0.35$ pF. The circuit has been designed for an 8-bit system.

(a) Suppose $V_{out}(t = 0) = 0$ and V_{in} is a constant, V_1. How long does it take the output to reach within 0.5 LSB of V_{in}?

(b) Suppose $V_{in} = V_1 \sin(2\pi f_{in} t)$, $V_1 = 0.35$ V, $f_{in} = 25$ MHz, and $f_{CK} = 2f_{in}$ (Nyquist sampling). For the case shown below, how long does it take the output to settle within 0.5 LSB of its "final" value?



2. Consider the switched-capacitor SHA shown below, where $C_H = C_L = 0.7$ pF and V_{in} is constant and equal to 1.1 V. Assume all switches are ideal and model the op amp as shown.



(a) At $t = 0$, S_1 and S_2 turn off and S_3 turns on and $V_{out}(0) = 0$. Plot the output voltage as a function of time and calculate the hold settling time to 0.5 LSB for 10-bit resolution.

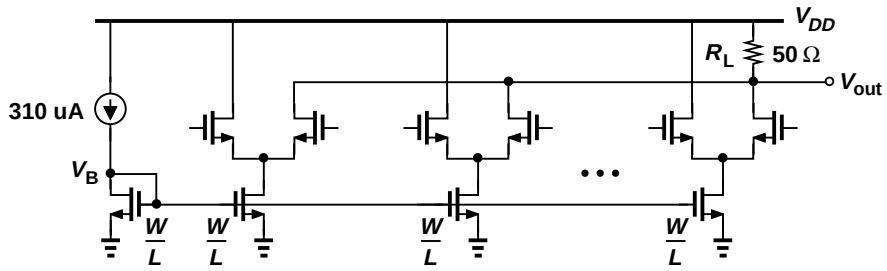
(b) Calculate the gain error of the SHA.

(c) Repeat (b) if the op amp has an input capacitance of 0.35 pF.

3. In this problem, we study the segmented section of a 10-bit current-steering CMOS DAC. The circuit consists of 64 nominally identical current switches, each delivering approximately 203 μA to a 50-Ω load so that the full-scale output is about 0.65 V. The supply voltage is 1.8 V. The 0.18-um MOS model files can be found at http://www.ee.ucla.edu/ brweb/teaching.html. (They are called 215a.sp and 215a.scs for HSPICE and Cadence, respectively. Source/drain junction areas and perimeters are given by 0.6 μm $\times W$ and 1.2 μm $+2W$, respectively.)

(a) Assume all of the devices are in saturation and their drawn length is 0.18 μm. If the gate of each transistor in the differential pairs is driven by signals having a high level equal to 1.5 V and a low level equal to 1.3 V, what is the minimum width of the two transistors required to switch 99% of the tail current?

(b) Using the width found in (a), calculate the maximum INL due to the finite output impedance of the current switches.



(c) To reduce the INL to 0.5 LSB, we increase the length of all of the current source devices and the mirror. What is the minimum length that satisfies this condition? Determine the minimum width such that each current source remains in saturation for $V_{DS} > 0.25$ V.

(d) Using HSPICE or Cadence, find the output settling time to 0.5 LSB of the final value. Use the device dimensions found in (a) and (c). You need not construct 64 subcircuits; you can simply use the factor "M" in HSPICE or Cadence to scale one complete current switch by a factor of 64.

(e) Add a very large capacitor (e.g., 1 μF) from V_B to ground and find the settling time. Does this improve the speed? Why?

(f) Suppose the maximum available on-chip capacitor is 4 pF. Would you use such a capacitor to improve the speed? Why?