Homework #4

Due Tue. May 8, 2012

1. In this problem, we study the effect of nonidealities on the performance of a two-step 10-bit ADC (with 5 bits resolved in each stage). For each of the following errors, explain how the input/output characteristic of the ADC is affected and demonstrate using proper plots (e.g. residue plots, input/output plots, etc.).

(a) Comparator A_j in the first stage has an offset voltage of $+1.4$ LSB. (Input offset is the voltage at which the output makes a transition.)

(b) The reference ladder of the first stage has an INL of $+0.9$ LSB at its midpoint.

(c) The DAC has an offset voltage of $+0.8$ LSB.

(d) The DAC has a gain error of $+0.04\%$.

(e) The DAC has a DNL of $+1.6$ LSB.

(f) The DAC has an INL of $+1.8$ LSB.

(g) The subtractor has an offset of $+1.6$ LSB.

(h) The subtractor has a gain error $+0.6\%$.

(i) The subtractor has an INL of $+1.1$ LSB.

(j) Suppose the subtractor has a nominal voltage gain of 4. What should the full-scale voltage of the second stage be (in LSB)? How much error can we tolerate in the gain of the subtractor or the full-scale voltage of the second stage if the DNL is to remain below 0.6 LSB? How much comparator offset is allowed in the second stage?

2. Design an 8-bit folding and interpolating ADC. Consider two cases:

(a) The analog input can be loaded by at most 32 differential pairs.

(b) The analog input can be loaded by at most 64 differential pairs.

(Assume the input stage of each comparator requires a differential pair.) Provide a diagram similar to that of the 6-bit example in the lecture notes for each case, but also show the interpolation network in detail. Summarize the hardware requirements in two tables, showing the total number of differential pairs, comparators, and resistors for each case. (You need not count the load resistors used in the differential pairs.)