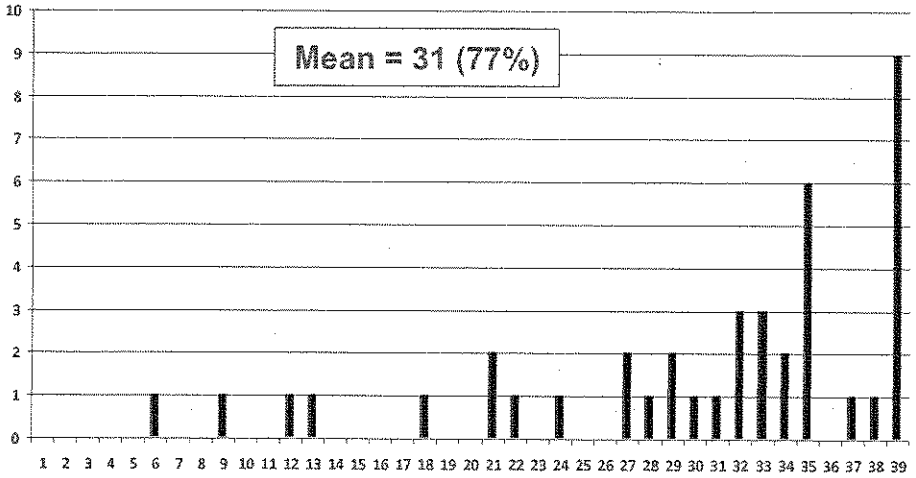
EE 215D

Midterm Exam

Spring 2012

Name: Solutions



1. 10

2. 10

3. 10

4. 10

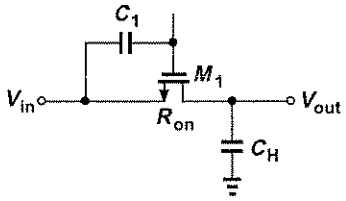
Total: 40

1. Consider the bootstrapped sampling circuit shown below, where the body of M_1 is tied to ground and the rest of the bootstrap network is not shown.

(a) If body effect is not neglected, *sketch* the on-resistance of M_1 as a function of V_{in}. You need not write equations.

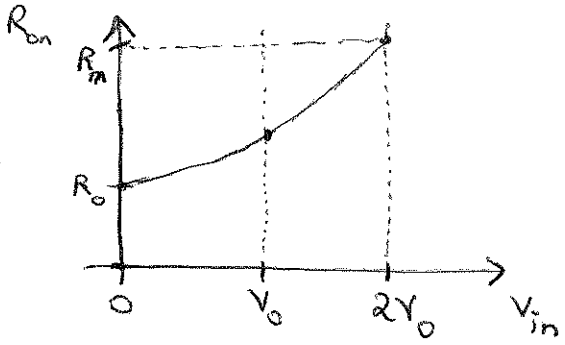
(b) Approximating the characteristic in (a) by a straight line passing through its end points, sketch R_{on} as a function of time. Assume $V_{in}(t) = V_0 \cos \omega_0 t + V_0$.

(c) Calculate the second harmonic amplitude at the output arising from phase distortion. Assume that the phase shift is much less than 1 radian.



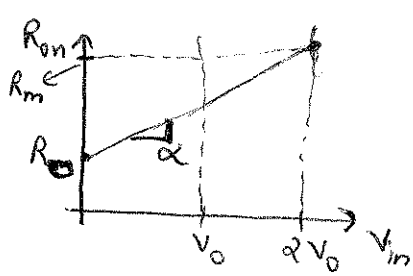
a)

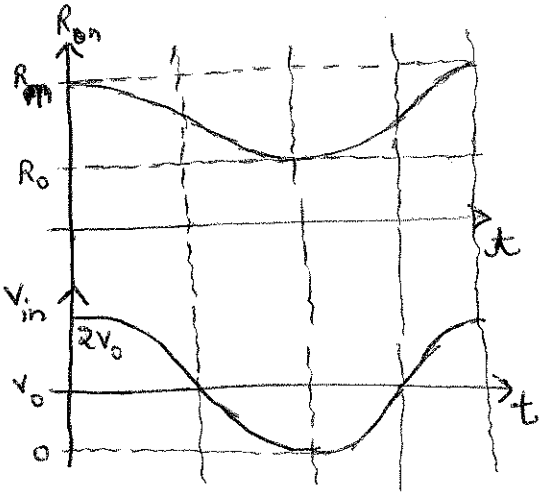
$$R_{on} = \frac{1}{k\frac{W}{L}\left\{V_{GS} - V_{tho} - \gamma\left(\sqrt{\phi + V_{SB}} - \sqrt{\phi}\right)\right\}} \quad \& \; V_{SB} = V_{in}$$



$V_{th} \uparrow$ as $V_{in} \uparrow$ and hence, R_{on} increases

b)





$$R_{on} = R_0 + \alpha(V_0 + V_0 \cos \omega_0 t)$$

c)

$$V_{out} \simeq V_0 + V_0 \cos\left(\omega_0 t - \tan^{-1}(\omega_0 R_{on} C_H)\right)$$

$$\simeq V_0 + V_0 \cos\left(\omega_0 t - \omega_0 R_{on} C_H\right)$$

$$\simeq V_0 + V_0 \cos(\omega_0 t) + V_0 \sin(\omega_0 t)\left\{\omega_0 R_{on} C_H\right\}$$

(for $\omega_0 R_{on} C_H \ll 1$ rad)

$$= V_0 + V_0 \cos(\omega_0 t) + V_0 \sin(\omega_0 t)\left\{\omega_0 R_0 C_H + \omega_0 \alpha V_0 C_H\right\}$$

$$+ \frac{1}{2} V_0^2 \alpha\, \omega_0 C_H \sin(2\omega_0 t)$$

2nd Harmonic Amplitude $\longrightarrow$ $\boxed{\frac{1}{2} V_0^2 \alpha\, \omega_0 C_H}$

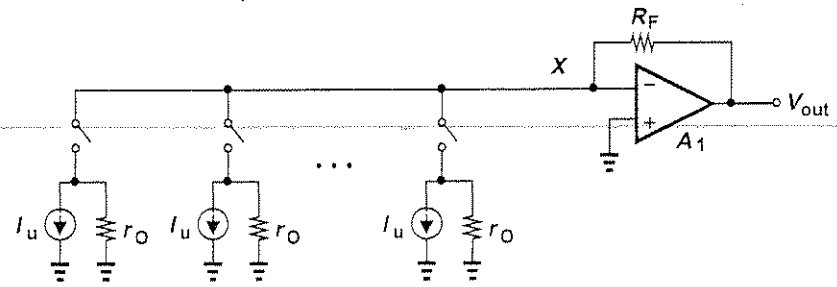
where α is given by

$$R_{on} = R_0 + \alpha V_{in}$$

2. A segmented current-steering DAC consists of N current sources and is followed by a transimpedance amplifier as shown below. Assume the op amp has a gain of A_1 but is otherwise ideal.

(a) Estimate the INL at node X. (7pt)

(b) Estimate the INL at the output. (3pt)



$V_{out} = -A_1 V_X$

KCL at Node X when n switches are on:

$$\frac{V_{out} - V_X(n)}{R_F} = n I_u + n \frac{V_X}{r_o}$$

$$\Rightarrow V_X(n) = -\frac{n I_u r_o R_F}{n R_F + (A_1+1) r_o}$$

$$\therefore V_X(0) = 0, \quad V_X(N) = -\frac{N I_u r_o R_F}{N R_F + (A_1+1) r_o}$$

$$\Rightarrow V_{X,ideal}(n) = -\frac{n I_u r_o R_F}{N R_F + (A_1+1) r_o}$$

(a) $$INL_X(n) = V_X(n) - V_{X,ideal}(n) = \frac{I_u r_o R_F^2}{N R_F + (A_1+1) r_o} \cdot \frac{n(n-N)}{n R_F + (A_1+1) r_o}$$

(b) Since $V_{out} = -A_1 V_X$

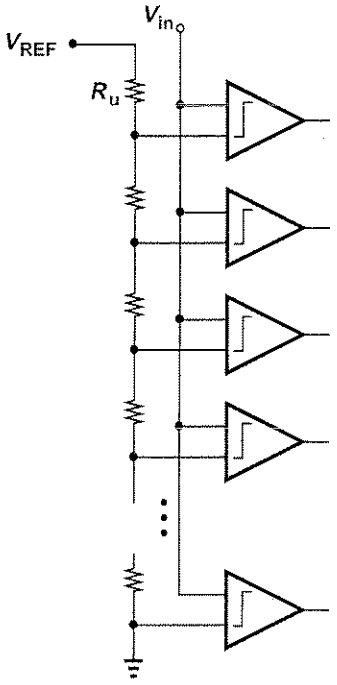
$$INL_{out}(n) = -A_1 \cdot INL_X(n) = \frac{A_1 I_u r_o R_F^2}{N R_F + (A_1+1) r_o} \cdot \frac{n(N-n)}{n R_F + (A_1+1) r_o}$$

3. Consider the flash ADC shown below. Assume V_{in} is provided by an ideal voltage source.

(a) If the kickback noise currents of all comparators are equal and denoted by $I(t)$, determine the largest perturbation voltage on the ladder. Assume $I(t)$ is small.

(b) Now assume that V_{in} is provided through a source impedance of R_S. Compute the differential voltage experienced by the comparator tied to $V_{REF}/2$. Assume that the kickback noise currents drawn by the two inputs of each comparator are equal.

(c) Suppose we choose the total ladder resistance equal to $8R_S$. Which comparator does now experience the largest differential error?



(a) The perturbation at node j:

$$\Delta V_j = -\frac{I}{2} \cdot Ru \cdot (j(N-j))$$

$$\Rightarrow \frac{\partial \Delta V_j}{\partial j} = 0 \Rightarrow j = \frac{N}{2}$$

and $$\Delta V_{max} = -\frac{I}{8} \cdot Ru \cdot N^2$$

(b) The perturbation at input is $-I \cdot N \cdot R_S$

Diff. voltage at $j = \frac{N}{2}$:

$$-I \cdot N \cdot R_S + \frac{I}{8} \cdot Ru \cdot N^2 = -I \cdot N\left(R_S - \frac{Ru \cdot N}{8}\right)$$

(c) With $Ru = \frac{8R_S}{N}$,

Differential error is $-INR_S + \frac{I}{2}\frac{8R_S}{N}(j(N-j))$

$$= I \cdot R_S\left(-N + \frac{4(j(N-j))}{N}\right) = f(j), \quad j = 0 \sim N-1$$

$$\frac{\partial f(j)}{\partial j} = 0 \Rightarrow j = \frac{N}{2}, \quad \text{but } f\left(\frac{N}{2}\right) = 0$$

$\Rightarrow$ The first the the last comparator experience the largest error.

4. Consider the 10-bit two-step ADC studied in Homework 4, where each stage resolves 5 bits. Assume that the DAC employs a resistor ladder as shown below. Analyze the following two cases independently.

(a) Suppose the outputs of NAND gates j and $j+1$ are accidentally swapped. Construct the residue plot and the input/output characteristic.

(a) Suppose the outputs of NAND gates j and $j+2$ are accidentally swapped. Construct the residue plot and the input/output characteristic.