EE 215D

Midterm Exam

Spring 2011

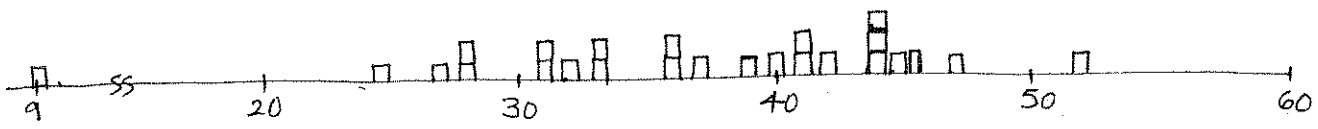
Name: Solutions

Time Limit: 2 Hours

Open Book, Open Notes

1. 15
2. 15
3. 15
4. 15

Total: 60



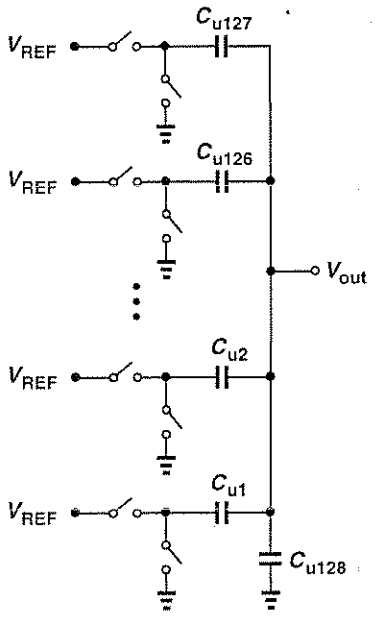
Mean = 36.4/60 = 61%

Median = 33.5/60 = 56%

1. A 7-bit segmented capacitor DAC is shown below. Code 0 produces $V_{out} = 0$ and code 127 switches the left plates of C_{u1}-C_{u127} from 0 to V_{REF}. Due to a layout error, capacitor number 63 has been omitted. Neglect all other capacitances. Assume a zero initial condition at the output. (15)

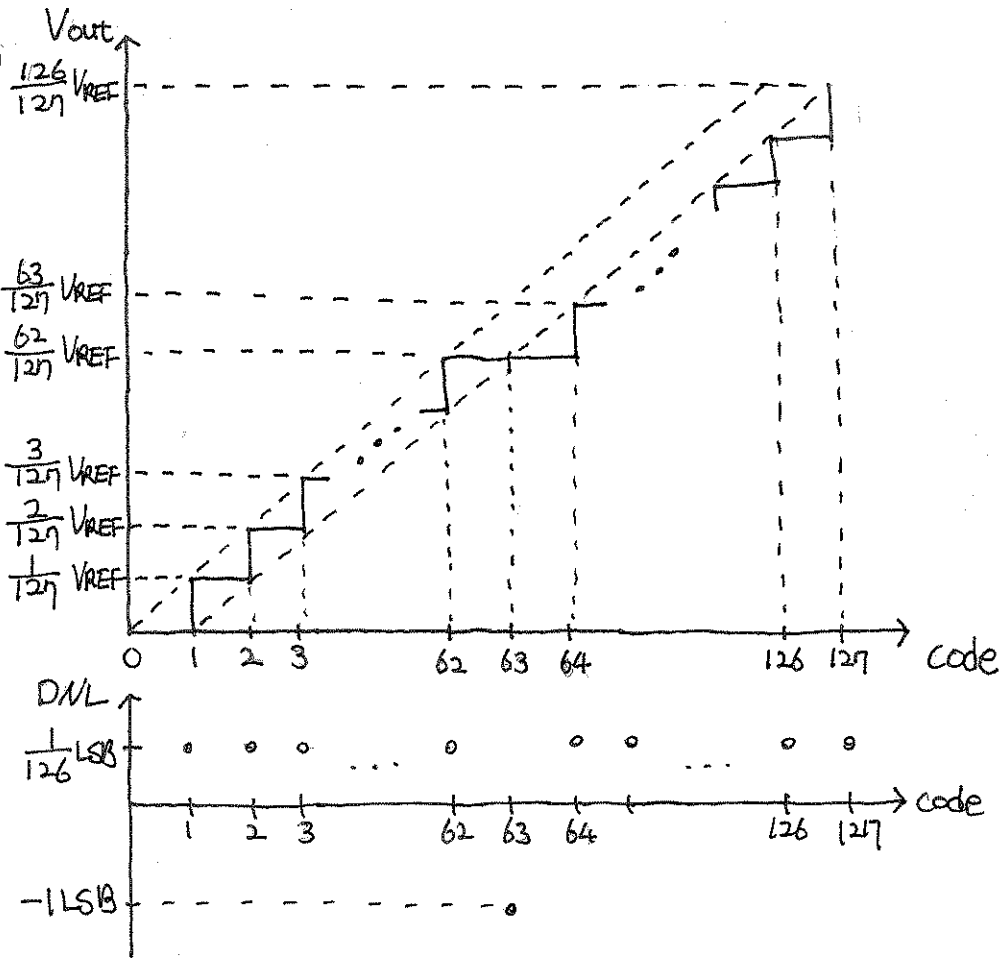
(a) Sketch the input/output characteristic, indicating the exact end points. Determine the maximum DNL.

(b) Sketch the INL profile.



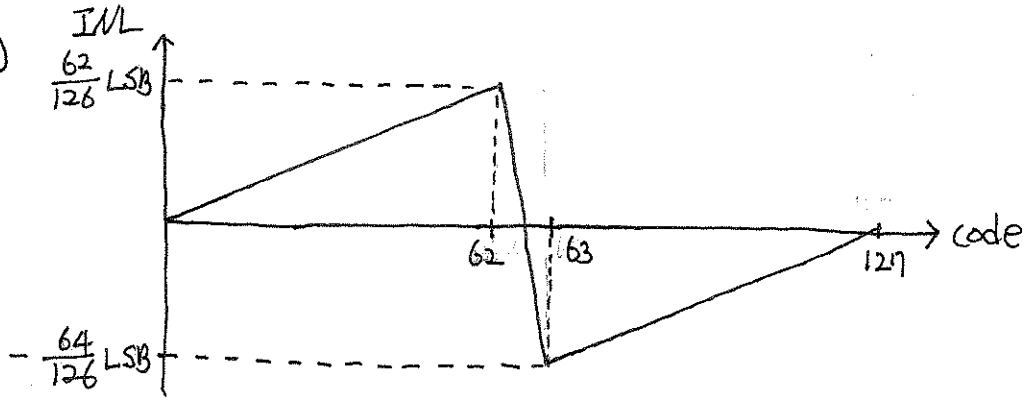
$$LSB = \frac{1}{127} \times \frac{126}{127} V_{REF}$$

(a)



Max. DNL = 1 LSB @ 63

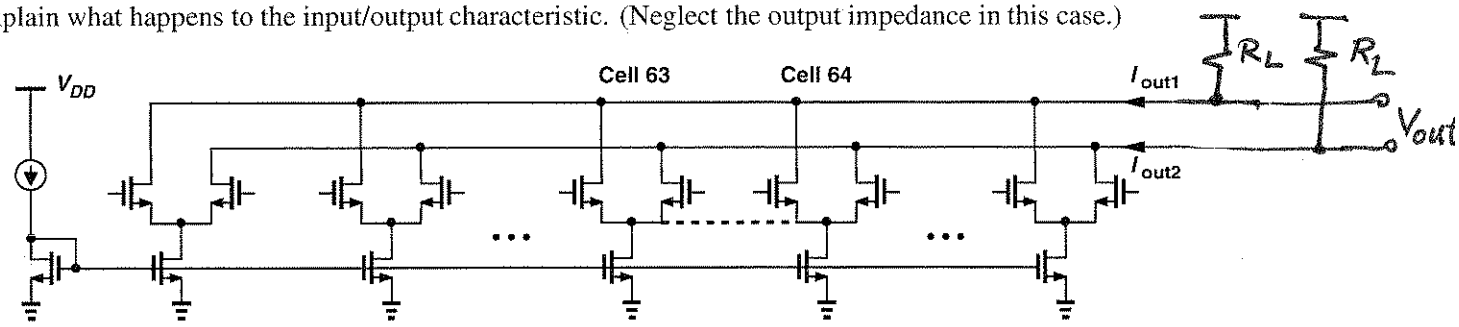
(b)



2. The 7-bit segmented current-steering DAC shown below employs 128 current sources nominally equal to I_0. Code 0 routes all of the tail currents to I_{out1} and code 127 routes all of the tail currents to I_{out2}. The output of interest is $I_{out1} - I_{out2}$. Neglect all mismatches. (15)

(a) If each current cell has a single-ended output resistance of R_1, determine the maximum INL of the DAC.

(b) The common source nodes of the differential pairs in cells 63 and 64 are accidentally shorted (the dashed line). Explain what happens to the input/output characteristic. (Neglect the output impedance in this case.)



(a)

Code $\phi \Rightarrow V_{out} = -N I_o \left(\frac{R_1}{N} \| R_L \right)$

Code 127 $\Rightarrow V_{out} = N I_o \left(\frac{R_1}{N} \| R_L \right)$ 2

$\Rightarrow$ Straigh line: $V_{out}(j) = (2j - N) I_o \left(\frac{R_1}{N} \| R_L \right) = \frac{R_1 \cdot R_L I_o (2j-N)}{R_1 + N R_L}$ 2

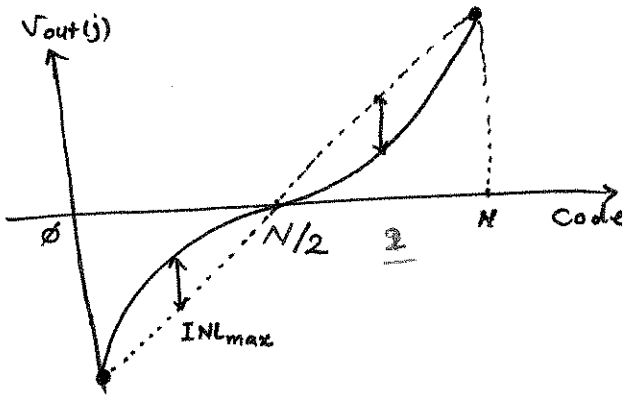
$$V_{out}(j) = j I_o \left(\frac{R_1}{j} \| R_L \right) - (N-j) I_o \left(\frac{R_1}{N-j} \| R_L \right) =$$

$$= \frac{I_o R_1 R_L}{R_1/j + R_L} - \frac{I_o R_1 R_L}{R_1/(N-j) + R_L} = I_o R_1 R_L \frac{R_1 \left(\frac{1}{N-j} - \frac{1}{j} \right)}{\left(\frac{R_1}{j} + R_L \right)\left(\frac{R_1}{N-j} + R_L \right)}$$

$$= \frac{I_o R_1^2 R_L (2j-N)}{(R_1 + jR_L)(R_1 + (N-j)R_L)}$$ 2

$$\Rightarrow INL_j = I_o R_1 R_L (2j-N) \cdot \left[\frac{R_1}{(R_1 + jR_L)(R_1 + (N-j)R_L)} - \frac{1}{R_1 + NR_L} \right]$$

due to Symmetry it is evident that INL_{max} happens at $j = \frac{N}{4}, \frac{3}{4}N$ 1



$$\Rightarrow INL_{max} = I_o R_1 R_L \left(\frac{N}{2} \right) \left[\frac{R_1}{\left(R_1 + \frac{3N}{4} R_L \right)\left(R_1 + \frac{R_L N}{4} \right)} - \frac{1}{R_1 + NR_L} \right]$$

assuming $R_1 >> NR_L$

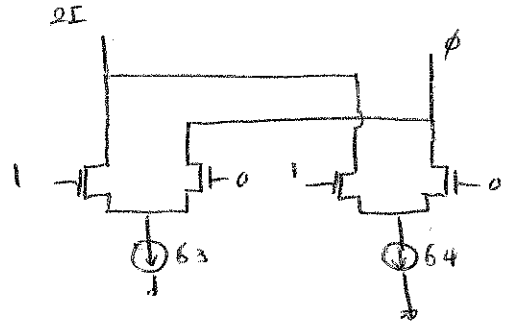
$$INL_{max} \approx I_o R_1 R_L \left(\frac{N}{2} \right)\left(\frac{3N}{16} \right) \frac{R_L^2}{R_1^3} = \frac{3N^2}{32} (I_o R_L) \left(\frac{R_L}{R_1} \right)^2 \quad (V)$$ 2

$$INL_{max} = \frac{3N}{32} \left(\frac{R_L}{R_1} \right)^2 \quad (\%)$$

(b)

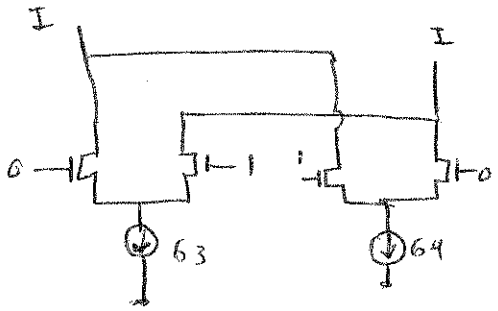
Due to the differential operation, the ADC characteristic does not change. To illustrate, we can zoom into 63rd and 64th current sources:

when 63rd is ~~on~~ off and 64th is off:

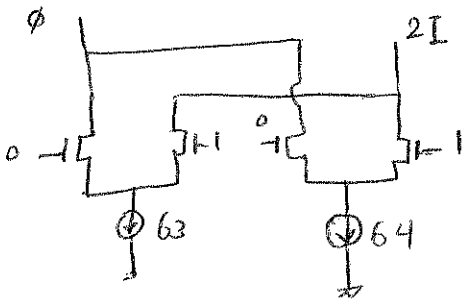


4

when 63rd is on and 64th is off:



when both are on



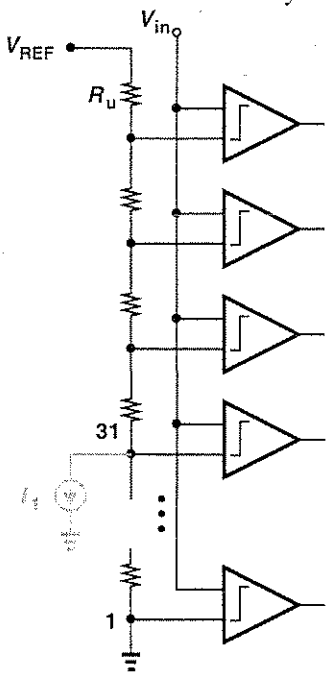
3. A 6-bit flash ADC is shown below. The output of interest is the thermometer code generated by the comparators.

(a) Suppose comparator 31 has an offset of +2.8 LSB. (This means the comparator flips if V_{in} is 2.8 LSB *greater* than its reference voltage.) Sketch the input/output characteristic and clearly show the effect of this offset.

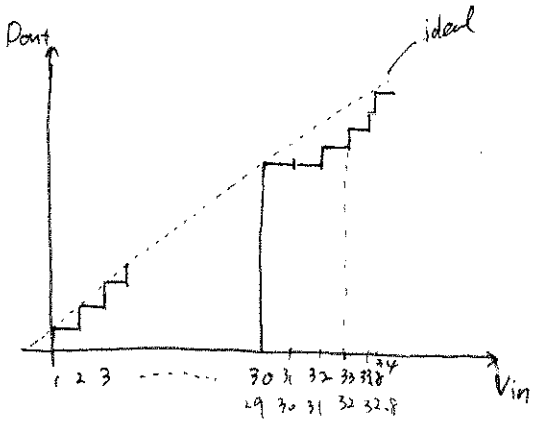
(b) Repeat part (a) for an offset of −2.8 LSB.

(c) A leakage current of I_1 has appeared at tap number 31 of the ladder. If $I_1 R_u = 0.1$ LSB, sketch the input/output characteristic and clearly show the effect of this current. (Neglect comparator offsets here.)

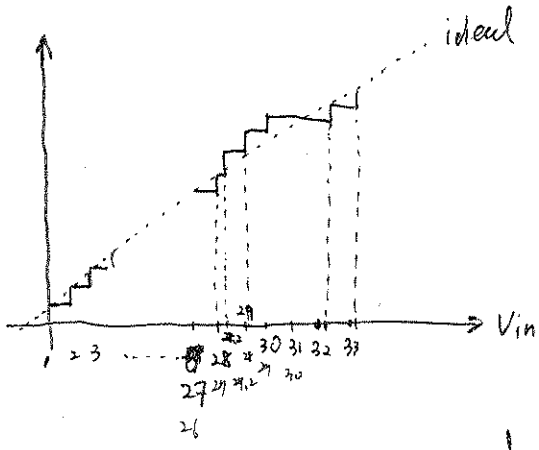
(15)



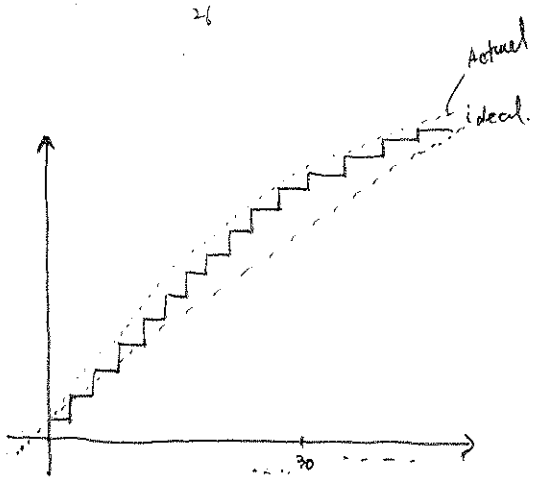
3. (a)



(b)



(c)



4. Consider a 6-bit flash ADC with 2x interpolation. The output of interest is the thermometer code generated by the latches.

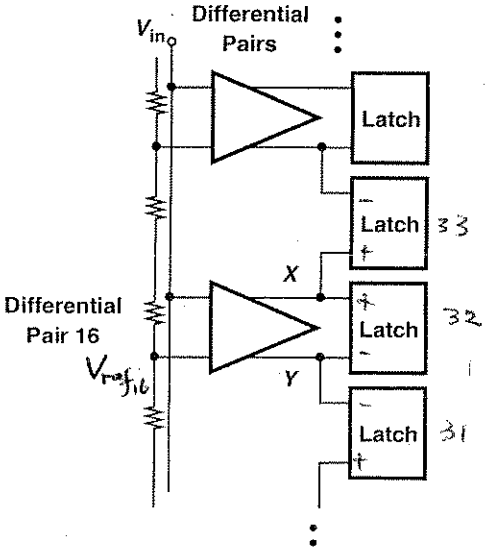
5 (a) Suppose differential pair number 16 has an offset of +3.2 LSB. (This means the differential output of the pair reaches zero if V_{in} is *greater* than its reference voltage by 3.2 LSB.) Sketch the input/output characteristic and clearly show the effect of this offset.

5 (b) Suppose differential pair number 16 has an offset of −3.2 LSB. Sketch the input/output characteristic and clearly show the effect of this offset.

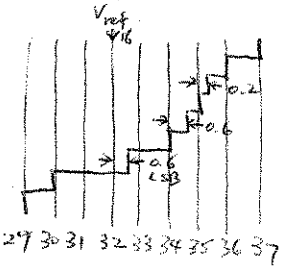
2.5 (c) In differential pair number 16, output X is shorted to V_{DD} and output Y to ground. Sketch the input/output characteristic and clearly show the effect of this layout error.

2.5 (d) Repeat part (c) if Y is shorted to V_{DD} and X to ground.

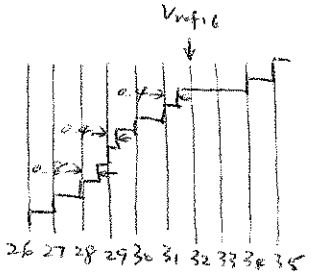
15



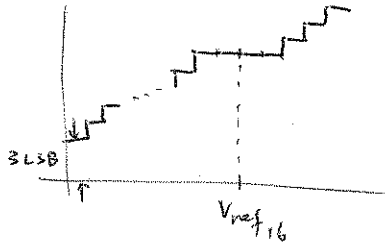
a)



b)



c) Latches 31, 32, 33 always "1"



d) Latches 31, 32, 33 always "0"

Same as c), without the 3 LSB offset

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1. 15
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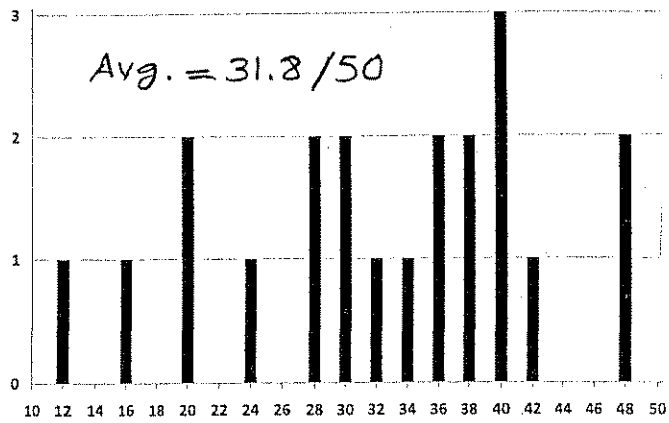
4. 15

Total: 50



1. A 6-bit segmented current-steering DAC employs 63 current sources nominally equal to I_0. Code 0 produces a zero output current and code 63 turns on all of the current sources.

(a) Due to a layout error, the 32nd current source is equal to $2I_0$ rather than I_0. Determine the maximum INL of the DAC.

(b) Repeat part (a) if only the first current source is equal to $2I_0$.

(c) Repeat part (a) if only the 63rd current source is equal to $2I_0$.

(15)

(a) $LSB = I_0$

Digital input	Real output	Reference	Error
000000	0	0	0
000001	I_0	$\frac{64}{63} I_0$	$-\frac{1}{63} I_0$
000010	$2 I_0$	$2 \times \frac{64}{63} I_0$	$-\frac{2}{63} I_0$
⋮	⋮	⋮	⋮
011111	$31 I_0$	$31 \times \frac{64}{63} I_0$	$-\frac{31}{63} I_0$
100000	$33 I_0$	$32 \times \frac{64}{63} I_0$	$\frac{31}{63} I_0$
100001	$34 I_0$	$33 \times \frac{64}{63} I_0$	$\frac{30}{63} I_0$
⋮	⋮	⋮	⋮
111110	$63 I_0$	$62 \times \frac{64}{63} I_0$	$\frac{1}{63} I_0$
111111	$64 I_0$	$63 \times \frac{64}{63} I_0$	0

→ max @ $j = 31, 32$

$\therefore INL_{max} = \pm \frac{31}{63} I_0 = \pm 0.4921$ LSB

(b)

Digital input	Real output	Reference	Error
000000	0	0	0
000001	$2 I_0$	$\frac{64}{63} I_0$	$\frac{62}{63} I_0$
000010	$3 I_0$	$2 \times \frac{64}{63} I_0$	$\frac{61}{63} I_0$
⋮	⋮	⋮	⋮
111110	$63 I_0$	$62 \times \frac{64}{63} I_0$	$\frac{1}{63} I_0$
111111	$64 I_0$	$63 \times \frac{64}{63} I_0$	0

→ max @ $j = 1$

$\therefore INL_{max} = \frac{62}{63} I_0 = 0.9841$ LSB

(c)

Digital input	Real output	Reference	Error
000000	0	0	0
000001	I_0	$\frac{64}{63} I_0$	$-\frac{1}{63} I_0$
000010	$2 I_0$	$2 \times \frac{64}{63} I_0$	$-\frac{2}{63} I_0$
⋮	⋮	⋮	⋮
111110	$62 I_0$	$62 \times \frac{64}{63} I_0$	$-\frac{62}{63} I_0$
111111	$64 I_0$	$63 \times \frac{64}{63} I_0$	0

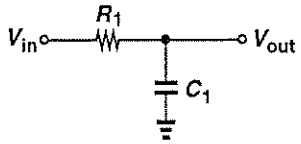
→ max @ $j = 62$

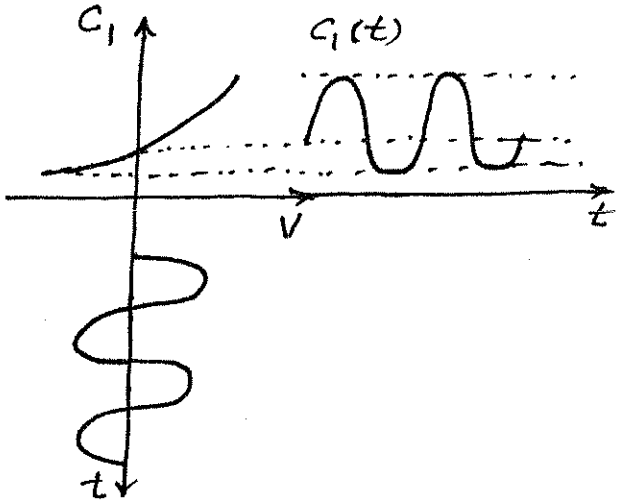
$\therefore INL_{max} = -\frac{62}{63} I_0 = -0.9841$ LSB

2. Consider the following representation of a sampling circuit in the acquisition mode. The resistor is assumed linear but the capacitor is nonlinear and expressed as $C_1 = g(V)$, where V denotes the voltage across the capacitor. If $V_{in} = V_0 \cos \omega_0 t$, $g(V)$ is monotonic, the nonlinearity of the circuit is small, and the amplitude attenuation is negligible,

(a) Write an expression for the output waveform and estimate the amplitude of the second harmonic.

(b) If two instances of the circuit are used for fully-differential operation and sense inputs equal to $\pm V_0 \cos \omega_0 t$, estimate the amplitude of the third harmonic in the differential output.





$$V_{out}(t) \approx V_0 \cos\left[\omega_0 t - \tan^{-1}(R_1 \omega_0 C_1)\right]$$

$$\approx V_0 \cos\omega_0 t + V_0 (\sin \omega_0 t)(R_1 \omega_0 C_1). \quad (1)$$

Method I

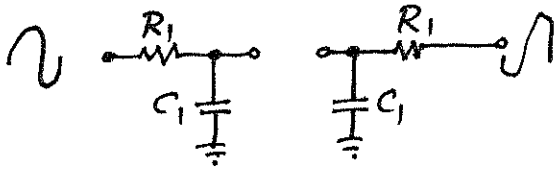
Since $g(V)$ is monotonic, $C_1(t)$ has the same period as the input and can be written as a Fourier series:

$$C_1(t) = C_{10} + C_{11}\cos(\omega_0 t + \phi_1) + C_{12}\cos(2\omega_0 t + \phi_2) + \cdots$$

(a) Replacing for C_1 in Eq. (1), we have

$$\text{Amplitude of Second Harmonic} = \frac{R_1 C_{11} \omega_0 V_0}{2}.$$

(b) $C_1(t)\big|_{left} = C_{10} + C_{11}\cos(\omega_0 t + \phi_1) + C_{12}\cos(2\omega_0 t + \phi_2) + \cdots$



$$C_1(t)\big|_{right} = C_{10} - C_{11}\cos(\omega_0 t + \phi_1) + C_{12}\cos(2\omega_0 t + \phi_2) + \cdots$$

$$V_{out,left} - V_{out,right} = 2V_0 \cos\omega_0 t + 2V_0 (\sin\omega_0 t)\left[R_1 \omega_0 C_{12}\cos(2\omega_0 t + \phi_2)\right]$$

$$\Rightarrow \text{Amplitude of Third Harmonic} = R_1 C_{12} \omega_0 V_0$$

Method II

$$C_1 = C_0\left(1 + \alpha_1 V_{out} + \alpha_2 V_{out}^2 + \cdots\right)$$

(a)
$$\approx C_0\left(1 + \alpha_1 V_0 \cos\omega_0 t + \alpha_2 V_0^2 \cos^2\omega_0 t + \cdots\right).$$

This is somewhat questionable because we have approximated V_{out} with $V_0 \cos\omega_0 t$ (no harmonics), but probably fine for small nonlinearities.

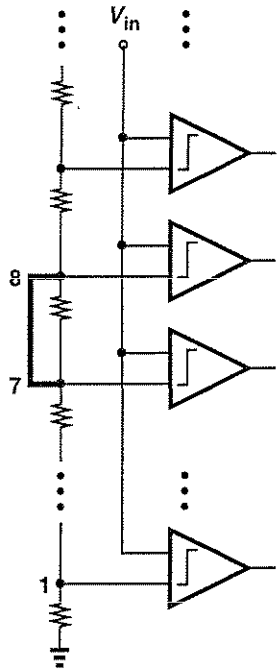
$$\Rightarrow \text{Amplitude of Second Harmonic} = \frac{R_1 \omega_0 \alpha_1 C_0}{2} V_0^2$$

(b)
$$\text{Amplitude of Third Harmonic} = \frac{R_1 \omega_0 \alpha_2 C_0}{2} V_0^3 .$$

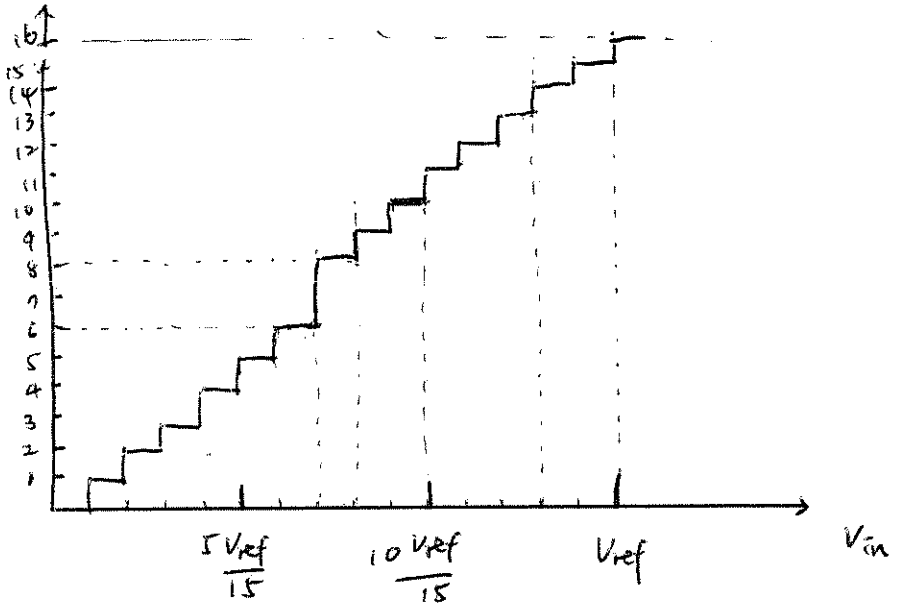
3. Consider the 4-bit flash ADC shown below, where taps number 7 and 8 of the ladder are accidentally shorted. Assume the system is otherwise ideal. (10)

(a) Sketch the input/output characteristic and show the critical parts.

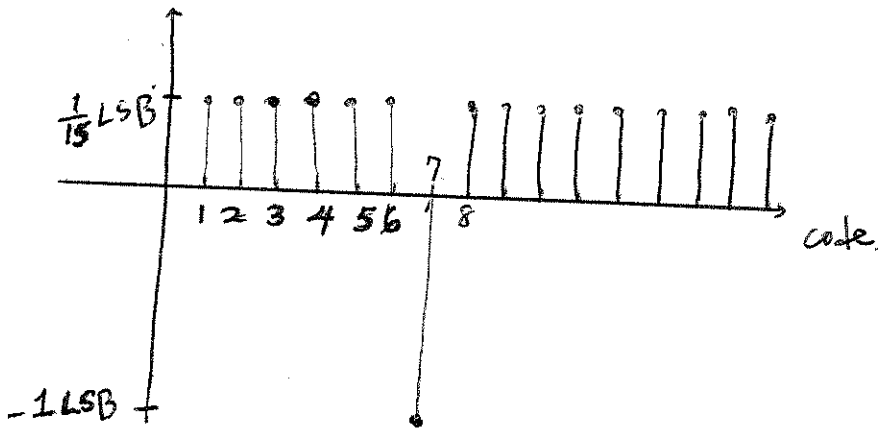
(b) Sketch the DNL profile of the ADC.



(a)



(b) DNL



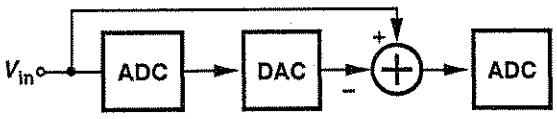
except code 7 is -1 LSB; all others' DNL equal to $\frac{1\text{ LSB}}{15}$

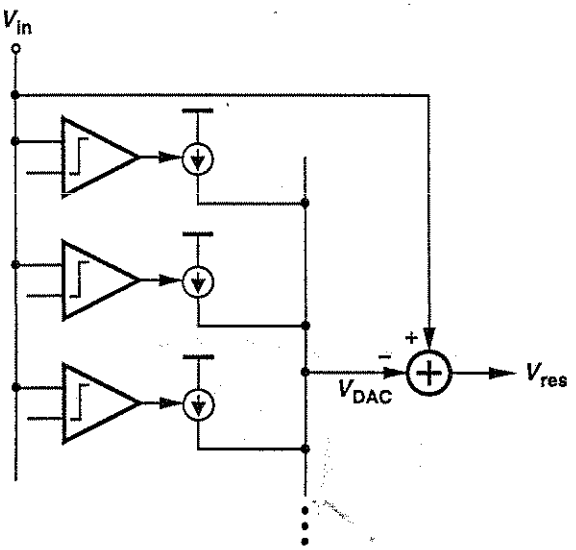
4. Consider the 10-bit two-step ADC studied in Homework 4, where each stage resolves 5 bits. Assume that the DAC employs a segmented current-steering array. Analyze the following three cases independently.

(a) Suppose the 15th comparator in the first flash stage is accidentally omitted. Construct the residue plot and the input/output characteristic.

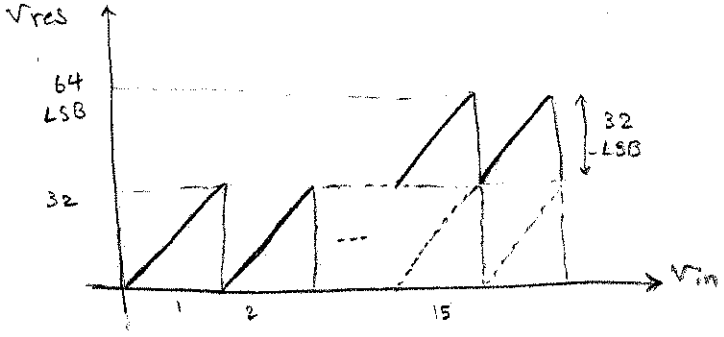
(b) Suppose the last current source in the DAC is accidentally omitted. Construct the residue plot and the input/output characteristic.

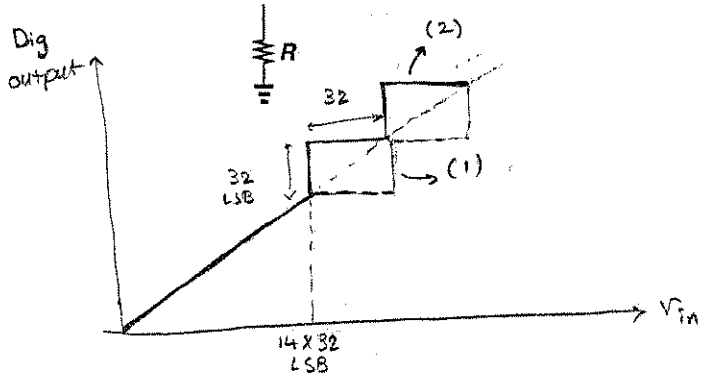
(c) Suppose the first current source in the DAC is accidentally omitted. Construct the residue plot and the input/output characteristic.



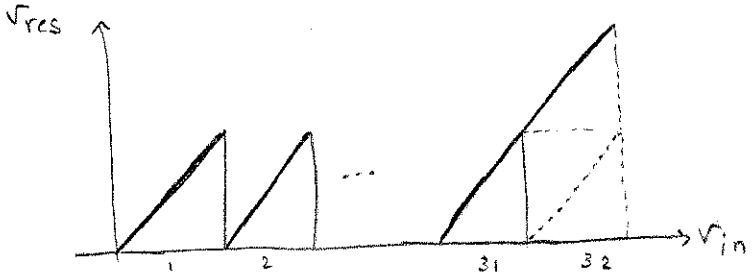


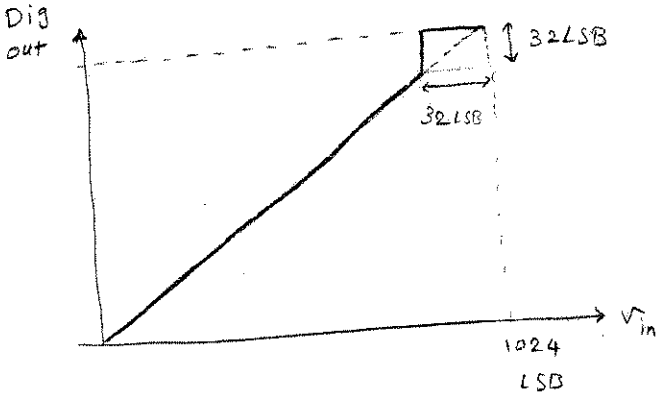
(a) for ADC in/out plot we can consider two cases depending on Thermometer to binary converter: either 15th coarse Step is missing → case (1)
or not → case (2)





(b)





(c)