

Homework #1

Due Mon., Jan. 11, 2010

1. An LNA with a relatively high input impedance exhibits a noise figure of NF_1 with respect to a source impedance of R_S . We tie a resistor of value R_S from the input of the LNA to (ac) ground so as to match the circuit to an antenna. [All noise figures in this problem are numeric (not logarithmic).]

- (a) Using Eq. (2.84), calculate the noise figure of the overall circuit with respect to a source impedance of R_S .
- (b) Repeat (a) but view the grounded resistor as R_P in Fig. 2.30(a) and use Friis' equation. Compare the results.

2. In this problem, we study the intermodulation behavior of a simple two-stage low-noise amplifier at 5.2 GHz. The model files can be found at <http://www.ee.ucla.edu/razavi/teaching.html> for Cadence and HSPICE. (They are called 215a.scs and 215a.sp, respectively.)

(a) Consider the common-gate circuit shown here, where M_2 represents a typical load capacitance for now. Assuming $\lambda = 0$, compute the width of M_1 such that $g_{m1} + g_{mb1} = (50 \Omega)^{-1}$.

(b) Use simulations to determine the value of L_1 for resonance at 5.2 GHz. The inductor must be modeled as shown, where R_P is chosen to give a Q of 4 at the frequency of interest and $C_P = 10$ fF for every nanohenry of inductance.

(c) Now find the input resistance (i.e., the real part of the input impedance) by simulations and explain why it is not equal to 50Ω . Adjust the width of M_1 to obtain a $50\text{-}\Omega$ input resistance again.

(d) Using the shortcut method, compute the IIP_3 and voltage gain of the circuit at 5.2 GHz.

(e) Determine the IIP_3 and voltage gain of the stage shown on the right at 5.2 GHz. The role and modeling of L_2 are similar to those of L_1 .

(f) Now remove M_2 from the first stage, place the two stages in a cascade, and find the overall voltage gain and IIP_3 . How closely do these results agree with those obtained from parts (d) and (e) and Eq. (2.46) in the text? (Make sure you include the *loaded* gain of the first stage in the equation.)

(g) Does the input resistance of the first stage change when the second stage is added? Why?

(h) Which stage limits the IIP_3 ?

