EE 215C HO#1

Winter 2010

Analysis and Design of RF Circuits and Systems

Instructor: Behzad Razavi
56-147D, Eng. IV
(310) 206-1633, razavi@ee.ucla.edu
Office Hours: MW, 10:30-12:00

Time: MW, 4:00-5:50 pm

Place: BL 5273

Use of laptops is prohibited during lectures (and exams).

Prerequisites: EE215A (Preferably with a grade of A- or higher)

Credit: 4 Units

Grading: Midterm 30%
Final 30%
Homeworks 20% (Late HW Policy: 25% deduction per day)
Final Project 20%

Course Textbook:


Reference Book:


Audit Policy: Individuals can audit if they do not collect the handouts.

Important Dates:

Mon. Jan. 11 HW#1 Due
Wed. Jan. 20 HW#2 Due
Mon. Feb. 1 HW#3 Due
Wed. Feb. 10 HW#4 Due
Mon. Feb. 15 Midterm Exam
Fri., March 12 Final Project Due
Mon. March 15, 8:00-11:00 am Final Exam
Outline

● Basic Concepts
  - Harmonic and Intermodulation Distortion, Third Intercept Point, Cascaded Stages
  - Intersymbol Interference and Nyquist Signaling
  - Random Processes and Noise, PDF, PSD, Noise Figure, Cascaded Stages
  - Sensitivity and Dynamic Range

● Communications Background
  - Analog and Digital Modulation, AM, FM, QPSK Family, FSK, GMSK
  - Bandwidth and Power Efficiency
  - Multiple Access Techniques (FDMA, TDMA, CDMA)
  - Wireless Standards (IS-54, GSM, DECT, IS-95)

● RF Transceiver Architectures
  - Heterodyne, Homodyne, and Image-Reject Receivers
  - Two-Step and Direct-Conversion Transmitters

● Low-Noise Amplifiers and Mixers
  - Bipolar and CMOS LNAs
  - Passive vs. Active Mixers
  - DSB and SSB Noise Figures
  - CMOS Mixers

● Oscillators
  - Basic LC Oscillator Topologies
  - Phase Noise
  - Phase Noise Mechanisms
  - CMOS VCOs
  - Quadrature Signal Generation

● Frequency Synthesizers
  - Phase-Locked Loops (Loop Dynamics, Building Blocks, Types I and II)
  - Phase-Locked Synthesizer Architectures (Integer-N, Fractional-N, Dual-Loop)
  - Direct Digital Synthesis
  - Frequency Dividers and Prescalers