


U-PAS

UCLA Pipelined ADC Simulator



Quick Start Guide

UCLA Pipelined ADC Simulator (UPAS) is a graphical user interface (GUI) based tool for analysis of pipelined ADC. Fig. 1 shows the architecture of the pipeline ADC that the simulator analyses. It consists of N stages followed by a 1-bit flash ADC that concurrently operate on N consecutive samples of the analog input. The architecture does not incorporate a sample-and-hold at the input of the ADC. Each stage digitizes its input, V_{in} , by means of a sub-ADC with a resolution of M bits (M is 1 or 1.5 bits in the current simulator), thereby producing a digital estimate of V_{in} . This estimate is then returned to the analog domain by a sub-digital-to-analog converter (sub-DAC), and subtracted from V_{in} . The resulting difference is then amplified by a factor of 2^M (i.e. 2 in the current simulator) and applied to the next stage for finer digitization.

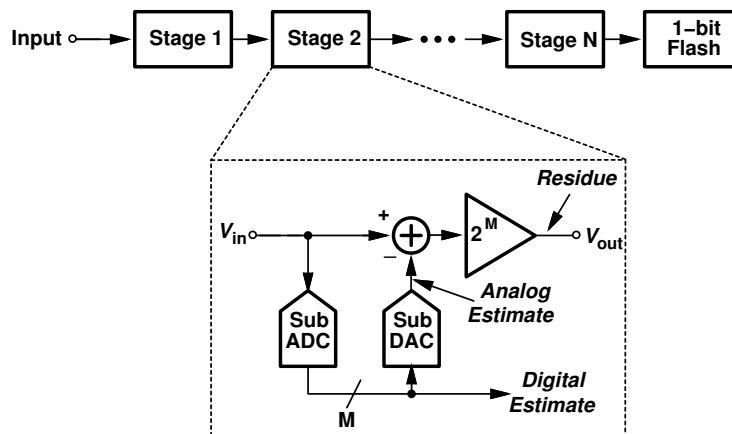


Fig. 1. Pipelined ADC architecture.

The tool captures the following imperfections that limit the performance of a pipelined ADC:

- finite open-loop gain of the op amp.
- nonlinearity of the op amp.
- capacitor mismatch.
- parasitic capacitance at the op amp input.
- slewing and linear settling of the op amp in the amplification mode.
- op amp offset.
- comparator offset.
- clock jitter.
- thermal noise.



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The tool currently simulates pipelined ADC having the following MDAC structures for each stage of the pipeline:

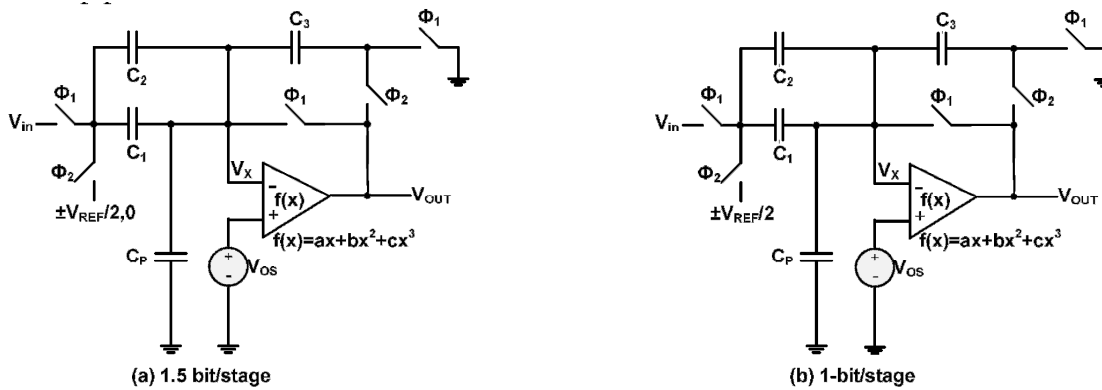


Fig. 2. Capacitor non-flip over architecture.

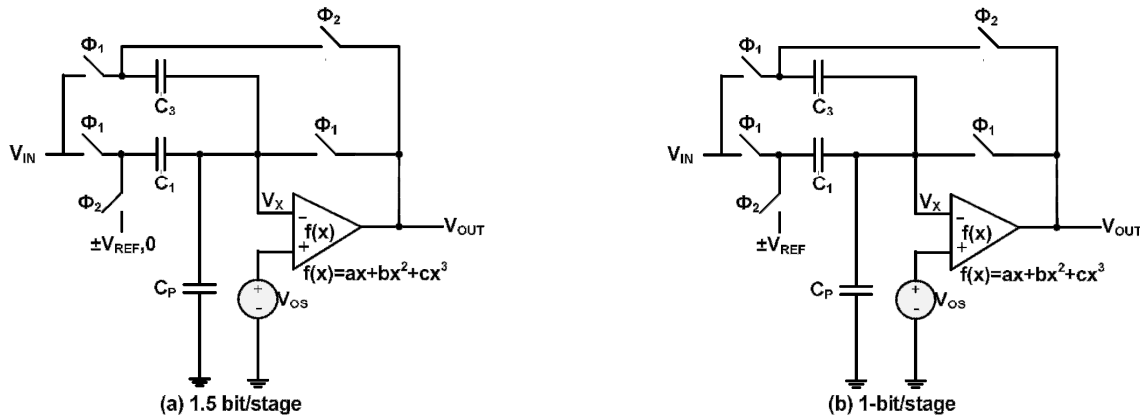


Fig. 3. Capacitor flip over architecture.

In the above MDAC structures the nominal values of the capacitors are such that $C_1=C_2=C_3$. The sampling capacitor $C_S=C_1+C_2$ in Fig. 1 and $C_S=C_1+C_3$ in Fig. 2.

ADC Parameters:

- Number of stages
- Signal Amplitude (P-P Diff) (V)
- Clock Frequency (MHz)
- Input Frequency (MHz)
- N-Point FFT
- RMS Clock Jitter (ps)
- Slewing Time (ns)
- Include Non-Idealities
- Number of stages in the pipeline (Maximum =16).
- Peak-Peak Input Differential Voltage to ADC (in Volts). (Used for computing the noise which is disabled)
- Sampling Frequency in MHz. (f_{clk})
- Frequency of the input signal in MHz. (f_{in})
- Number of points used to compute the FFT. (N_{FFT})
- Variance of the clock jitter in ps. (t_j)
- Time allocated for op amp slewing in ns.
- If checked the user can enter the various nonidealities.



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Stage Parameters:

- Non-Linear Op amp: The open loop input-output characteristic of the op amp is modeled as $f(x)=ax+bx^2+cx^3$.
 - a = Linear Part of the Amplifier Gain
 - b = 2nd order Term in the Amplifier Gain
 - c = 3rd order Term in the Amplifier Gain
 - G_m = Transconductance of the op amp. Used to compute the 1st order linear settling error.
- Capacitors (C_1 , C_2 and C_3) are in pF. The user can give the required values as dictated by matching requirements.
- Comparator offset in mV.
- Parasitic Capacitance in pF.
- Op amp Offset in mV.

Getting Various Plots:

After entering all the values the user needs to push the “**Simulate**” button to simulate the ADC and see the various plots.

- Residue Plot : The output of each stage of the ADC i.e. the residue of each stage can then be plotted.
- Plot(I/O) : To plot the input output characteristic of the ADC.
- FFT : The SNR can be computed by taking the FFT. The user can enter the number of points used to compute the FFT.
- DNL/INL : DNL/INL computed using the histogram of the codes generated from a sinusoid of frequency f_{in} . The number of vectors used to compute the DNL/INL is $8 \times N_{FFT}$. To speed up simulation time $N_{FFT} < 8192$ is recommended.

Zooming on the Plots:

- The user can zoom in on the plots by clicking on zoom button.

Calibration:

- Current version doesn't have the calibration algorithm selection enabled. However, clicking on any file in that window activates a very basic linear gain calibration algorithm which would lead to SNR improvement and better DNL/INL.

Thermal Noise Analysis:

The tool can compute the overall input referred thermal noise of a pipelined ADC. The tool offers thermal noise analysis for both single-stage and two stage op amp topologies. It requires the following parameters for a two stage op amp for noise analysis:

1. Op amp gain:
 - Gain of stage 1 (A_{v1})
 - Gain of stage 2 (A_{v2})



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2. Op amp transconductance
 - Transconductance of stage 1 (g_{m1})
 - Transconductance of stage 2 (g_{m2})
3. Current source noise factor
 - Ratio of the transconductance of current source of stage 1 and g_{m1} (n_1)
 - Ratio of the transconductance of current source of stage 2 and g_{m2} (n_2)
4. Compensation capacitance (C_C)
5. Parasitic capacitance at the output of stage 1 (C_{O1})
6. Parasitic capacitance at the output of stage 2 (C_{O2})
7. Temperature
8. Gamma (γ)

The noise analysis can be done by clicking the “**Noise Analysis**” button which pops up an additional window. The user can then enter the various parameters listed above to do the noise analysis. Fig. 4 illustrates an MDAC incorporating a two stage op amp with the various noise sources.

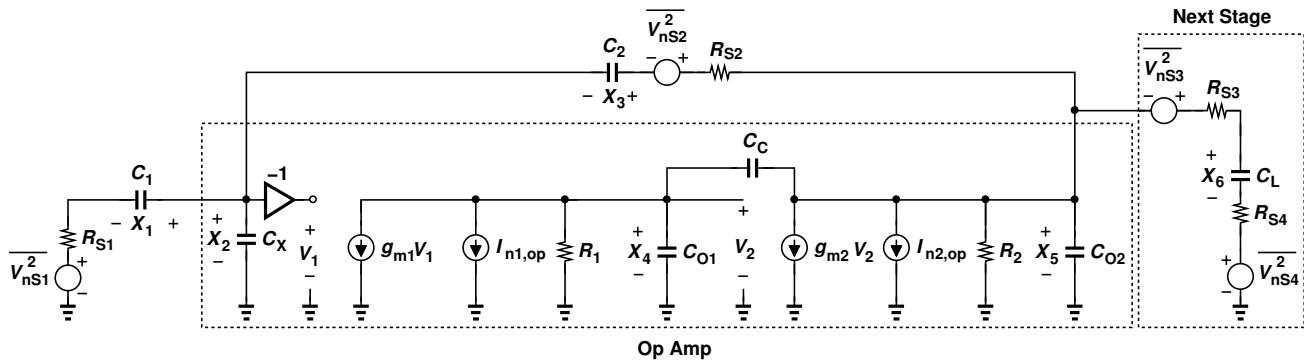


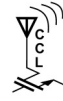
Fig. 4 MDAC incorporating a 2-stage op amp with all noise sources.

C_1 , C_2 , C_X , and C_L are obtained from the main window of the GUI. R_1 and R_2 are A_{v1}/g_{m1} and A_{v2}/g_{m2} respectively. The power spectral density of the noise current at the output of stage 1 and stage 2 of the op amp are $4kT\gamma(1+n_1)g_{m1}$ and $4kT\gamma(1+n_2)g_{m2}$ respectively.

If single stage op amp topology is chosen then the tool ignores the parameters A_{v2} , g_{m2} , n_2 , C_C , and C_{O2} . The user should make sure that the remaining parameters are accurate.

By clicking on “**Compute Noise**” for each of the stages the user can get the noise at the output of each MDAC and also the gain of the MDAC.

Clicking on “**Total Input Noise**” the user can obtain the total input referred noise of the pipelined ADC.



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NOTE: If the number of stages in the pipeline ADC is changed in the main window then the user should close the window for noise analysis and then click on the “**Noise Analysis**” button on the main window again to start the noise analysis.

How to get an accurate noise report?

In order to get an accurate estimate of the input referred noise the user should provide C_C , C_{O1} , C_{O2} , and C_X correctly.

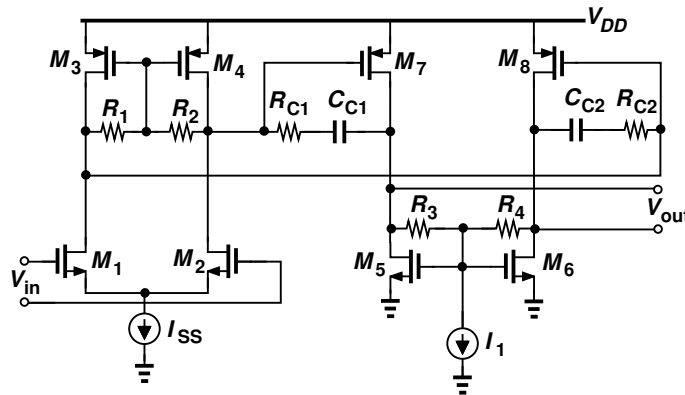


Fig. 5 Two stage op amp

Fig. 5 shows a simple two stage op amp. The various capacitances, C_C , C_{O1} , C_{O2} , and C_X are as follows:

- Compensation capacitance, $C_C = C_{C1} + C_{GD-M7}$
- Parasitic capacitance at the output of stage 1, $C_{O1} = C_{D-M1} + C_{D-M3} + C_{GS-M8}$.
- Parasitic capacitance at the output of stage 2, $C_{O2} = C_{D-M5} + C_{D-M7}$.
- Input capacitance, $C_X = C_{GS-M1}$
- For a fully differential op amp:
 - $C_{C1} = C_{C2}$
 - $C_{D-M1} = C_{D-M2}$
 - $C_{D-M3} = C_{D-M4}$
 - $C_{D-M7} = C_{D-M8}$
 - $C_{D-M5} = C_{D-M6}$
 - $C_{GS-M8} = C_{GS-M7}$
 - $C_{GS-M1} = C_{GS-M2}$

Bugs:

- Please report bugs to bsahoo@ee.ucla.edu. Please include all the steps that led to the bug so that it can be reproduced and fixed accordingly.