Yu-Lin Chao

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Profile

- thorough experience in IC fabrication (0.15-0.42 μm) and foundry environment.
- strong background in semiconductor devices, circuits and technology.
- capable of trouble shooting and project planing and executing.
- quick leaner with excellent communication skills.

Education

Ph.D. candidate, Department of Electrical Engineering, UCLA, Los Angeles, CA (2002-present, expected graduation date: Sept. 2007)
Research topic: "Germanium Channel Devices for Nanoscale CMOS Applications"
Major: Solid State Devices
Minor: Integrated Circuits and Systems

M.S., Department of Mechanical Engineering and Material Science, Duke University, Durham, NC (1996-Dec. 1998)
Thesis: "Low Temperature Wafer Bonding"
Majored in semiconductor materials and processing.

B.S., Department of Material Engineering and Science, National Tsing-Hua University, Hsin-Chu, Taiwan (1992-1996)
Majored in electronic materials, thin film processing, and solid state physics.

Experience

UCLA, Los Angeles, CA
Research Assistant, CMOS Lab, 10/02 to present
- Germanium on insulator (GeOI) fabrication using wafer bonding technique.
- Electrical characterizations of germanium MOSCAPs.
- Germanide/dopant study for germanium source/drain engineering.
- Bulk Ge and GeOI MOSFETs fabrication and characterization.

WaferTech L.L.C., Camas, WA
Backend Process Engineer, 5/99 to 8/02
- CMP group leader, in charge of new technology implementation, process control and improvement, budgeting and cost reduction.
- CVD/PVD production sustenance and trouble shooting.
- Yield analysis and enhancement. One major customer had normalized yield improvement over 50%.

Duke University, Durham, NC
Research Assistant, Wafer Bonding Lab., 1/97 to 12/98
- Improvement of Si/Si, SiO2/SiO2 bonding quality for various applications.
- Dissimilar materials bonding (Quartz/Si, InP/Si, GaAs/Si) and layer transfer by hydrogen-induced splitting technique.

Max-Planck Institute for Microstructure Physics, Germany
Research Assistant, Summer 1997
- Thermomechanical stress analysis of dissimilar materials bonding pairs.

Skill

Processing: cleaning (DNS, Ontrak, TEL), furnace processes, photolithography (Karl Suss, Leica E-beam), CMP (AMAT, IPEC, Logitech, Strausbaugh), RTA, CVD/PVD (p-5000, Centura, Endura, Producer, Plasmatherm, Sloan, CVC). dry etching (Oxford), wafer bonding (Karl Suss).
Characterization: material characterization (SEM/EDX, XRD, AFM), film thickness measurement (OP2600, NanoSpec, Sopra, ResMap), KLA, thin film stress gauge, semiconductor parameter analyzer HP4155B, 4284A, 4120B.
Software: SPICE, TSuprem, Athena, Verilog, Synopsys, Cadence, UNIX, Windows, Mac, Mathematica, Latex, HTML, BASIC.
Miscellaneous: FMEA, SPC, ACME, Poseidon

Honors

Marubun grant, International conference on Solid State Devices and Materials, 2004.
Research Assistantship, Dept. of Electrical Engineering, UCLA, (2002 to present)
Fellowship, Dept. of Mechanical Engineering and Material Science, Duke University (1996-1998)
Scholarship, the Chinese Metallurgy Academic Association (1995)
Scholarship, National Tsing-Hua University President Award, Taiwan (1995)
National Engineering Ethics Competition, First Prize, Taiwan (1996)

Publications

Journal Papers

- device performance

1. "Source/Drain Engineering for Parasitic Resistance Reduction for Ge p-MOSFETs", **Y.-L. Chao**, R. Scholz, J. C.-S. Woo, scheduled publication in Oct. 2007 in *IEEE Transactions on Electron Devices*.

- source/drain engineering in germanium

1. "Characterization of copper germanide as contact materials for advanced MOSFETs" **Y.-L. Chao**, Y. Xu, R. Scholz, J. C.-S. Woo, *IEEE Electron Device Letters*, Vol. 27, p. 549, (2006).
2. "Pre-Amorphization Implantation Assisted Boron Activation in Bulk Germanium and Germanium-on-Insultator", **Y.-L. Chao**, S. Prussin, R. Scholz, J. C-S. Woo, *Applied Physics Letters*, Vol. 87, p. 142102, (2005).

- wafer bonding

1. "Germanium-on-Insulators fabrication by wafer bonding and Smart-Cut technology", **Y.-L. Chao**, R. Scholz, M. Reiche, U. Gösele, J. C.-S. Woo, *Japn. J. Appl. Phys.*, Vol. 45, no. 11, p. 8565, (2006).
2. "Ammonium hydroxide effects on low temperature wafer bonding enhancement", **Y.-L. Chao**, Q.-Y. Tong, T.-H. Lee, M. Reiche, R. Scholz, J. C.-S. Woo, U. Gösele, vol. 8, *Electrochemical and Solid State Letters*, 2005, G74-G77.
3. "Low temperature InP layer transfer", Q.-Y. Tong, **Y.-L. Chao**, L.J. Huang, U. Gösele, *Electronics Letters*, vol. 35, no. 4, 18 Feb. 1999, p.341-2.
3. "Si and SiC layer transfer by high temperature hydrogen implantation and low temperature layer splitting", Q.-Y. Tong, T.-H. Lee, L.J. Huang, **Y.-L. Chao**, U. Gösele, *Electronics Letters*, vol. 34, no. 4, 19 Feb. 1998, p. 407-8.
4. "A "Smarter-cut" approach to low temperature silicon layer transfer", Q.-Y. Tong, R. Scholz, U. Gösele, T.-H. Lee, L.J. Huang, **Y.-L. Chao**, T.Y. Tan, *Applied Physics Letters*, 72 (1), 5 January 1998, p.49-51.

Conference Papers

- device performance

1. "Reduction of Parasitic Resistance of Self-Aligned Copper Germanide for Gemanium p-MOSFETs", **Y.-L. Chao**, J. C.-S. Woo, *Extended Abstract of the 2006 International Conference on Solid State Devices and Materials*, 2006.

- gate stack integration

1. "Gate stack integration of germanium oxynitride for germanium MOSFETs", **Y.-L. Chao**, R. Scholz, J. C.-S. Woo, *Extended Abstract of the 2005 International Conference on Solid State Devices and Materials*, p. 516, 2005.

- source/drain engineering in germanium

1. "Dopant activation in bulk germanium and germanium-on-insulator", **Y.-L. Chao**, S. Prussin, R. Scholz, J. C.-S. Woo, Mat. Res. Soc. Symp. Proc. , 2004 Materials Research Society.

- wafer bonding

1. "Fabrication and characteristics of germanium-on-insulators", **Y.-L. Chao**, R. Scholz, M. Reiche, U. Gösele, J. C.-S. Woo, *Extended Abstract of the 2004 International Conference on Solid State Devices and Materials*, p. 224, 2004.
2. "Thermomechanical stress in silicon on quartz wafer bonding and Smart Cut® process", **Y.-L. Chao**, Q.-Y. Tong, U. Gösele, Mat. Res. Soc. Symp. Proc. Vol. 681E, 2001 Materials Research Society, I5.10.1.
3. "Semiconductor layer transfer by anodic wafer bonding", T.-H. Lee, Q.-Y. Tong, **Y.-L. Chao**, L.J. Huang, U. Gösele, *1997 IEEE International SOI Conference Proceedings*, IEEE, 1997, p.40-1.
4. "Silicon on quartz by a smarter cut process", T.-H. Lee, Q.-Y. Tong, **Y.-L. Chao**, L.J. Huang, U. Gösele, *Proceedings of the Eighth International Symposium on Silicon-on-Insulator Technology and Devices*, Electrochemical Society, 1997, p.27-32.

Languages Fluent in English, Mandarin.
Proficiency Fair in German, Japanese.

Activities

Pipe organ study, mentors including Prof. Parkins at Duke University and Prof. Terry at University of Washington
Assistant Organist, First Christian Church, Portland, OR (Aug. 2002)
President, The Strings Club, National Tsing-Hua University (1994)
Chief Editor, The Piano Club Yearly Publications, National Tsing-Hua University (1993)
Chief Editor, "Aurora", periodicals in poems, Taipei Municipal First Girls' High School (1990)
Member of Honor Guards, Taipei Municipal First Girls' High School (1990 to 1992)