UCLA ENGINEERING
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Electrical Engineering Department

Ph.D. Defense

Approaching Capacity at Short Blocklengths with Feedback and Low-Density Parity-Check Coding for Flash Memory

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Engr. IV Bldg., 67-124, Faraday Room

Abstract: This work primarily focuses on two branches of error control coding for data communications and storage. The first area of investigation explores the benefits of feedback with incremental redundancy in communication systems. Using carefully designed adaptive non-binary low-density parity-check (LDPC) codes, over 90% of channel capacity is achieved for average blocklengths of 150-450 bits. Without feedback, much longer blocklengths on the order of 10,000 symbols would be required to achieve a similar performance.

In feedback systems where the number of incremental transmissions is limited, selecting the optimum length for each message is crucial in maximizing the rate. However, the exhaustive-search approach to find the optimum size of each incremental transmission is computationally prohibitive. In this work, this optimization problem is efficiently solved by closely approximating the distribution describing the smallest blocklength of successful decoding using the reciprocal-Gaussian probability density function. Furthermore, the sequential differential optimization (SDO) algorithm with linear complexity is proposed that gives the same results as the exponentially complex exhaustive search.

The second track of this work involves the study of binary and non-binary LDPC codes designed for Flash memory. The communication channel associated with Flash memory provides only a single bit of information about the charge level stored in the floating gate with each read. In this work, the coding gain from multiple reads of the same Flash memory cell is analyzed. LDPC codes are optimized for various quantization levels used in Flash memory and the trade-off in LDPC code design is characterized when decoding is performed with multiple precision levels.

Biography: Kasra Vakilinia is a Ph.D. candidate in Electrical Engineering Department at the University of California, Los Angeles (UCLA). He is a member of the UCLA Communication Systems Laboratory (CSL) and UCLA Center on Development of Emerging Storage Systems (CoDESS). His research interests include coding theory, information theory, flash memory storage systems, and communications systems. He is also a member of IEEE and the IEEE Information Theory society.

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