Flash Channel Estimation for Dynamic Voltage Allocation

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Channel Noise Model

- We model the NAND flash memory cell data storage process as [1]

$$y = x + n_p + n_w + n_r$$

x : intended programmed state threshold voltage

y : sensed programmed state threshold voltage

n_p : programming noise

n_w : wear-out noise

n_r : retention noise

[1] Chen, Tsung-Yi; Williamson, Adam R.; Wesel, Richard D., "Increasing flash memory lifetime by dynamic voltage allocation for constant mutual information," Information Theory and Applications Workshop (ITA), 2014 , vol., no., pp.1,5, 9-14 Feb. 2014

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Programming Noise (n_p)

- The uncertainty of the programmed threshold voltage immediately after program operation can be modeled by a Gaussian random variable.
- The variance of the programmed threshold voltage is larger when left in the erased state than when actively programmed [2, 3].

$$f(n_p) = \begin{cases} N(0,\sigma_e^2) & \text{if } x = 0 \\ N(0,\sigma_p^2) & \text{if } x > 0 \end{cases} \quad \text{where } \sigma_e > \sigma_p$$

[2] K. Takeuchi, T. Tanaka, and H. Nakamura. A double-level-Vth select gate array architecture for multilevel NAND flash memories. IEEE Journal on Solid-State Circuits, 31(4):602–609, Apr. 1996.
[3] C.M. Compagnoni, A.S. Spinelli, R. Gusmeroli, A.L. Lacaita, S. Beltrami, A. Ghetti, and A. Visconti. First evidence for injection statistics accuracy limitations in NAND Flash constant-current Fowler-Nordheim programming. In Proc. of IEEE International Electron Devices Meeting, pages 165–168, 2007.

Wear-out Noise (n_w)

- Wear-out induces P/E-cycle-dependent threshold voltage shift as a result of bulk oxide and oxide interface traps generation and electron trapping/de-trapping during P/E cycling [4, 5, 6, 7].
- Trap behavior is modeled as random telegraph noise (RTN). This causes the distribution of measured thresholds features exponential tails [8].
- In some devices, the positive-shift tail is more significant than the negative-shift one, so we use an exponential distribution to model wear-out noise.

$$f(n_w) = \begin{cases} \frac{1}{\lambda} e^{-\frac{n_w}{\lambda}} & n_w \geq 0 \\ 0 & n_w < 0 \end{cases}$$

[4] D. Wellekens, J. Van Houdt, L. Faraone, G. Groeseneken, HE Maes, and L. IMEC. Write/erase degradation in source side injection flash EEPROM's: Characterization techniques and wearout mechanisms. IEEE Transactions on Electron Devices, 42(11):1992–1998, 1995.
[5] P. Olivo, B. Ricco, and E. Sangiorgi. High Field Induced Voltage Dependent Oxide Charge. Applied Physics Letter, 48:1135–1137, 1986.
[6] S. Yamada, Y. Hiura, T. Yamane, K. Amemiya, Y. Ohshima, and K. Yoshikawa. Degradation mechanism of flash EEPROM programming after program/erase cycles. In Proc. of International Electron Devices Meeting (IEDM), pages 23–26, 1993.
[7] P. Cappelletti, R. Bez, D. Cantarelli, and L. Fratin. Failure mechanisms of flash cell in program/erase cycling. In Proc. of International Electron Devices Meeting (IEDM), pages 291–294, 1994.
[8] C.M. Compagnoni, M. Ghidotti, A.L. Lacaita, A.S. Spinelli, and A. Visconti. Random telegraph noise effect on the programmed threshold-voltage distribution of flash memories. IEEE Electron Device Letters, 30(9), 2009.

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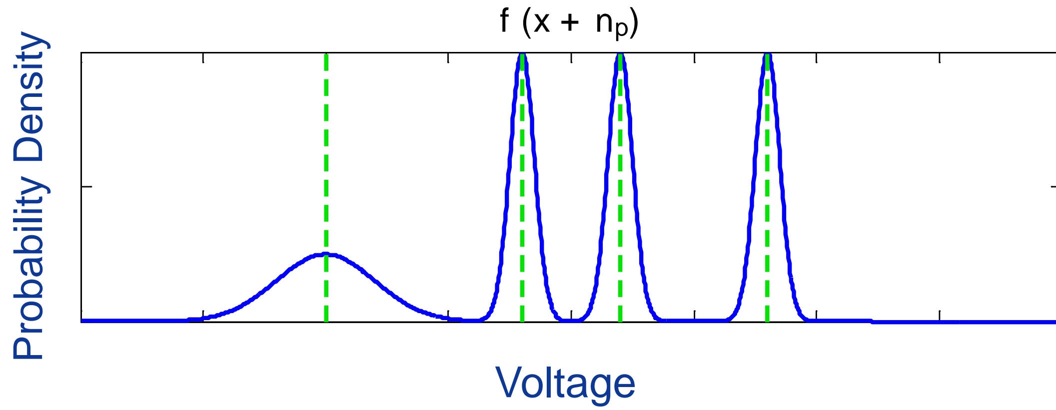
Retention Noise (n_r)

- Retention loss is the reduction of programmed threshold voltage over time caused primarily by electron de-trapping [9, 10].
- Retention noise n_r is modeled as a Gaussian distribution $N(\mu_r, \sigma_r^2)$ where the mean and variance are depending on time and number of traps.
- De-trapping scales approximately with the logarithm of post-cycling retention time and the number of traps before the post-cycling retention process [10].

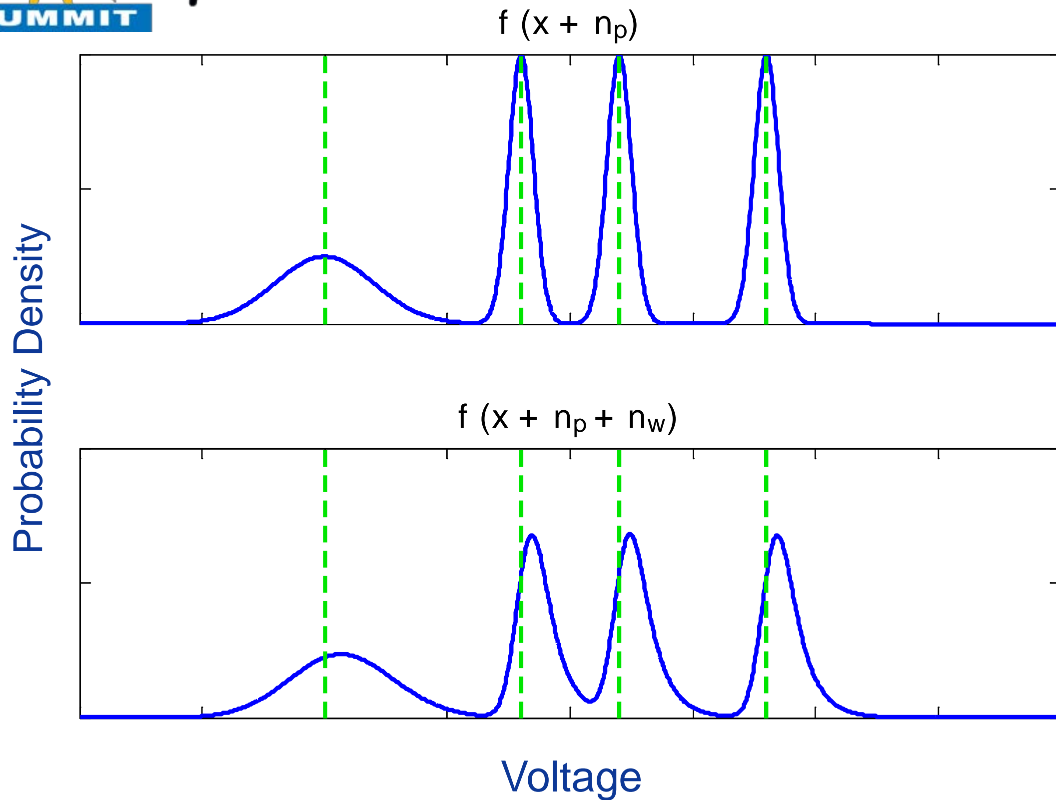
[9] J.D. Lee, J.H. Choi, D. Park, and K. Kim. Data retention characteristics of sub-100 nm NAND flash memory cells. IEEE Electron Device Letters, 24(12):748–750, 2003.
[10] N. Mielke, H.P. Belgal, A. Fazio, Q. Meng, and N. Righos. Recovery Effects in the Distributed Cycling of Flash Memories. In Proc. of IEEE International Reliability Physics Symposium, pages 29–35, 2006.

Sample PDF



Programming Noise Only

Sample PDF



Programming Noise Only

Programming and Wear-out Noise

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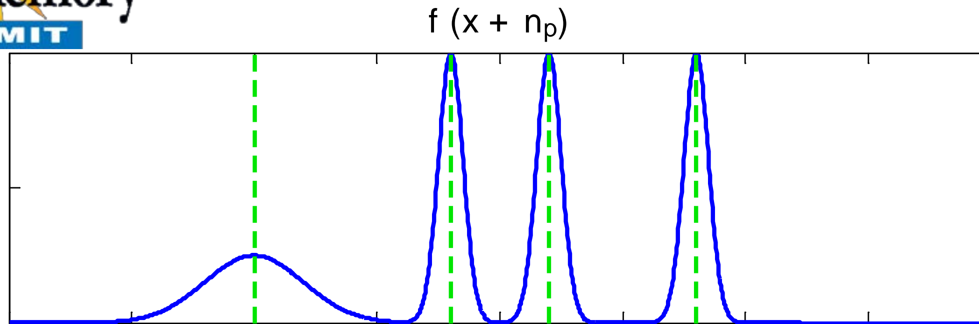

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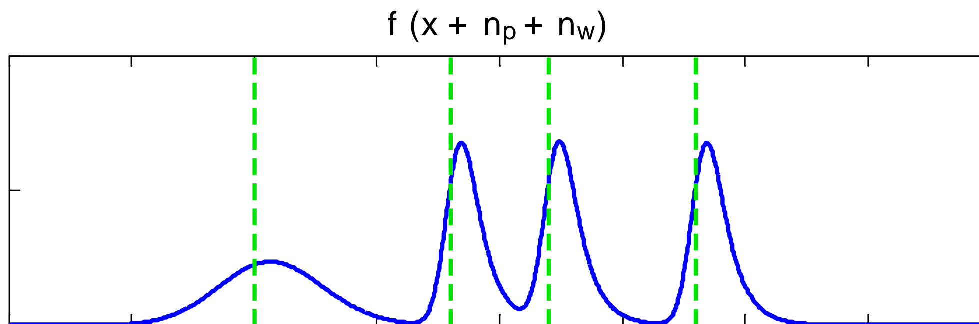
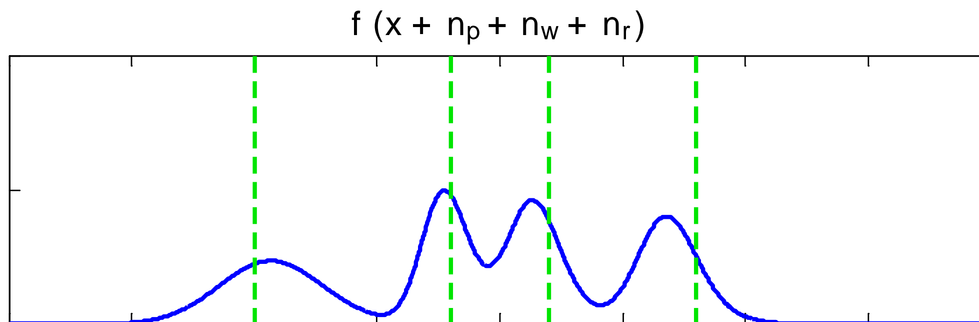


Programming and Wear-out Noise



Programming, Wear-out and Retention Noise

Probability Density

Voltage

Replace PE with *Vacc*

- Channel degradation is usually modeled as a function of the number of program/erase (P/E) cycles.
- The charge passing through dielectrics actually causes the degradation [11].
- We use accumulated voltage *Vacc* as a more precise metric of wear-out instead of P/E cycles. *Vacc* indicates the amount of charge passing through the dielectrics since the first write.

[11] W.D. Brown, J.E. Brewer. Nonvolatile Semiconductor Memory Technology, page 130

Normalized Accumulated Voltage

$$V_{acc} = \sum_{j=1}^{N} \left(V_p^{(j)} - V_e \right)$$

- V_{acc} : accumulated voltage over N P/E cycles,
- $V_p^{(j)}$: programmed threshold voltage of the jth P/E cycle
- V_e : threshold voltage of the erased state
- $V_{\max}$: the maximum of $V_p^{(j)} - V_e, \forall j$

The normalized accumulated voltage is $V_{acc} / V_{\max}$.

When using fixed voltage levels, $V_{acc} / V_{\max} \approx \#$ of PE Cycles.

Parameter Degradation Model

- Degradation Model
  - Wear-out noise:

$$\lambda = C_w + A_w \cdot \left(\frac{V_{acc}}{V_{\max}}\right)^{0.62}$$

  - Retention noise:

$$\mu_r = -x \cdot \ln\left(1 + \frac{t}{t_0}\right) \cdot \left[A_r \cdot \left(\frac{V_{acc}}{V_{\max}}\right)^{0.62} + B_r \cdot \left(\frac{V_{acc}}{V_{\max}}\right)^{0.3}\right]$$

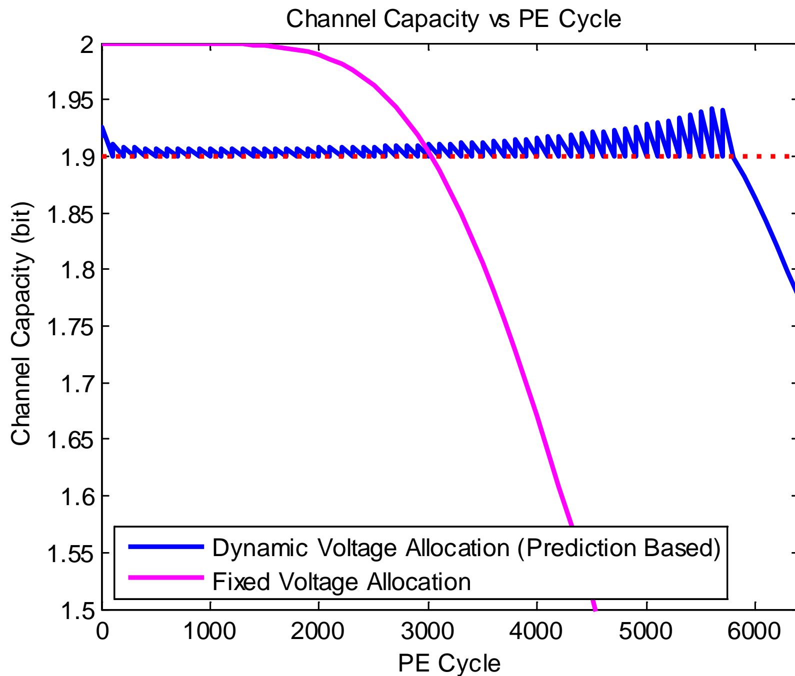
$$\sigma_r^2 = 0.1x \cdot \ln\left(1 + \frac{t}{t_0}\right) \cdot \left[A_r \cdot \left(\frac{V_{acc}}{V_{\max}}\right)^{0.62} + B_r \cdot \left(\frac{V_{acc}}{V_{\max}}\right)^{0.3}\right]^2$$

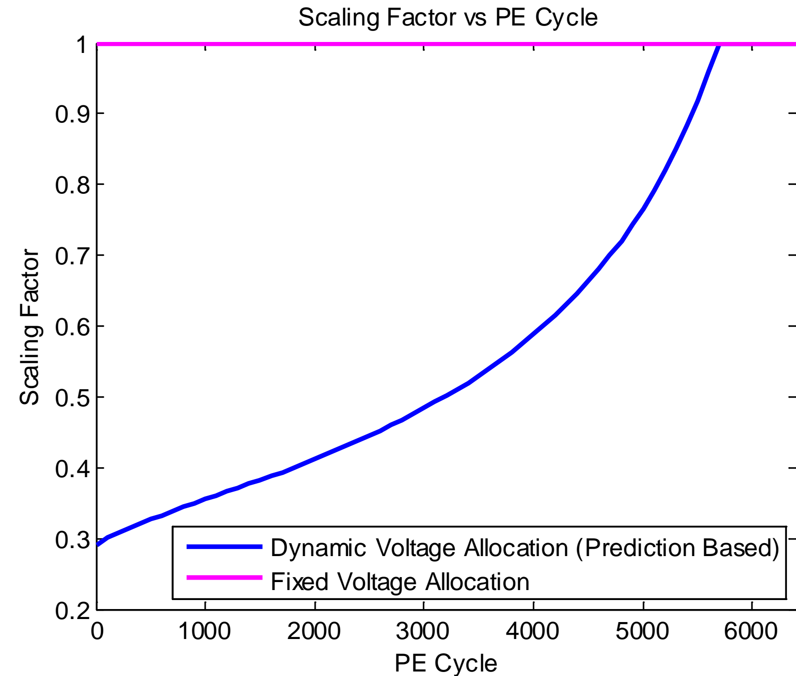
Dynamic Voltage Allocation

- Fixed threshold voltage allocation induces same amount of wear-out to Flash device in each P/E cycle.
- Dynamic Voltage Allocation can reduce unnecessary wear-out, and thus increase lifetime by using lower threshold voltage for early writes [1].
- The threshold voltages can be gradually increased as needed to combat channel degradation [1].
- The optimize target is to maintain a minimum channel capacity as long as possible.

[1] Chen, Tsung-Yi; Williamson, Adam R.; Wesel, Richard D., "Increasing flash memory lifetime by dynamic voltage allocation for constant mutual information," Information Theory and Applications Workshop (ITA), 2014 , vol., no., pp.1,5, 9-14 Feb. 2014

Theoretical DVA Demonstration





- Dynamic Voltage Allocation (DVA) on MLC based on the perfect prediction of future channel condition can extend the block's lifetime by 93%.

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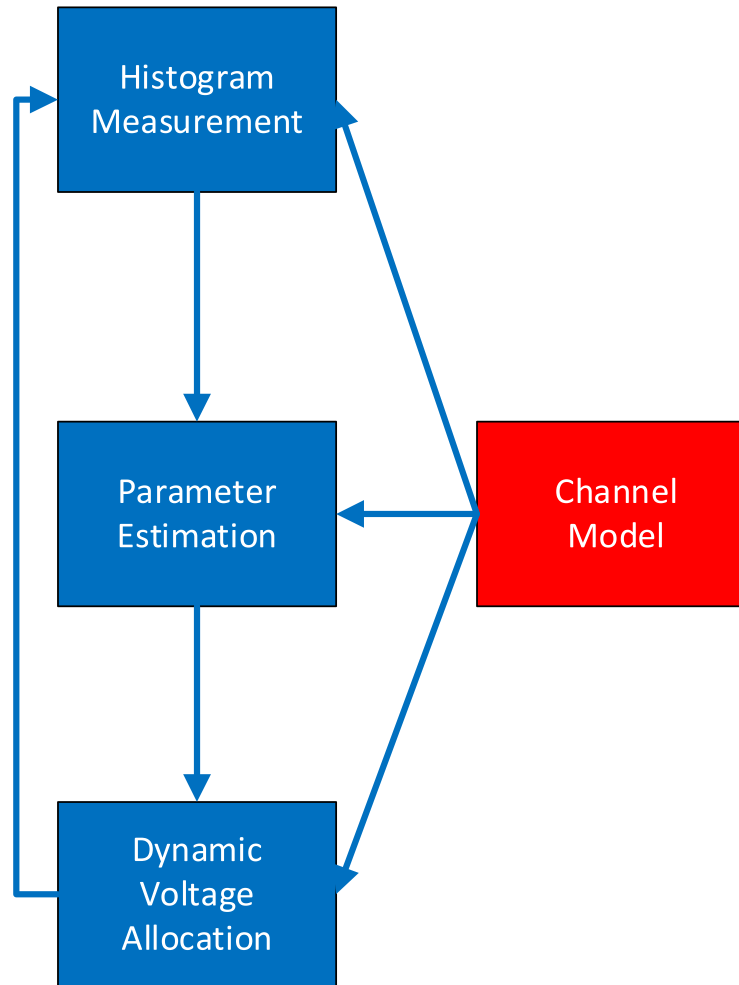
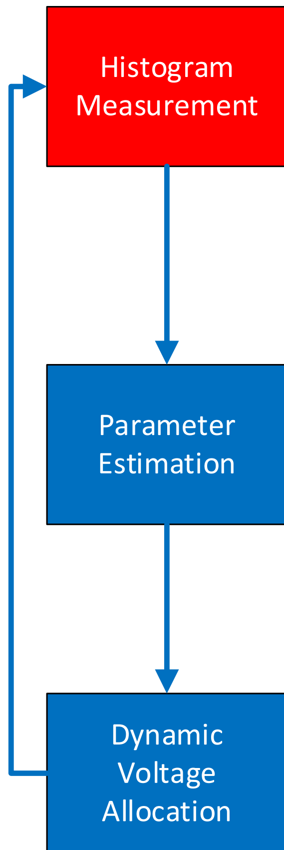
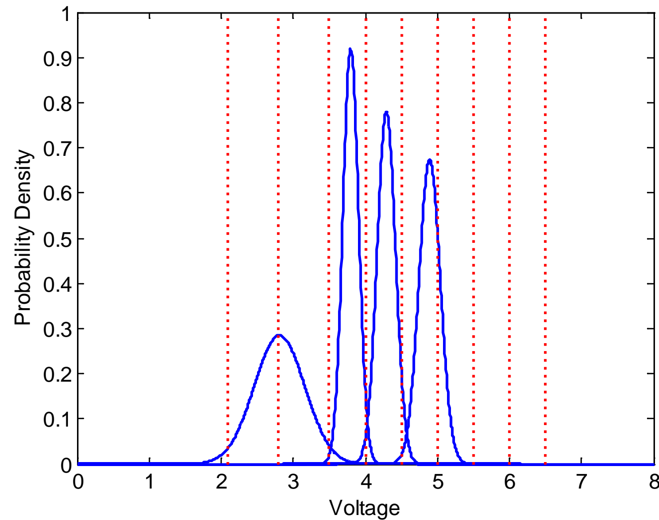
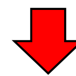
Practical DVA using Histogram-based Channel Estimation

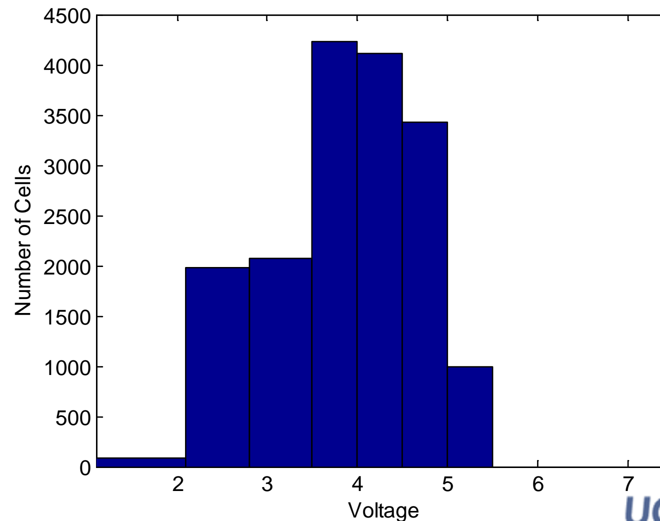


Histogram Measurement



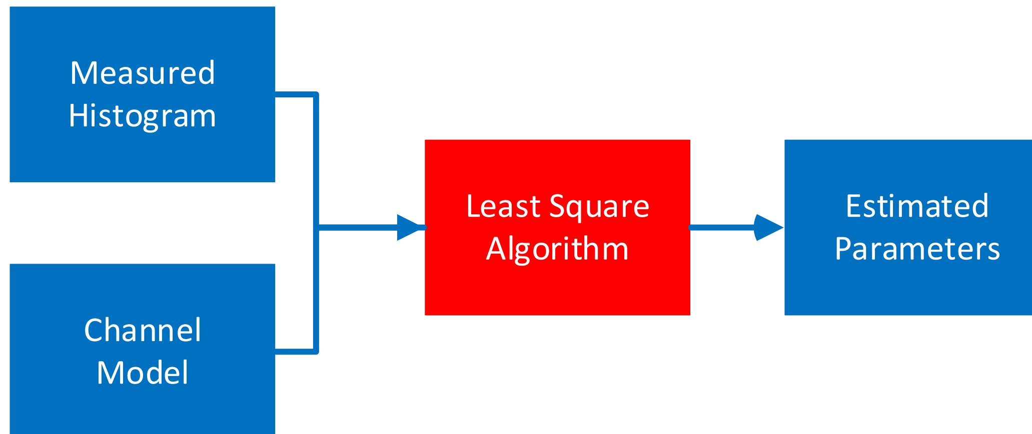






Channel Parameter Estimation

- Channel parameters can be estimated from measured histograms [12].
- Channel parameter estimation workflow:



[12] Dong-hwan Lee; Wonyong Sung, "Estimation of NAND Flash Memory Threshold Voltage Distribution for Optimum Soft-Decision Error Correction," Signal Processing, IEEE Transactions on , vol.61, no.2, pp.440,449, Jan.15, 2013

Parameter Vector

- Parameter Vector

  - $\boldsymbol{\alpha} = [\lambda, \sigma_{\text{programming}}, \sigma_{\text{erase}}, \sigma_{\text{retention}}, \mu_{\text{retention}}]$

  - We actually estimate $[\lambda, \sigma_p, \sigma_e, m_r, n_r]$, where

$$\mu_{\text{retention}} = -x \cdot n_r$$
$$\sigma^2_{\text{retention}} = x \cdot m_r^2 \ .$$

Estimation Objective Function

- Estimation Objective Function is the squared Euclidean distance between predicted histogram and measured histogram

$$C_M = \sum_{i=0}^{M-1} \left(\frac{\hat{N}_{\text{bin,i}} - N_{\text{bin,i}}}{N} \right)^2$$

N : total number of cells in a page

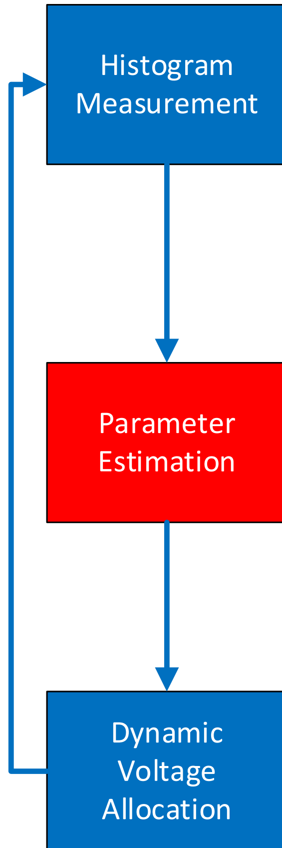
$N_{\text{bin,i}}$: total number of cells in ith bin of measured histogram

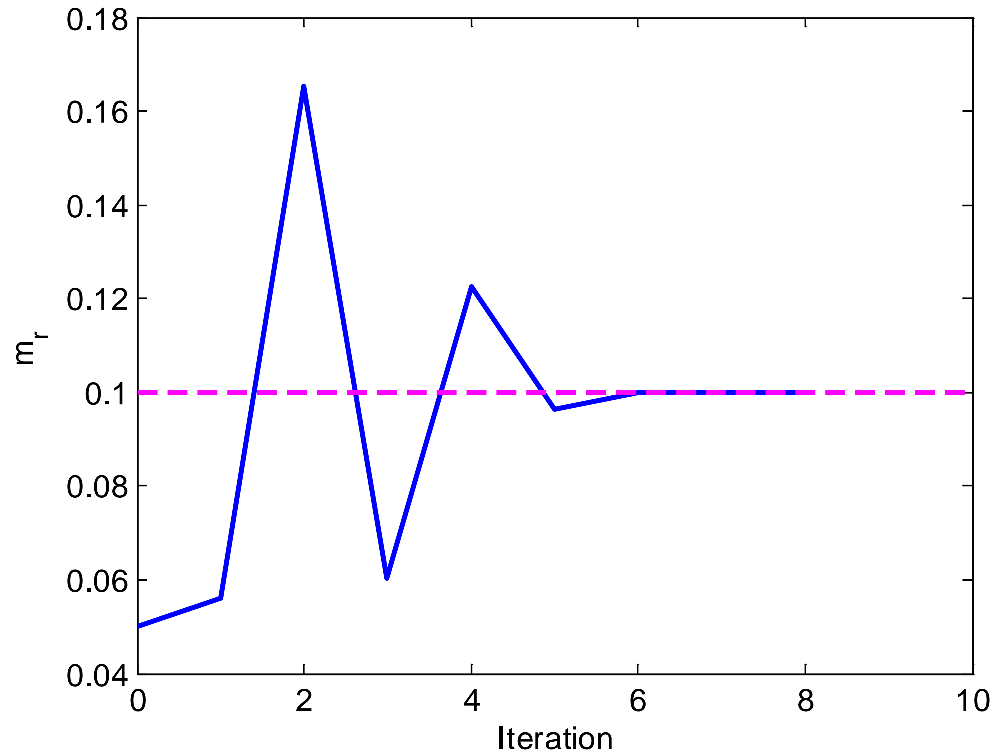
$\hat{N}_{\text{bin,i}}$: total number of cells in ith bin by estimation

M : total number of bins

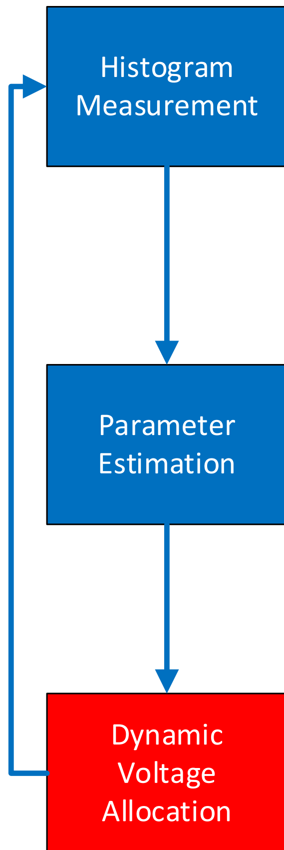
Parameter Estimation

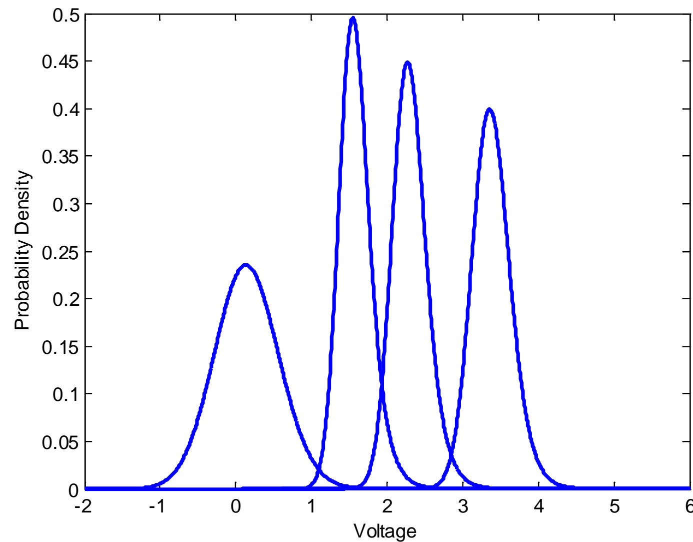
$$\boldsymbol{\alpha} = [\lambda, \sigma_p, \sigma_e, m_r, n_r] \Rightarrow [0.0500, 0.1997, 0.6000, 0.1002, -0.1000]$$

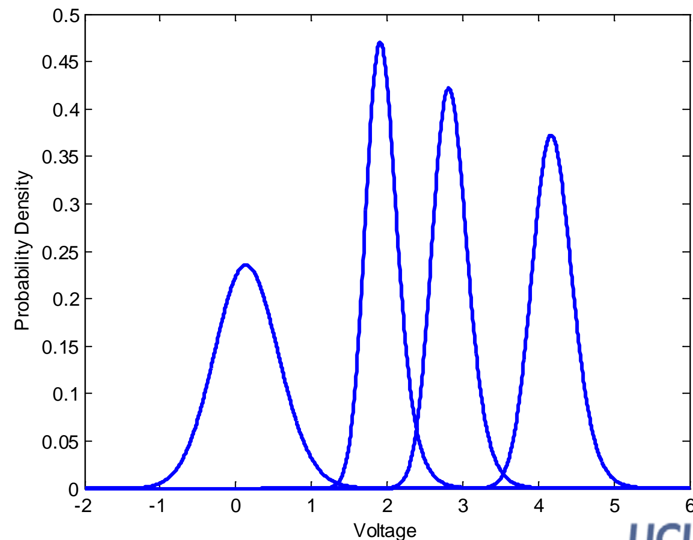




Voltage Levels Adapted to Degraded Channel



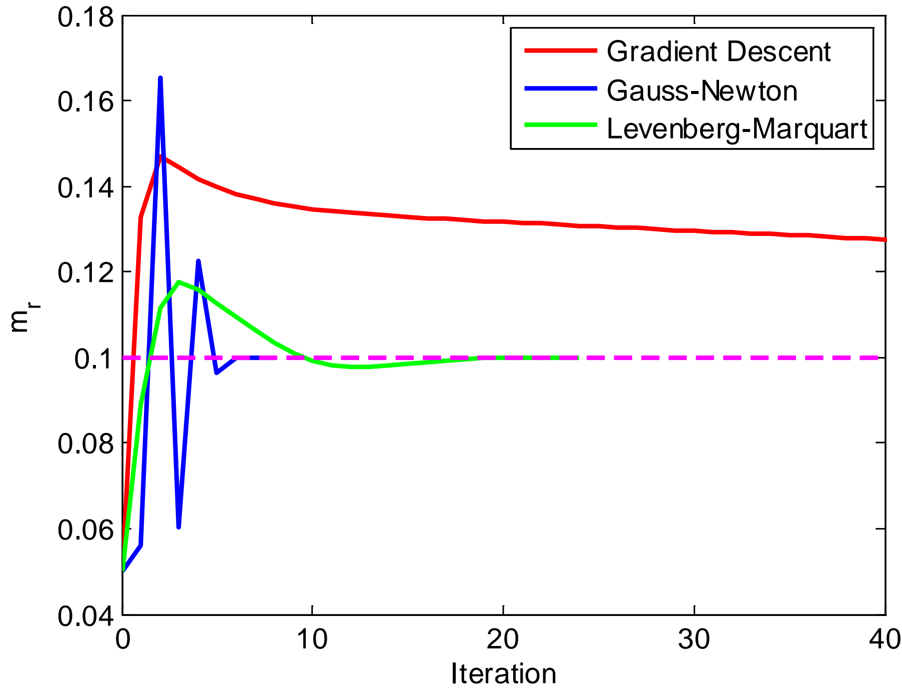


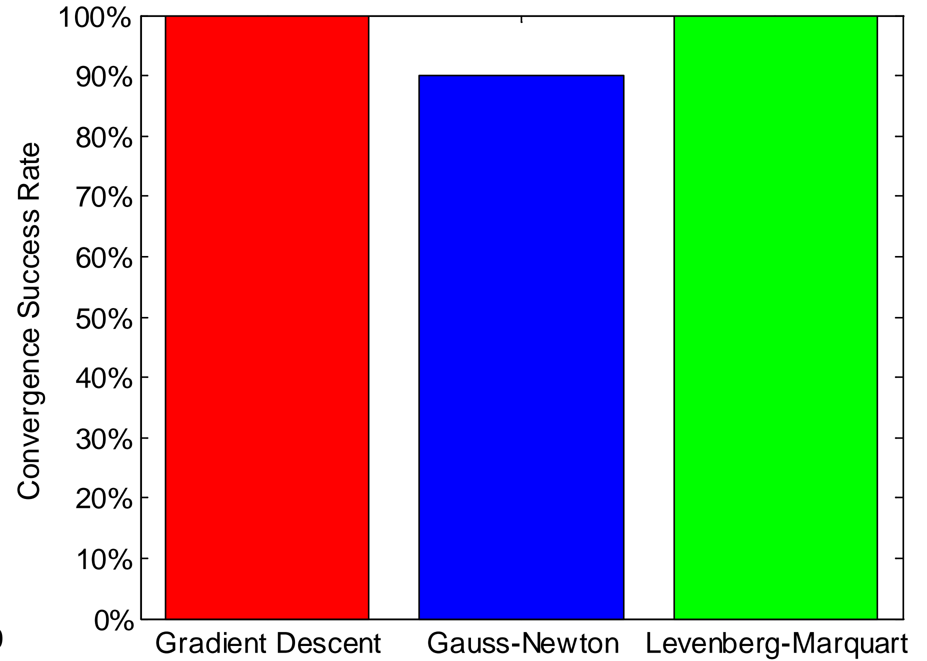


More about Least Square Algorithms

- Objective
  - Minimize the cost function.
- Algorithm 1 – Gradient Descent
  - Follow the descending gradient with a fixed step size.
- Algorithm 2 – Gauss–Newton Algorithm
  - Take each step based on quadratic approximation at current point.
- Algorithm 3 – Levenberg–Marquardt Algorithm
  - Rotate Gauss-Newton increment vector toward the direction of descending gradient.

Least Square Algorithm Comparison





Convergence Speed

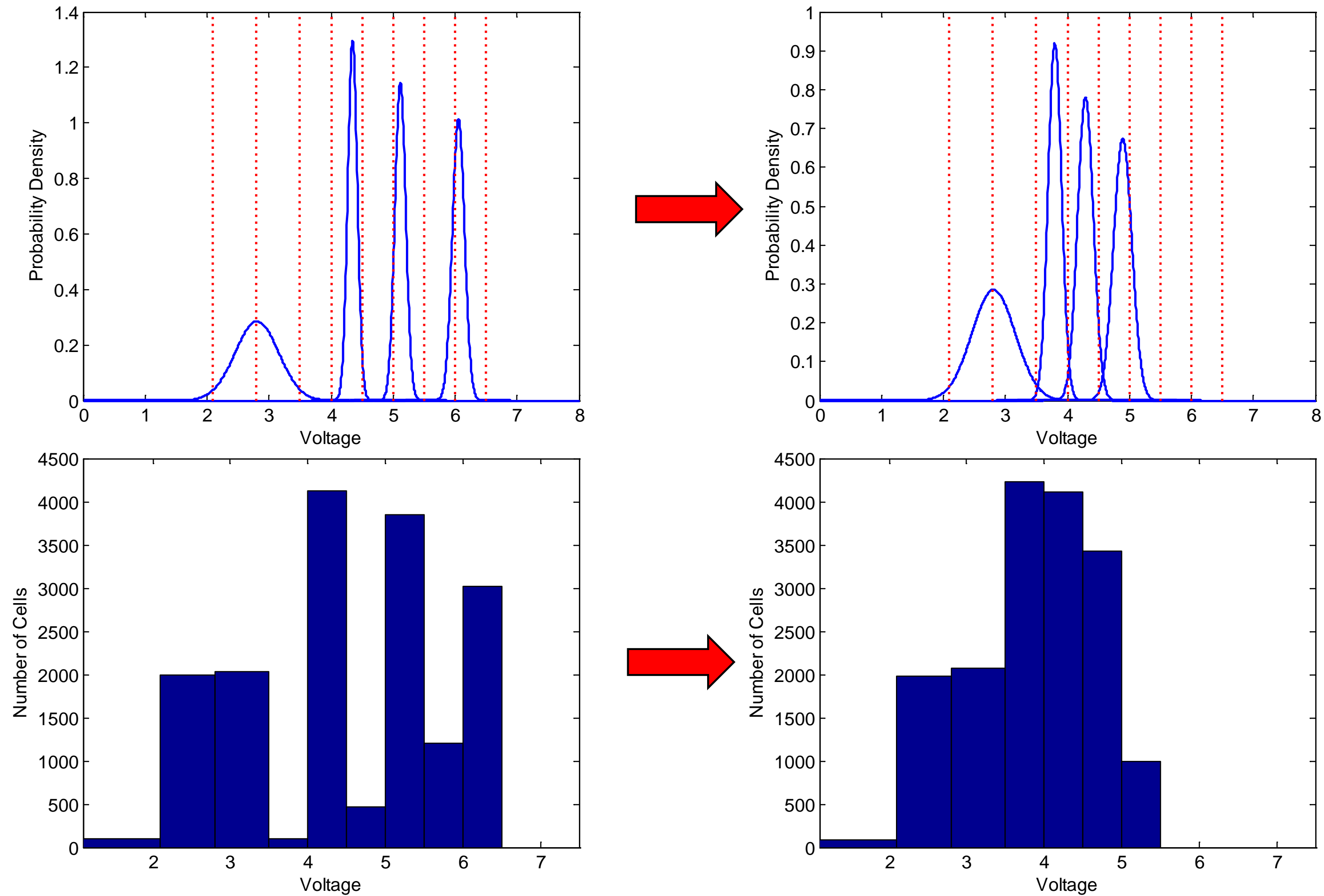
Convergence Success Rate

Histogram Types

- Equal Interval Histogram [12]
  - Not actually equal. Bins covering erased state distribution can be slightly wider.
- Maximum Mutual Information (MMI) Histogram [13]
- Equal Probability Histogram
  - Each bin has the same number of cells.

[12] Dong-hwan Lee; Wonyong Sung, "Estimation of NAND Flash Memory Threshold Voltage Distribution for Optimum Soft-Decision Error Correction," Signal Processing, IEEE Transactions on , vol.61, no.2, pp.440,449, Jan.15, 2013
[13] J. Wang, K. Vakilinia, T.-Y. Chen, T. Courtade, G. Dong, T. Zhang,H. Shankar, and R. Wesel, “Enhanced precision through multiple reads for LDPC decoding in flash memories,” Selected Areas in Communications, IEEE Journal on, vol. 32, no. 5, pp. 880–891, May 2014

Equal Interval Histogram Does not Adapt Well to Retention Loss.



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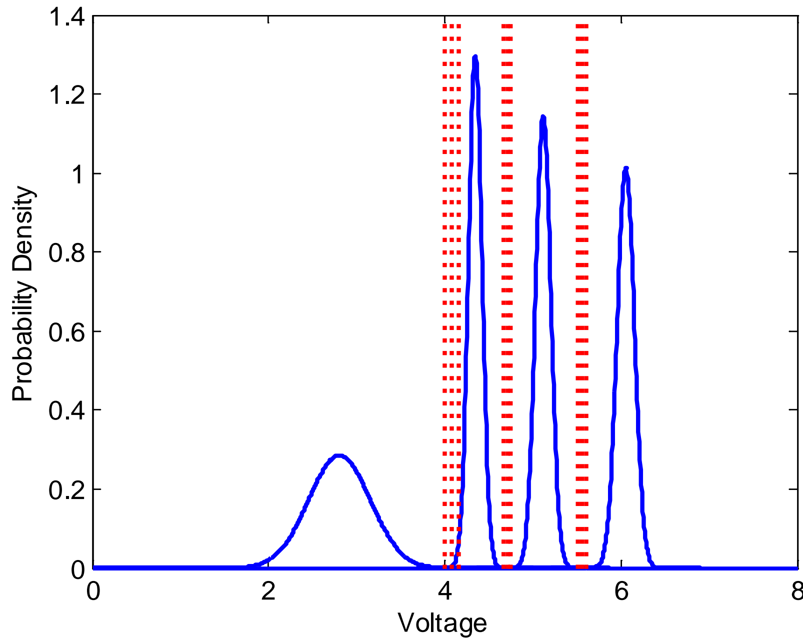
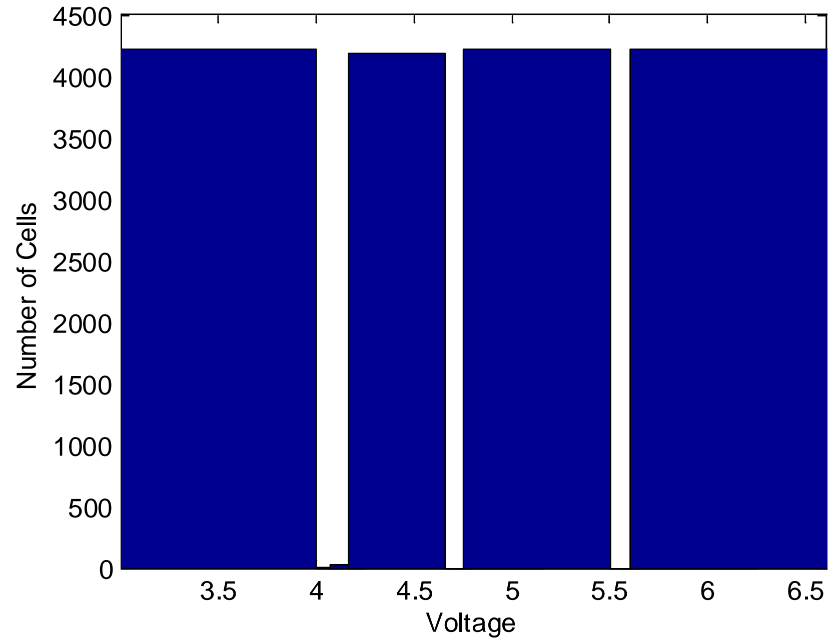
MMI Histogram Has Poor Resolution.





Histogram Choice

- Equal Interval Histogram [12]
  - Equal interval histogram does not adapt well to retention loss.
- Maximum Mutual Information Histogram [13]
  - This histogram optimizes decoder performance, but may not be the best for channel parameter estimation.
- Equal Probability Histogram
  - Every bin has an equal number of cells, intuitively good for parameter estimation.

[12] Dong-hwan Lee; Wonyong Sung, "Estimation of NAND Flash Memory Threshold Voltage Distribution for Optimum Soft-Decision Error Correction," Signal Processing, IEEE Transactions on , vol.61, no.2, pp.440,449, Jan.15, 2013
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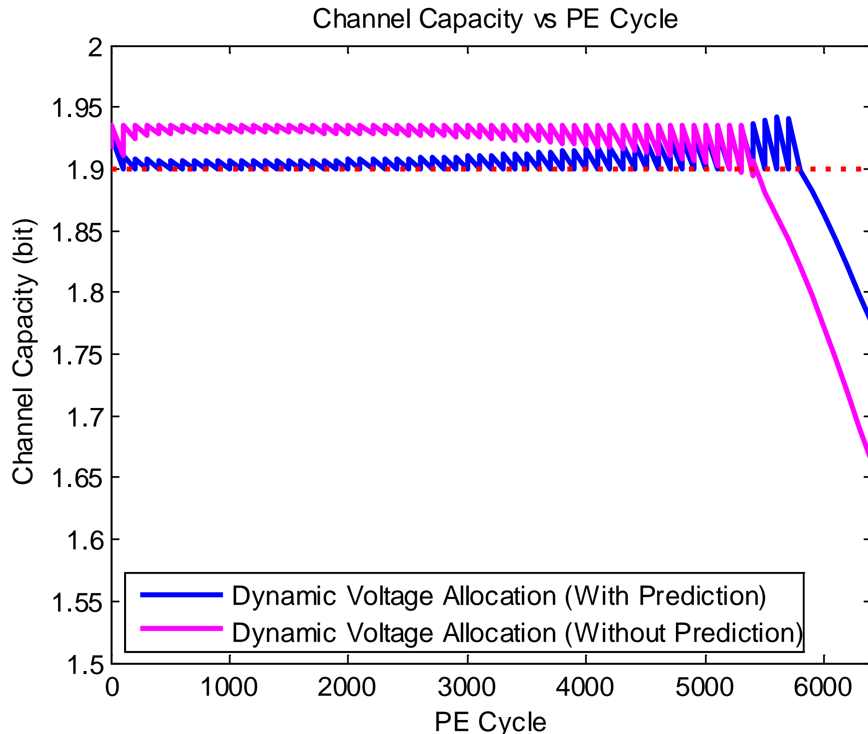
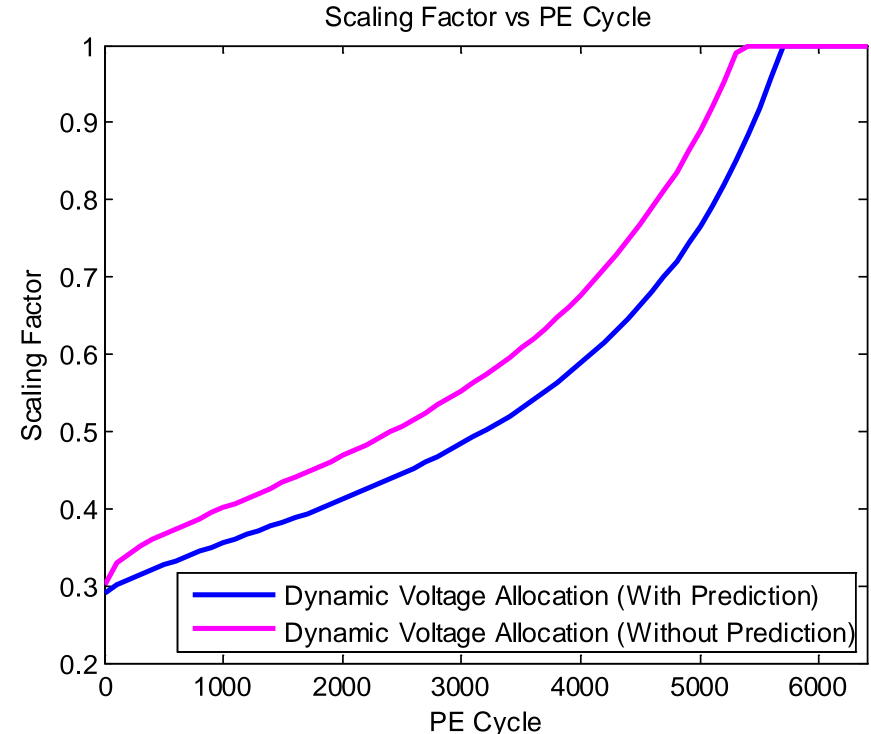
Prediction vs Fixed Margin

- Prediction requires knowledge of parameter degradation models.
- In reality, the parameters derived from degradation models may not always represent the performance of every block.
- Dynamic Voltage Allocation can utilize current channel condition with a fixed margin.
- The fixed margin should be set to allow channel capacity remain above the optimization target until the next adaptation.

Prediction vs Fixed Margin





- There is a 500 PE loss.
- Dynamic Voltage Allocation using current channel condition can still extend the block's lifetime by 77%.

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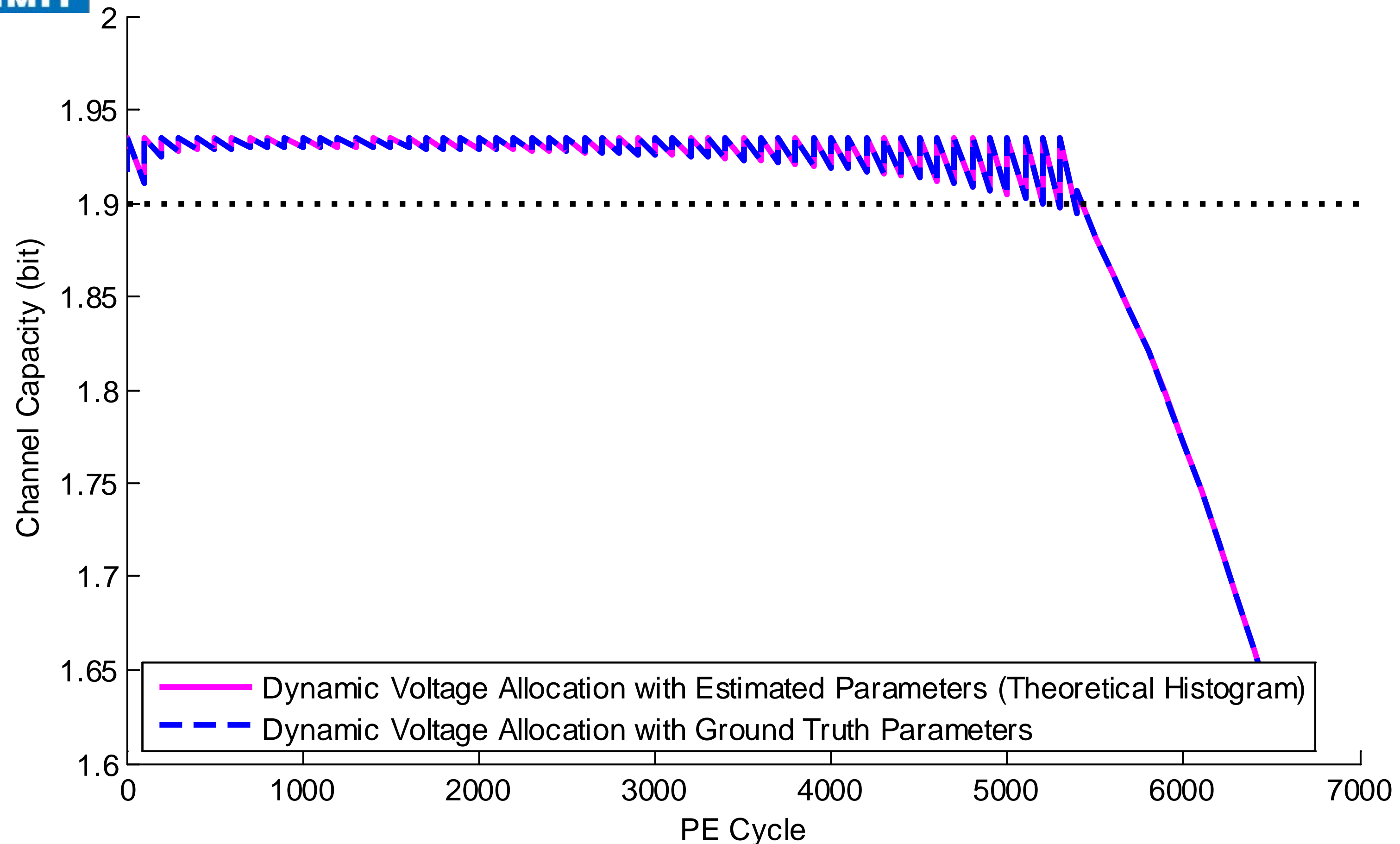
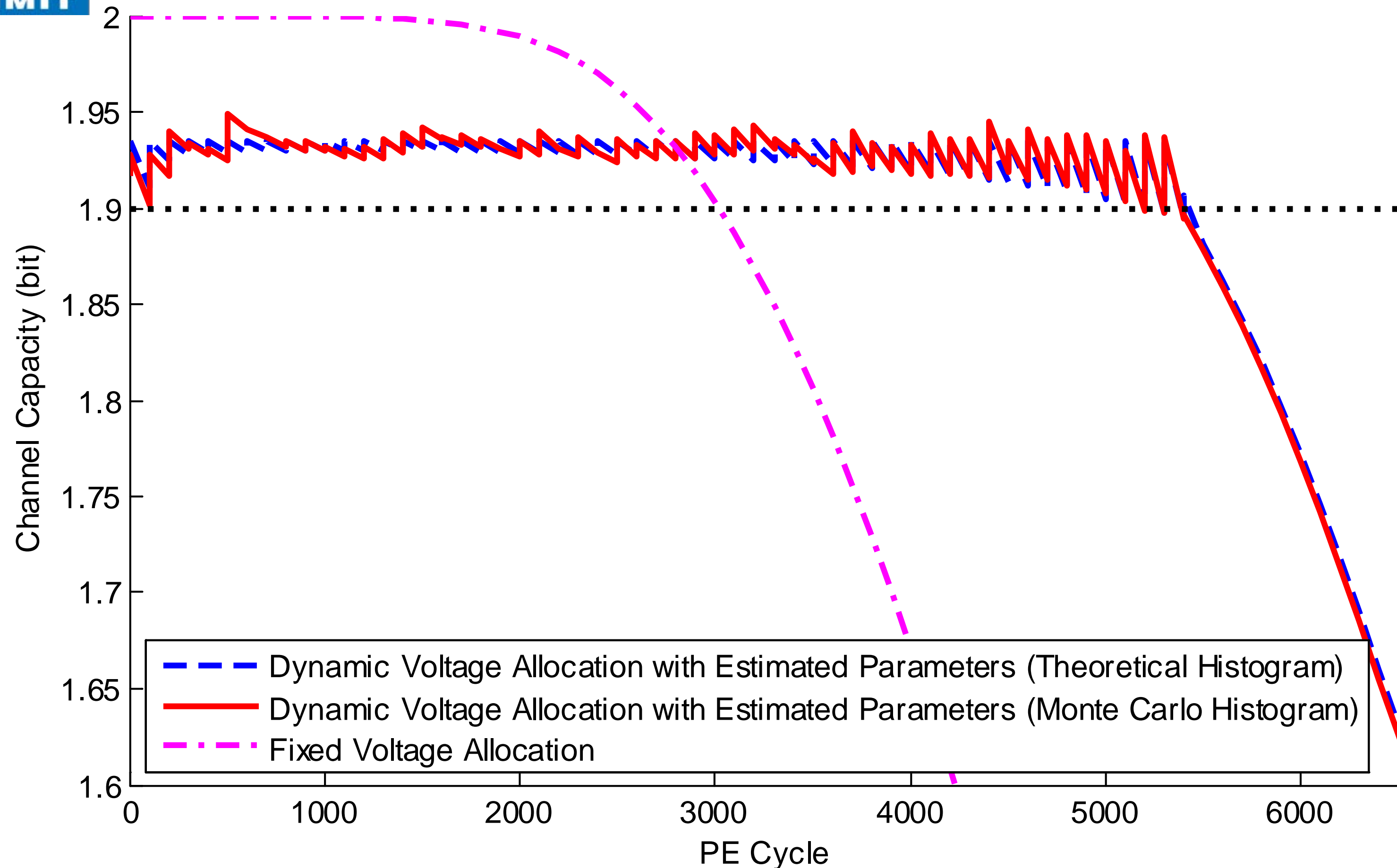
SIMULATION RESULT

Theoretical Simulation Result for MLC Flash



- Comparison of fixed margin DVA with perfect channel knowledge and estimation of channel using idealized equal probability histogram of 9 bins.

Monte Carlo Simulation Result for MLC Flash



- Comparison of fixed margin DVA with channel estimation using idealized equal probability histogram of 9 bins and realistic Monte Carlo generated histogram.

UCLA Center on Development of Emerging Data Storage Systems (CoDESS)

- CoDESS is founded in 2013.
- Webpage: http://www.uclacodess.org/
- Mission:

  - Push the frontiers in emerging data storage systems through integrated research program.

  - Create highly-trained workforce of graduate students and post-doctoral researchers.
- For more information, please email to

  - Prof. Lara Dolecek (dolecek@ee.ucla.edu)

  - Prof. Richard Wesel (wesel@ee.ucla.edu)