Constant-Blocklength Multiple-Rate LDPC Codes for Analog-Decoding Implementations

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Abstract— **This paper describes and analyzes low-density parity-check codes for a variety of different rates that all share the same fundamental decoder architecture. This technique allows the design of programmable analog LDPC decoders for different rates. An important advantage of this approach is that all effective code rates have the same blocklength as opposed shortening and puncturing that reduce the effective blocklenght as the rate changes. The proposed design method maintains good graphical properties and hence low error floors for all rates.**

Index Terms— **Analog Decoding, Channel coding, Low-Density Parity-Check (LDPC) codes, Multiple-rate codes.**

I. Introduction

PRACTICAL communication systems often need to operate at several different rates. To keep the implementation as simple as possible, the same basic hardware architecture should be able to decode the encoded data at all possible rates. One way to achieve this with Low-Density Parity-Check (LDPC) codes is to generate higher-rate codes by puncturing lower-rate codes as proposed in [1], [2] and [3]. However, puncturing reduces the code blocklength, which degrades performance. For the highest-rate codes, where the puncturing is most severe, the performance degradation is significant when compared to an LDPC code with the original blocklength.

Another way to achieve this is to generate lower-rate codes by shortening higher-rate codes, as described in [2]. As with puncturing, shortening reduces the code blocklength, which degrades performance. For the lowest-rate codes where the shortening is most severe, the performance degradation is significant when compared to an LDPC code with the original blocklength.

The row-combining technique, introduced in [4], generates LDPC codes with a structure that supports a wide range of rates while maintaining a constant code blocklength. The basic idea is to generate higher rate codes (called effective codes in this paper) from a low-rate code (called the mother code in this paper) by reducing the number of rows in its parity check matrix. This reduction is achieved by linearly combining the rows, which is equivalent to replacing a group of check nodes with a single check node that sums all the edges of the original check nodes.

In this paper these codes will be called Strict Row Combining (SRC) codes. SRC codes have good behavior at some high rates, but there is a loss in performance at low rates due to the strict constraints row-combining places in the design of the code in [4].

A performance improvement is obtained by adding a few edges in the graph as the rows are combined. This allows the code to have good variable-node degree distributions at each rate. In this paper these codes will be called Row Combining with Edge Variation (RCEV) codes.

In general, row combining allows the analog decoder designer to build one circuit that can decode codes of different rates by simply switching on and off some connections in the circuit. This makes analog decoders very attractive for applications that need a wide variety of rates where puncturing and shortening would significantly shorten the effective blocklength of the codes.

Section II describes the row-combining approach. Section III explains how row combining can be used to build a programable analog decoder. A design method for SRC codes is proposed in Section IV. Section V describes the RCEV code design approach that results in an improvement in performance with respect to SRC codes. Section VI compares the performance of SRC, RCEV, single-rate stand-alone codes and punctured codes. Section VII delivers the conclusions.

II. Row-Combining Codes

Consider the example mother LDPC matrix in (1),

$$H_{\frac{1}{2}} = \begin{pmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{pmatrix}. \quad (1)$$

This is a rate-1/2 mother LDPC matrix with blocklength 12 whose graph representation can be seen in Fig. 1. This is by no means a good LDPC code but the reader should see it as an example to explain row combining. Fig. 1 also shows that replacing each pair of nodes with a new single node transforms this rate-1/2 code into a rate-3/4 code. This is equivalent to summing the rows of the mother LDPC matrix that correspond to the check nodes that are combined, since the check nodes in the example do not have any common neighbors. In general, the mother matrix

This work was supported by the state of California and three corporations; ST Microelectronics, Conexant, and Texas Instruments, through UC discovery grant COM 03- 2, UC MICRO grant 03-92, and UC MICRO grant 03-93 respectively. This paper was presented in part at the Asilomar Conference on Signals, Systems and Computers, Pacific Grove, CA, 2004.

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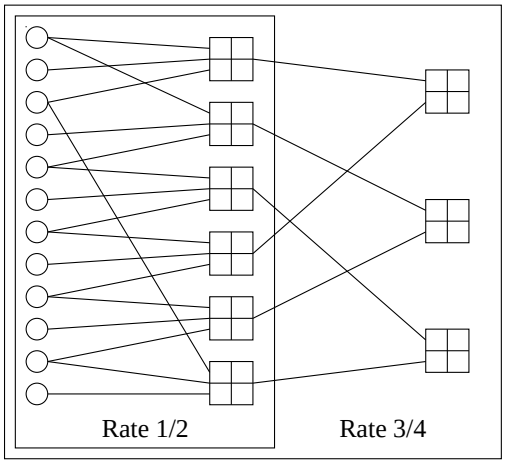

Fig. 1. Graph of a rate-3/4 LDPC code obtained from a rate-1/2 LDPC code via row combining.

should be designed so that the rows that will be combined don't have ones in the same column.

The following is the effective rate-3/4 LDPC matrix that resulted from the row combining described in Fig. 1, where the resulting row 1 comes from combining rows 1 and 3 of the mother matrix, row 2 comes from combining rows 2 and 4 and row three results from the combination of rows 3 and 6:

$$H_{\frac{3}{4}} = \begin{pmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \end{pmatrix}. \quad (2)$$

It is easy to see that many different rates can be obtained from the same mother code by changing the way rows are combined. This method changes the rate without changing the blocklength or the basic architecture of the decoder as explained in section III. Furthermore, the variable-node degree distribution remains the same as the rate changes.

III. Impact of Row Combining on Analog Decoding

Analog decoders of turbo-like codes were introduce simultaneously in 1998 by Hagenauer [6] and Loeliger et al. [7]. A good in-depth look to this alternative decoding hardware can be found in [8]. Analog decoders are circuits that oscillate until an equilibrium state is reached. Analog decoding shows promise because the decoders require low power and the convergence is typically faster than with digital decoders. Digital decoders can use the same hardware to decode different LDPC codes by re-programming the chip. Their analog counterparts are not programable, and they need different circuits to decode different LDPC codes. Since many applications need various codes with different rates, the lack of programmability of analog decoders makes them less attractive than digital decoders for some applications.

However, row-combining codes allows programable analog decoders. If row combining is used, an analog decoder that works for all the rates would consist of the circuit that decodes the mother code, with switches that turn on and off the connections to the new check nodes as shown in Fig. 1 that increase the rate of the code.

IV. Design of SRC Codes

This section proposes a design method for row-combining codes given the blocklength of the code and the mother and effective rates. Since only row combining is allowed to generate the high-rate matrices, these codes are called Strict Row-Combining (SRC) codes.

The first step consists on the selection of both the variable-node degree distribution and the check-node degree distribution. As seen in Fig. 1, the number of neighbors of the variable nodes remains the same as the rate changes, thus the variable-node degree distribution will also remain unchanged. This implies that this degree distribution can not be optimized for the different rates of the code, so a degree distribution that works reasonably well for all the rates must be chosen.

A concentrated degree distribution is a degree distribution in which every node has the same degree or all the degrees are within one of each other. Concentrated check-node degree distributions tend to approximate theoretical optimality [9].

The check-node degree distributions depend on the selection of the rows to be combined. There is a simple way to achieve a concentrated check node degree distribution for all the codes if the desired rates have the $(a-1)/a$ form. The mother matrix will be a square matrix with a concentrated check node degree distribution. This square matrix corresponds to a rate-0 LDPC code. Combining a rows at a time, generates a code with rate $(a-1)/a$ as long as the total number of rows of the mother matrix is a multiple of a. This effective code will have a concentrated check node degree distribution. This shows that SRC codes can maintain a concentrated check node degree distribution among all its rates if they all are in the $(a-1)/a$ form.

The only thing left is to assign the positions and right cyclic shifts of the non-zero sub-matrices in the mother code. It is well known that the performance of the LDPC codes is limited by the fact that their graphs contain cycles which compromise the optimality of the belief propagation decoding. These cycles generate error floors in the performance of LDPC codes in the high SNR regions. However, the negative effect of the cycles can be reduced using graph conditioning techniques such as those described in [10] and [11]. Therefore, the mother and effective matrices of SRC codes will be generated using simultaneous graph conditioning as described in [4].

V. Row Combining with Edge Variation (RCEV) Codes

A. Disadvantages of SRC Codes

The main disadvantage with SRC codes is that the row-combining approach doesn't permit different variable-node degree distribution for different rates. This is problematic since in principle different rates require different variable-node degree distributions for theoretical optimality, as stated in [9].

One of the most critical elements in the variable-node degree distribution design is the selection of the number of degree-two variable nodes the codes have. In order to have good error floor properties the number of degree-two variable nodes can not exceed the number of check nodes as shown in [12]. Having more degree-two nodes than check nodes implies that there will be cycles composed by only degree-two nodes and check-nodes. These cycles are stopping sets and have been shown to degrade the performance of the codes [10]. These cycles will grow smaller and more numerous as the number of degree-two nodes increases, further worsening the performance of the codes.

This implies that the maximum number of degree-two variable nodes for a family of SRC codes is given by the number of check nodes of the highest rate effective code. This limits the performance of the lower rate codes since their optimal degree-distribution generally requires a significantly larger number of degree-two variable nodes [12]. The difference in the distributions depends on the rates of both the mother code and all the effective codes. The loss in performance due to this limitation increases as the range of possible rates of the SRC codes grows larger.

B. Edge Variation

The previously presented problem can be avoided by improving the row-combining method. By allowing the addition of edges as rows are combined, the degree-distributions for the different codes can be different. The key to maintaining a simplified decoder architecture is to make the number of additions small compared to the total number of edges in the graph.

The edge-addition strategy consists of assigning an optimal variable-node degree distribution to the mother code. It will be assumed that the number of degree-two nodes is equal to the number of check nodes of the mother code matrix which is a worst case scenario. Now, every time a row is combined, an edge is added to a degree-two variable-node so that the maximum number of degree-two nodes continues to be the number of check nodes in the graph. If the number of degree-two variable nodes of the mother matrix is fewer than the number of check nodes, fewer edges need to be added, which is better since it requires fewer additions. This is the reason why having the number of degree-two nodes equal to the number of check nodes of the mother code matrix is the worst-case scenario.

RCEV codes are designed using the design steps for SRC codes given in section IV, along with the edge variation techniques described in this section.

VI. Performance Comparison

Fig. 2 shows the AWGN performance of a SRC code and four stand-alone codes with rates corresponding to those of the effective codes of the SRC code. The mother code is a rate-0 code as explained in section IV. The effective codes have rates 1/2, 2/3, 3/4, and 5/6. The blocklength of the codes is 1944 bits and a maximum of 15 iterations was used in the simulation.

Fig. 2 shows that the SRC codes perform very well under these conditions (blocklength, and number of iterations). The effect of the non-optimality of the variable-node degree distribution for the rate-1/2 code is not noticeable with 15 iterations. This is because for such a small number of iterations performance is dominated by the high-degree variable nodes. Thus, the lower-than-optimal number of degree-two nodes of the rate-1/2 code does not dramatically affect performance. For fifty iterations, the rate-1/2 code performance is affected, as we'll see shortly.

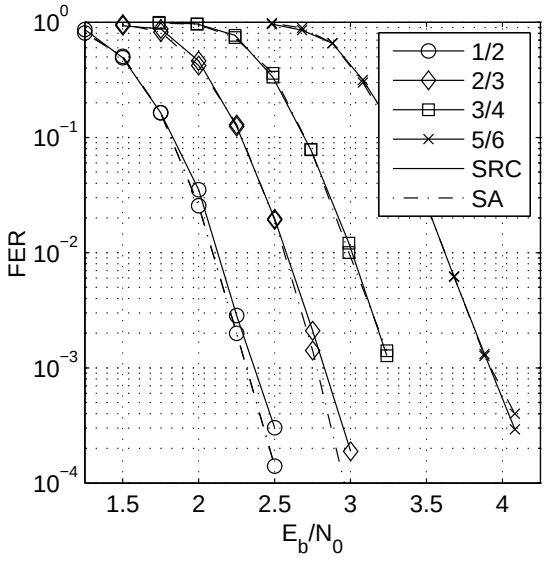

Fig. 2. Performance of SRC and Stand-Alone (SA) codes with blocklength 1944 on an AWGN channel. Maximum number of iterations equal to 15.

This comparison at 15 iterations is practically important since there are many applications that only allow a small number of iterations of the digital decoder which translates into a small maximum amount of time for analog decoders. For example, in most wireless applications the channel decoding must be done in a very small amount of time.

Fig. 3 presents another comparison of the performance on an AWGN channel of a SRC code, four stand-alone codes, and a RCEV code. The row-combining codes have effective rates 1/2, 2/3, 3/4 and 5/6. The blocklength of the codes is 1944 bits and a maximum of 50 iterations was used in these simulations.

As expected, Fig. 3 shows the loss in performance of the SRC low rate codes. The SRC rate-1/2 code show a performance gap of more than 0.2 dB with respect to the stand-alone codes with the same blocklength and this is due to their inadequate variable-node degree distribution.

As observed in Fig. 3 the FER of the lower rates of the RCEV code are significantly better than those of the lower rates of the SRC code and close to the stand-alone codes. This gain follows from the improved degree distributions of the RCEV codes over those of the SRC codes. For the high rate codes there is very little difference between the performances of the RCEV and SRC codes, since their degree distributions are very similar. RCEV techniques allow the optimization of the degree distributions for each rate.

A comparison in the performance of RCEV codes and

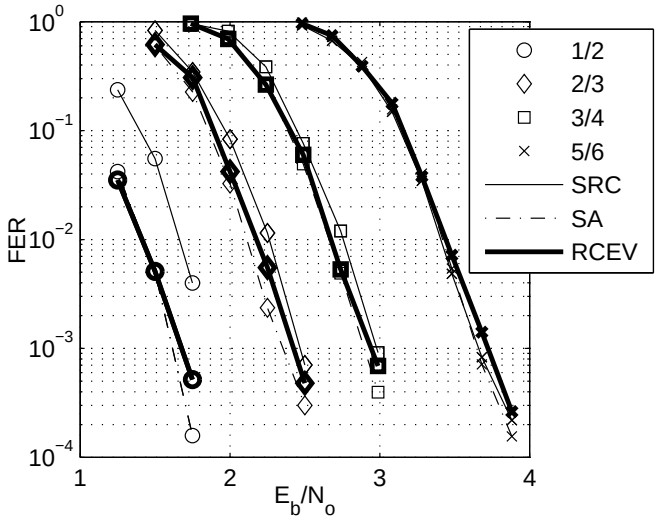

Fig. 3. Performance of SRC, RCEV, and Stand-Alone (SA) codes with blocklength 1944 on an AWGN channel. Maximum number of iterations equal to 50.

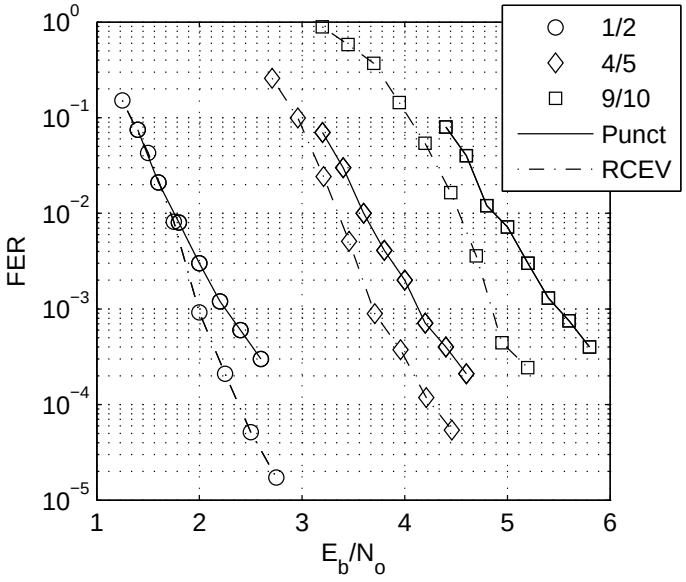

Fig. 4. Performance of RCEV codes and punctured LDPC codes.

punctured LDPC codes is shown in Fig. 4. The punctured codes correspond to the ones presented in [3]. The RCEV code was designed to have a very similar degree distribution to the punctured code so that the comparison would be fair. The blocklength of the punctured codes is 1024 while the blocklength of the RCEV codes is 1030. There is a clear performance gap between the higher rate codes. This is due to the fact that puncturing reduces the effective blocklength of the code.

VII. Conclusions

As we know from information theory, channel codes approach capacity-achieving performance as blocklength goes to infinity. Both theory and practice confirm that codes with longer blocklengths perform better. Recently, puncturing and shortening have been used to provide a variety of rates in the context of a single decoder architecture, but these techniques shorten the code blocklength as rates move away from the rate of the mother code.

Multiple-rate LDPC codes that avoid this blocklength reduction can be generated using a row-combining approach. SRC codes allow the use of a simple decoder that can be used to decode the mother and all the effective rates. The design of these codes impose some constraints that barely affect the performance when the codes are used at a small number of iterations (small maximum decoding time). As the maximum number of iterations (maximum decoding time) used increases, the performance gap between SRC codes and stand-alone codes also increases.

RCEV codes relax these constraints, and show a gain in performance with respect to SRC codes for a large number of iterations (large maximum decoding time). This increase in performance comes at a cost of architecture complexity. The performance of RCEV codes is very close to the performance of stand-alone codes for a large number of iterations.

These codes become attractive for applications that require both performance close to capacity and a low decoder complexity.

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