Constant-Blocklength Multiple-Rate LDPC Codes for Analog-Decoding Implementations

Andres I. Vila Casado
Stefano Valle*
Wen-Yen Weng
Richard D. Wesel

*Stefano Valle is with STMicroelectronics

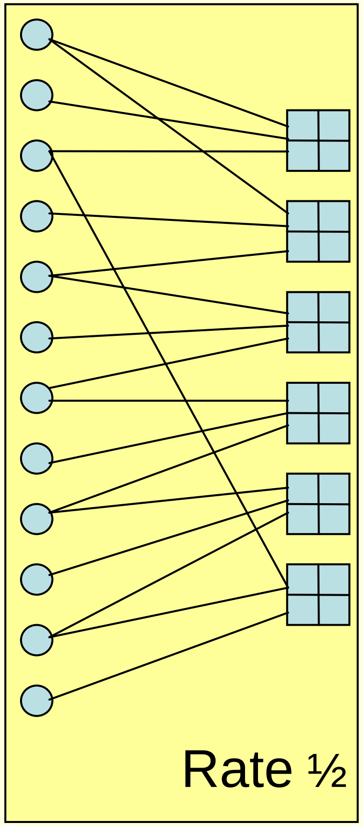
Outline

- Motivation
- Row-combining method
- Benefits of row-combining for an analog-decoder implementation
- Strict Row-Combining (SRC) codes design
- Row-Combining with Edge Variation (RCEV) codes
  - Shortcomings of SRC codes
  - Design technique of RCEV codes
- Conclusions

Motivation

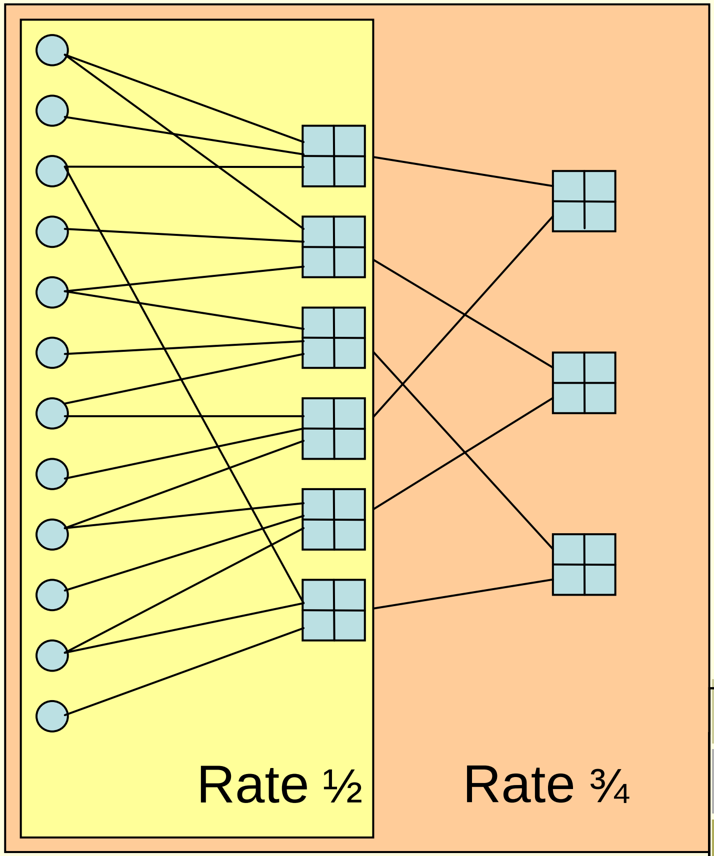
- Practical communication systems need to operate at several different rates
- The same basic hardware should be able to decode the data at all possible rates
- For LDPC codes this can be achieved by puncturing [Ha 02] or shortening [Jones 04].
- Both puncturing and shortening reduce the code blocklength as rate varies away from the mother code rate, which degrades performance.
- We present the row-combining method to generate multiple-rate LDPC codes that maintain the same blocklength across all the rates.

Rate-1/2 Mother LDPC Matrix



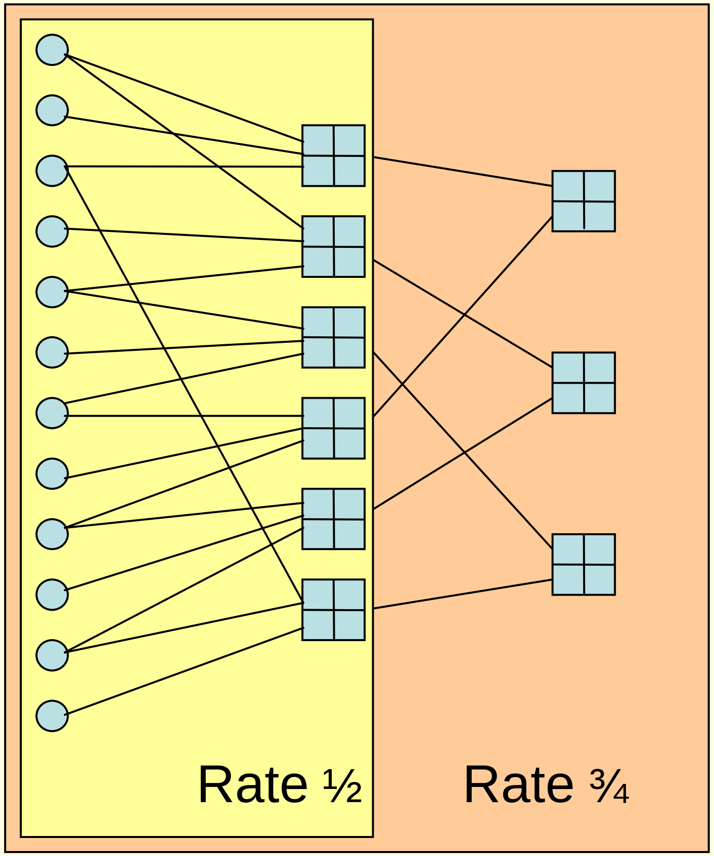
$$H_{R=1/2} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

Row-Combining to produce rate 3/4



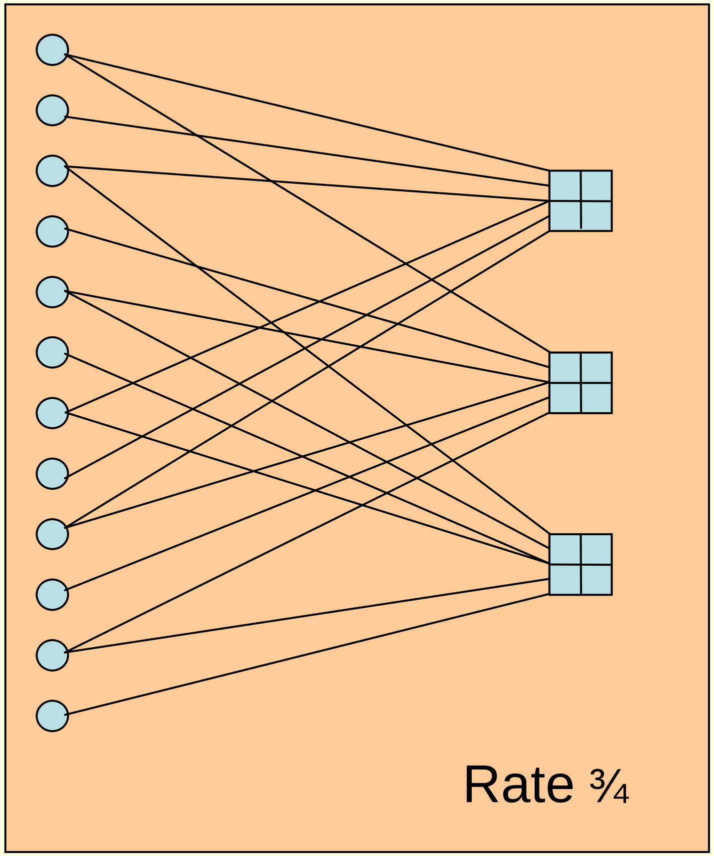
$$H_{R=1/2} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

Row-Combining to produce rate 3/4



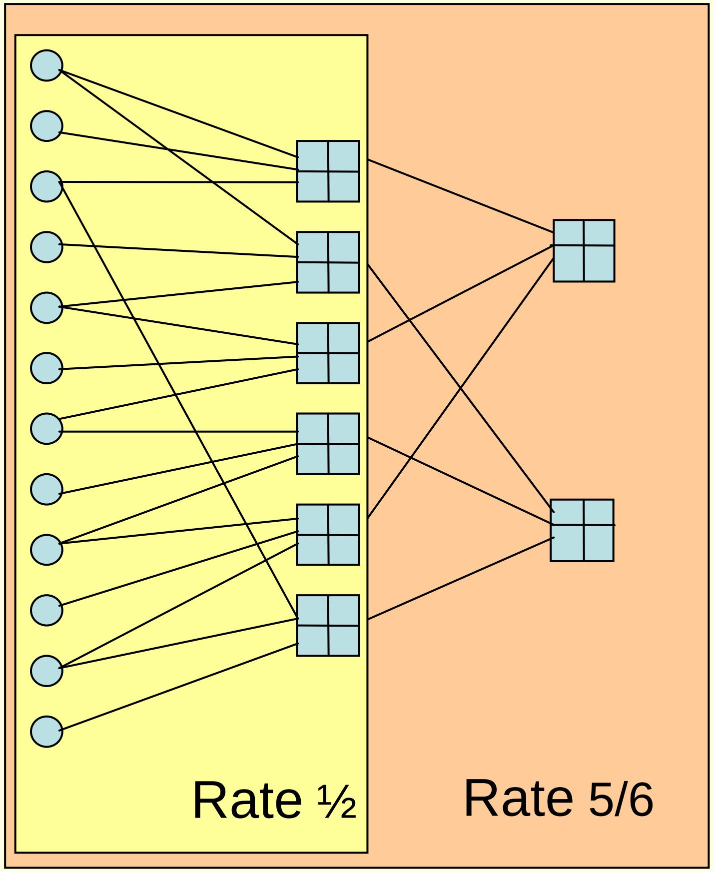
$$H_{R=3/4} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

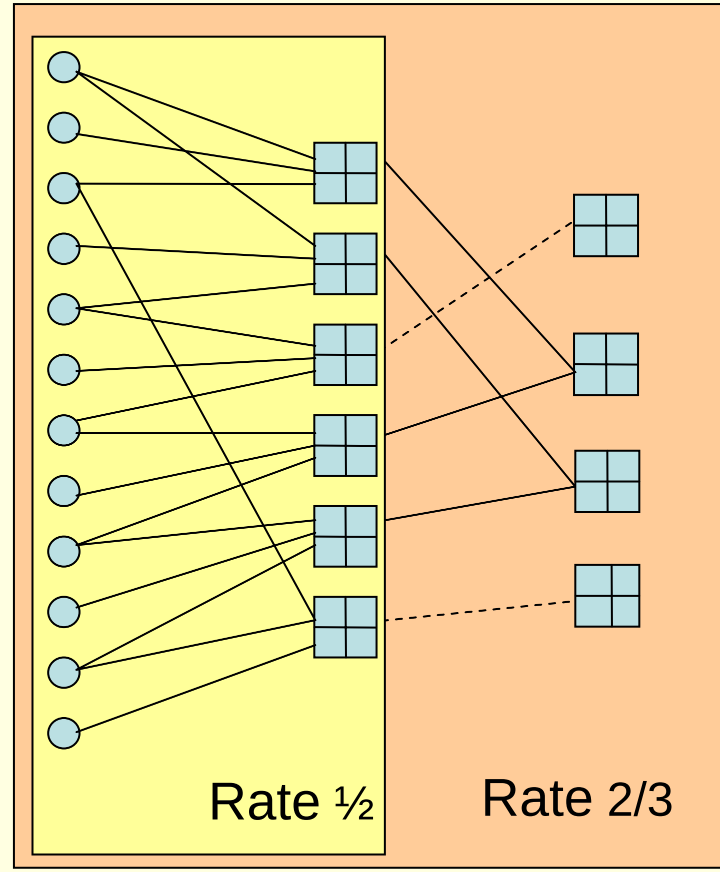
Row-Combining to produce rate 3/4



$$H_{R=3/4} = \begin{bmatrix} 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

Row-Combining to produce rate 5/6 and 2/3





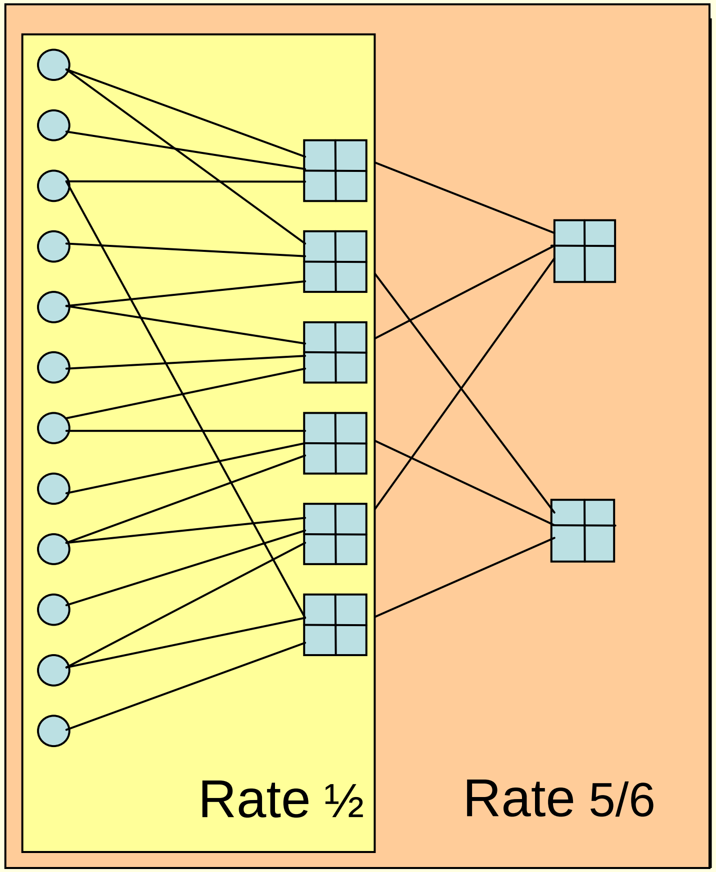
$$H_{R=5/6} = \begin{bmatrix} 1 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 1 & 1 & 1 & 0 \\ 1 & 0 & 1 & 1 & 1 & 0 & 1 & 1 & 1 & 0 & 1 & 1 \end{bmatrix}$$

$$H_{R=2/3} = \begin{bmatrix} 0 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 1 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 & 0 & 0 \\ 1 & 0 & 0 & 1 & 1 & 0 & 0 & 0 & 1 & 1 & 1 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 & 0 & 0 & 0 & 0 & 1 & 1 \end{bmatrix}$$

Analog Decoders

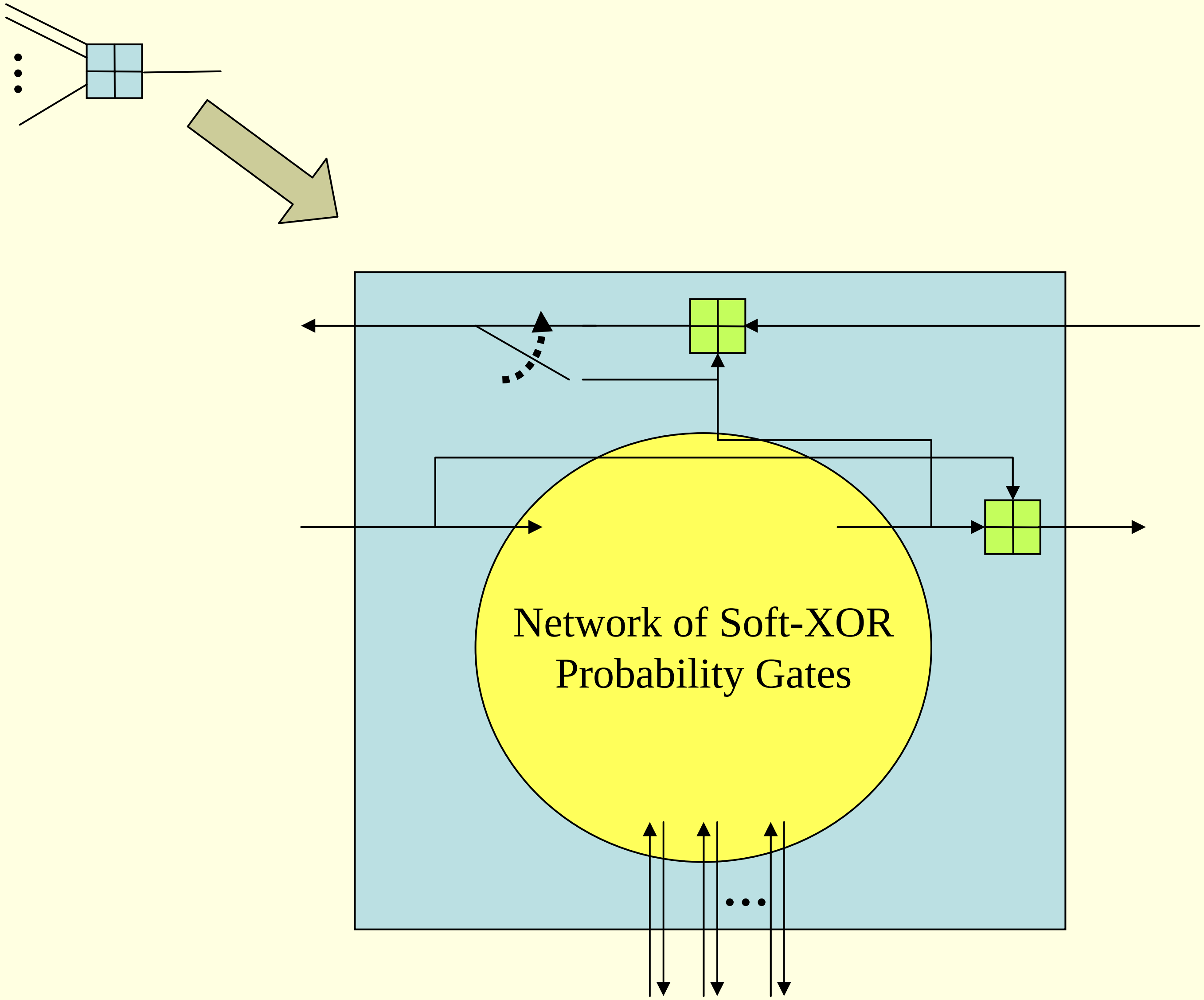
- Analog circuits that perform the operations needed in message passing are build and connected according to the graph of the code
- Thus the decoder is a big analog circuit that oscillates until an equilibrium state is reached (or a maximum amount of time has passed)
- Show promise given that they require low power and are faster than their digital counterparts
- A big setback is the lack of programmability (one analog decoding circuit per code)
- Row-combining codes allows different codes of different rates to be decoded with the same basic analog circuit

Row-Combining and Analog Decoding



- The higher-rate code is decoded by turning on the extra check-nodes and connecting them to the circuit

Mother Code Check Nodes



Strict Row-Combining (SRC) Codes

- Higher-rate codes are generated using only row-combining
- All higher-rate codes have the variable-node degree distribution of the “mother” code
- The check-node degree distribution of the higher-rate codes is given by the check-node degree distribution of the “mother” code and the row-combining strategy

Design of SRC Codes

- Chose rates and blocklength.
- Chose variable-node degree distribution.
- Chose the rows to be combined in order to generate the higher-rate codes.
- Generate simultaneously the H matrices of the code.

Variable-Node Degree Distribution

- The variable-node degree distribution is the same for all the rates.
- The optimal variable-node degree distribution [Richardson 01] changes with the rate.
- Thus, the variable-node degree distribution won’t be optimal for some of the chosen rates

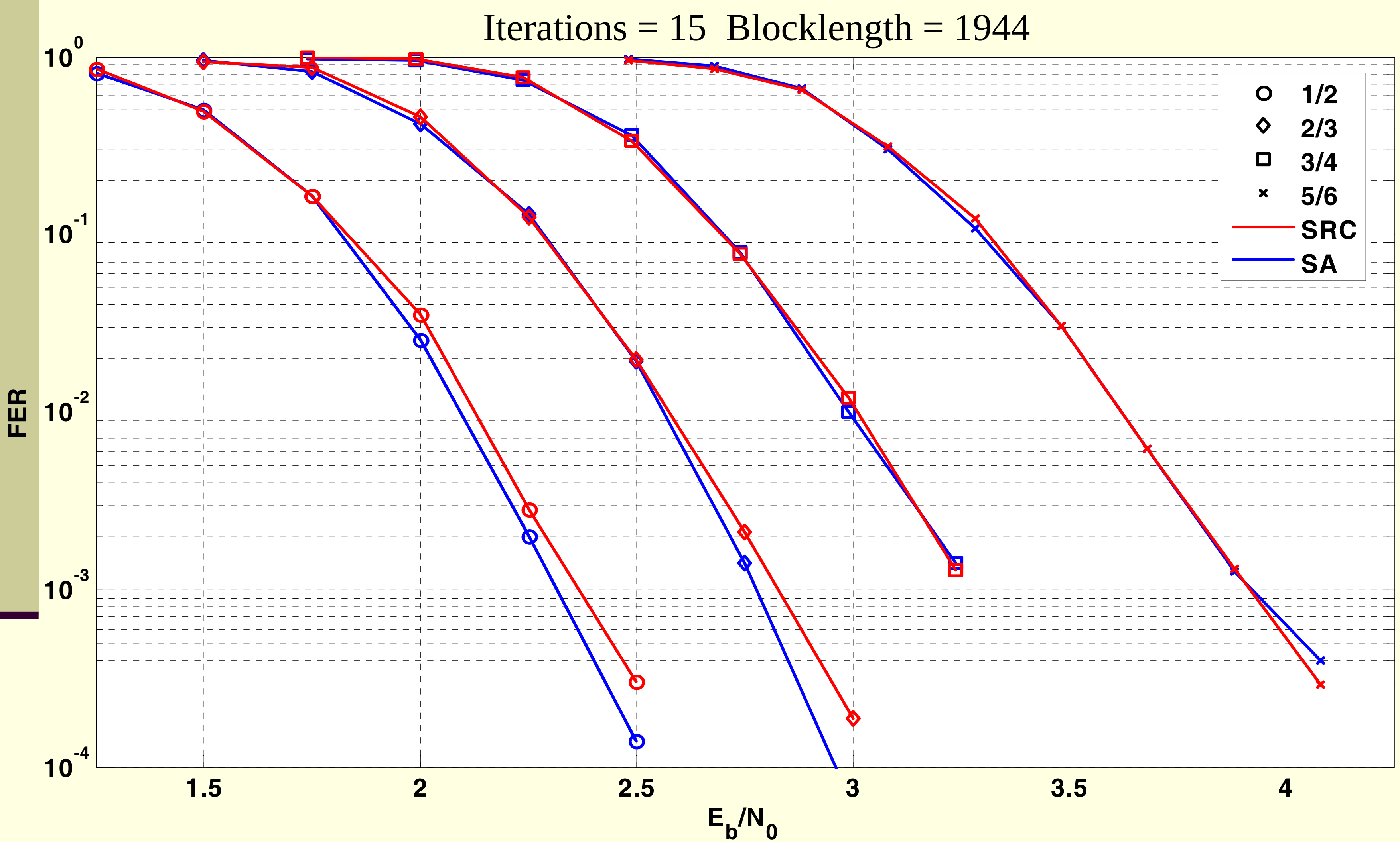
Rows to be combined

- The check-node degree distribution should be concentrated according to theory [Richardson 01].
- If the mother code has a uniform check-node degree distribution, combining equal-size groups of rows maintains a uniform check-node degree distribution.
- In our previous examples, if the rate-1/2 “mother” code has a concentrated degree distribution, then the rate-3/4 and rate-5/6 codes also have a concentrated degree distribution.
- Two check nodes that will be combined can not have any common neighbors
- The overall number of row combinations across all rates must be as low as possible

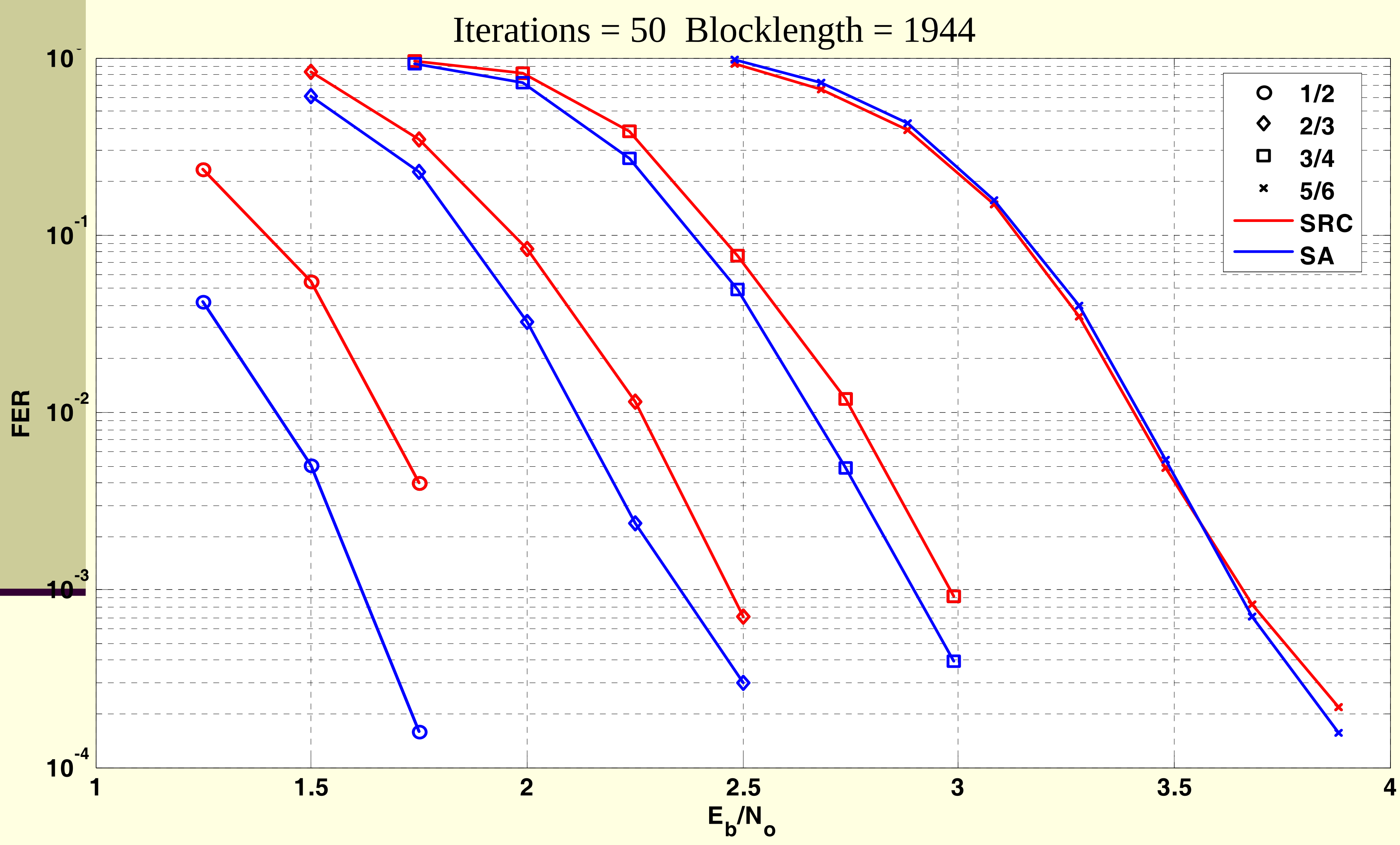
H Matrix Design

- Randomly generate a column according to the degree distribution and rows that will be combined.
- Check if the column satisfies graph constraints set for all the rates
- If the constraints are satisfied, move to the next column and if not, throw it away and repeat the process.

SRC vs Stand-Alone Codes



SRC vs Stand-Alone Codes



Non-Optimality of SRC Codes

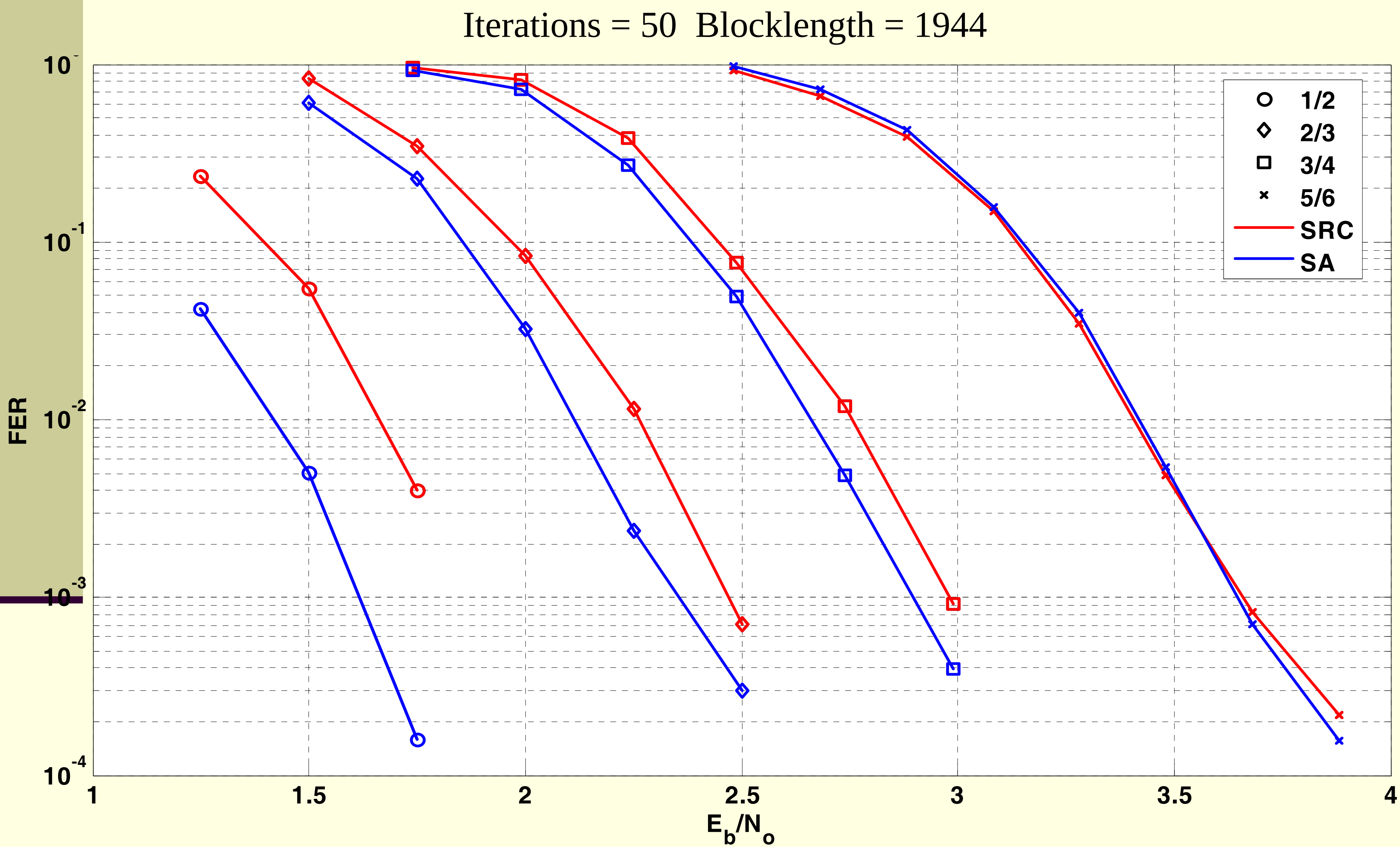
- A fixed variable-node degree distribution limits the performance of SRC Codes
- Specifically, the main problem is related to the few degree two variable nodes for the lower rate codes

Degree-2 Variable Nodes

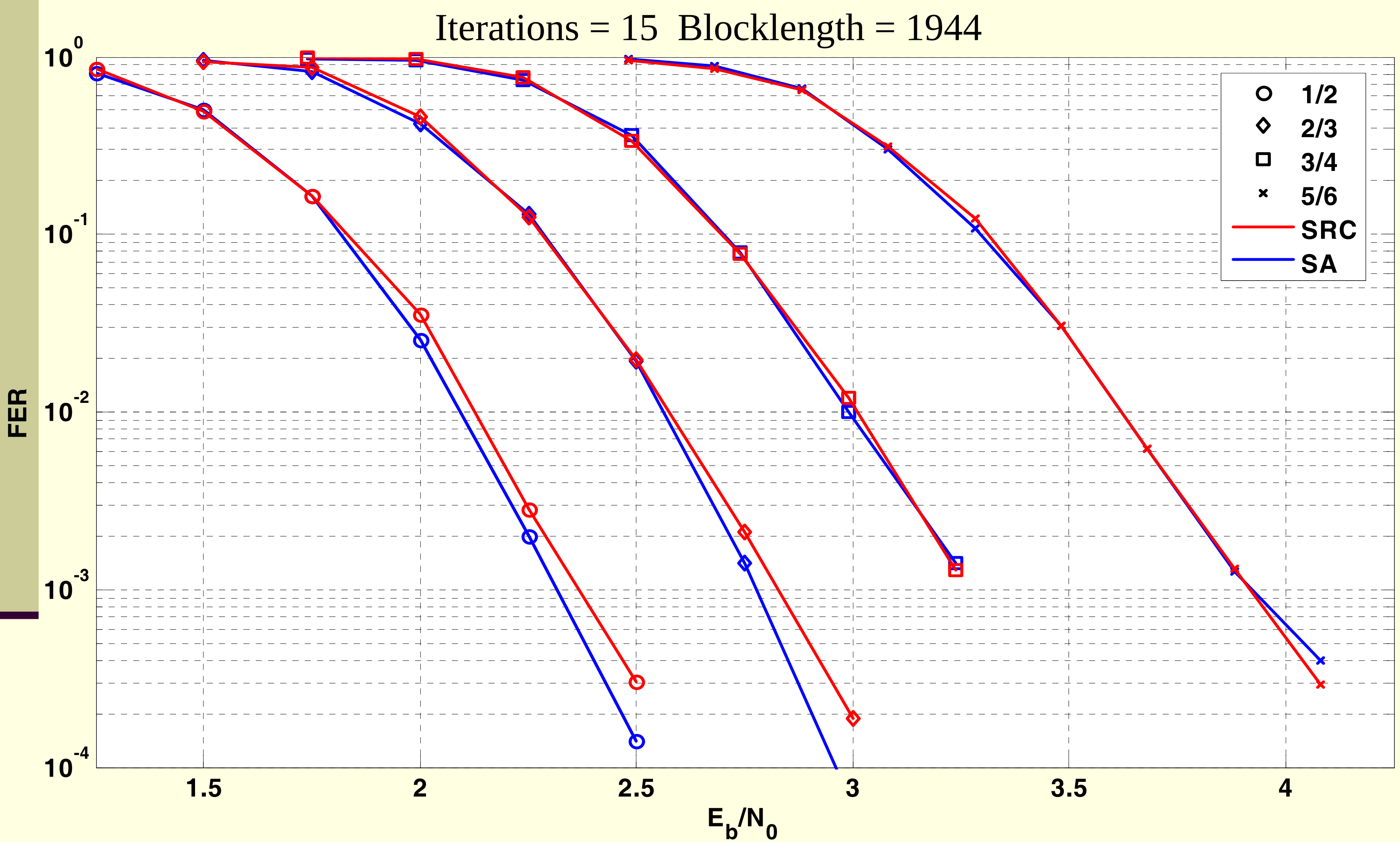
- Having more degree-2 variable nodes than check nodes guarantees the presence of cycles of degree-2 variable nodes which are stopping sets
- Thus, the maximum amount of degree-2 variable nodes in a SRC code is the amount of check nodes of the highest rate code
- This will limit the performance of the lower rate codes

$$\begin{bmatrix}
1 & & & & & & & & & \\
1 & 1 & & & & & & & & \\
 & 1 & 1 & & & & & & & \\
 & & 1 & 1 & & & & & & \\
 & & & 1 & 1 & & & & & \\
 & & & & 1 & 1 & & & & \\
 & & & & & 1 & 1 & & & \\
 & & & & & & 1 & 1 & & \\
 & & & & & & & 1 & 1 & \\
 & & & & & & & & 1 & 1
\end{bmatrix}$$

SRC vs Stand-Alone Codes



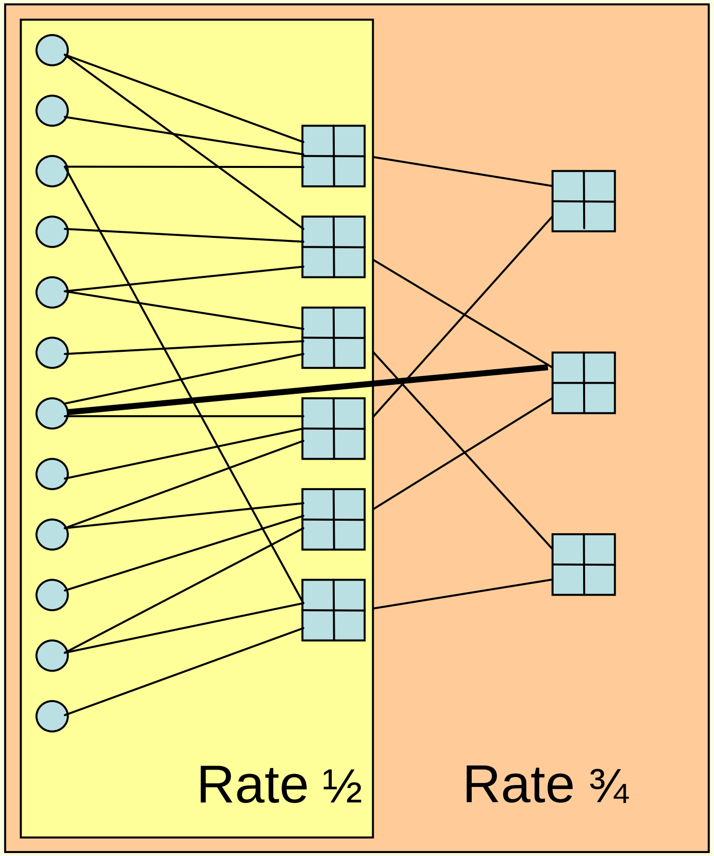
SRC vs Stand-Alone Codes



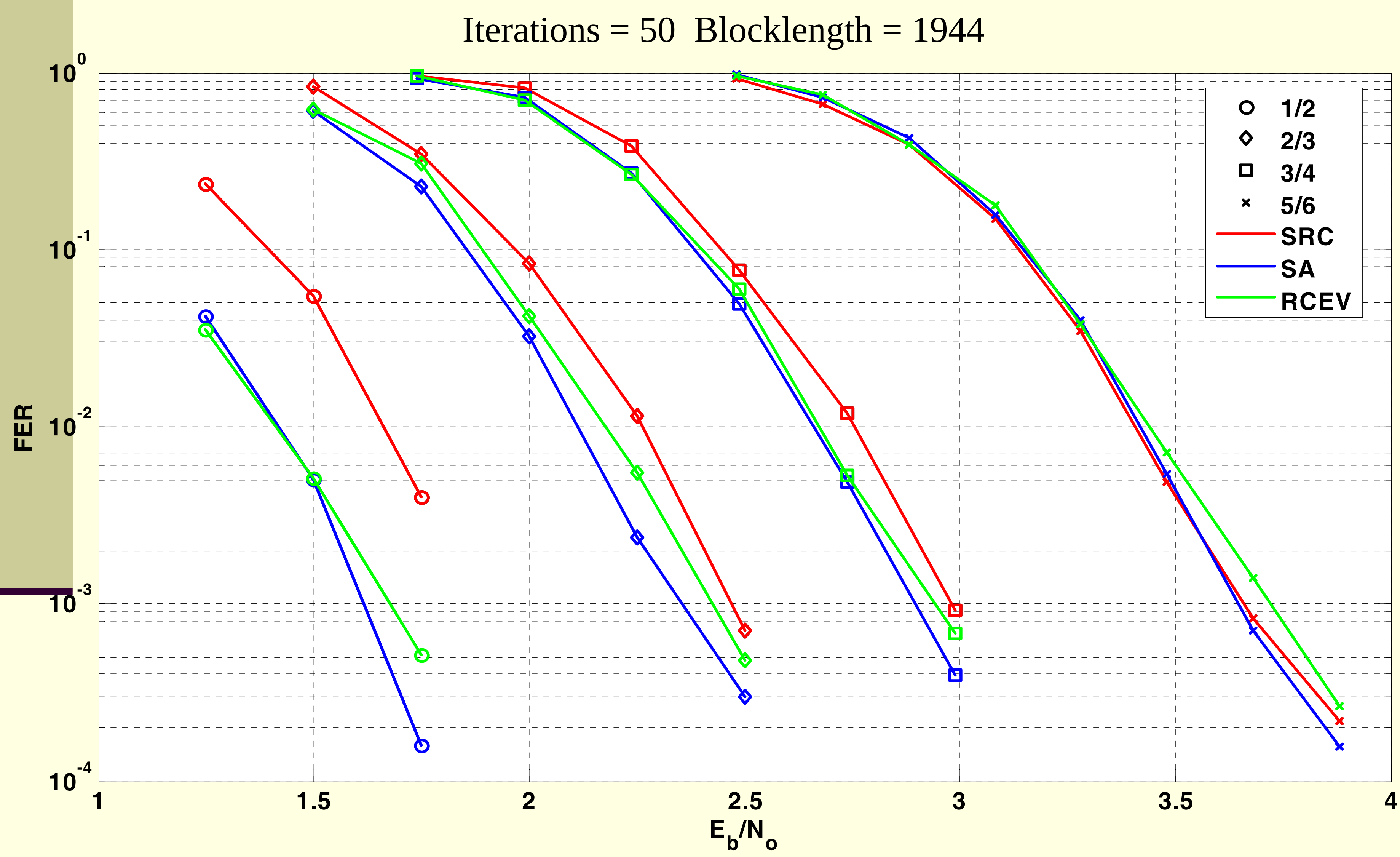
Row Combining with Edge Variation Codes

- RCEV codes allow minor edge variation as rows are combined
- Edge variation is done by adding edges to degree-2 variable nodes as the rows are combined
- This allows the lowest-rate LDPC code to have an “optimal” number of degree-2 variable nodes while keeping the highest-rate LDPC code without degree-2 variable node cycles

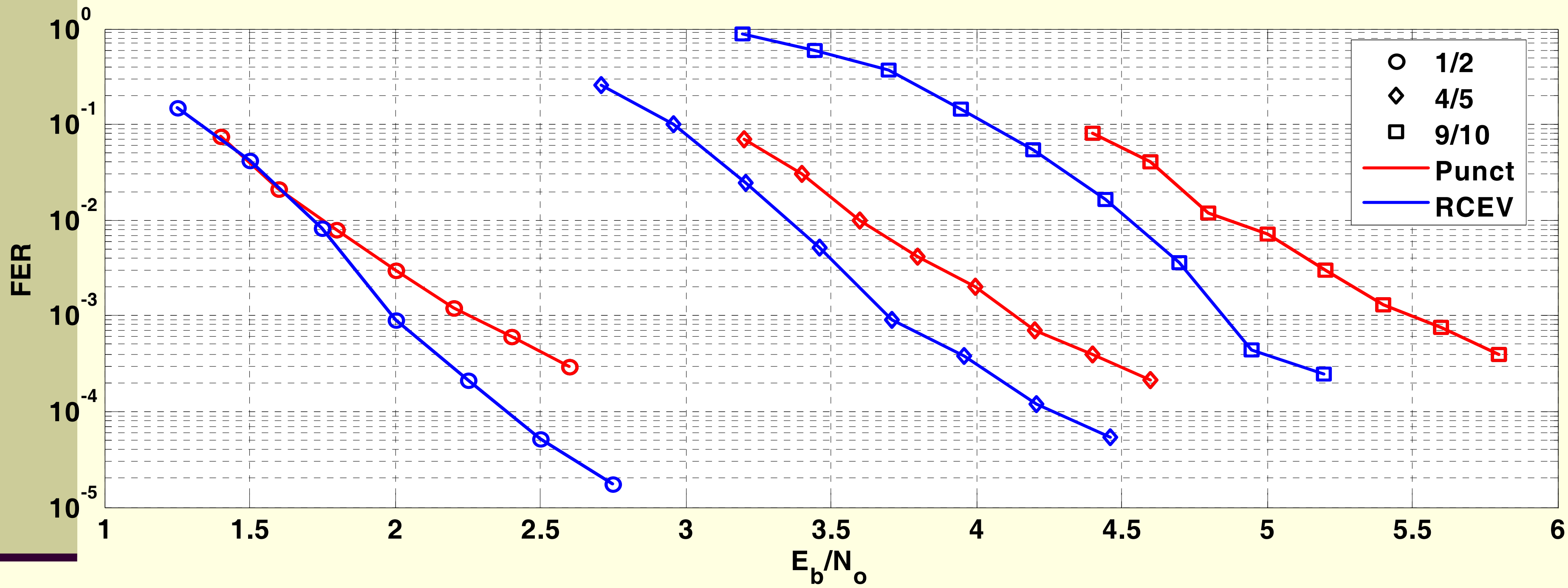
Row Combining with Edge Variation



SRC vs SA vs RCEV



Row Combining vs Puncturing



Conclusions

- Multiple-rate LDPC codes can be generated using a row-combining approach.
- All the codes can be decoded using the same analog circuit by turning on and off some parts of the circuit and switching on and off some connections.
- The advantage of the approach is that the codes have the same blocklength, thus maintaining good performance at all the rates.
- Also, graph conditioning algorithms can be used to design of the codes, producing good error floor performance at all the rates.
- For a large number of iterations (maximum decoding time), allowing edge variation improves the performance of the codes.