Information-Reduced Carrier Synchronization of BPSK and QPSK Using Soft Decision Feedback

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Introduction

- This paper addresses the carrier-phase estimation problem under low SNR conditions in a ***soft decision-directed*** LDPC-coded system.

- Two distinct techniques for joint decoding and synchronization :
  1. Modifying iterative detection/decoding algorithms and/or graph structure to include parameter estimation
  2. **Turbo Synchronization**: Pass messages between an independent phase estimation block and an essentially unmodified iterative decoder [Noels05]

- The technique in this presentation falls into this second category.

- We propose a ***soft decision-directed pilotless*** carrier recovery circuit with little modification to either the iterative decoder or the carrier recovery block.

Motivation

- When designing communication systems engineers need to decide whether or not to suppress the transmitted carrier power

- Total power = Carrier Power + Data Power → $P_t=P_c+P_d$
  - Carrier Power: related to the accuracy of the *carrier synch* process
  - Data Power: related to the accuracy of the *data detection* process (in the presence of perfect carrier synchronization).

- System design requires a proper trade off between these power requirements to minimize the *average error probability* of the system [Simon96] .

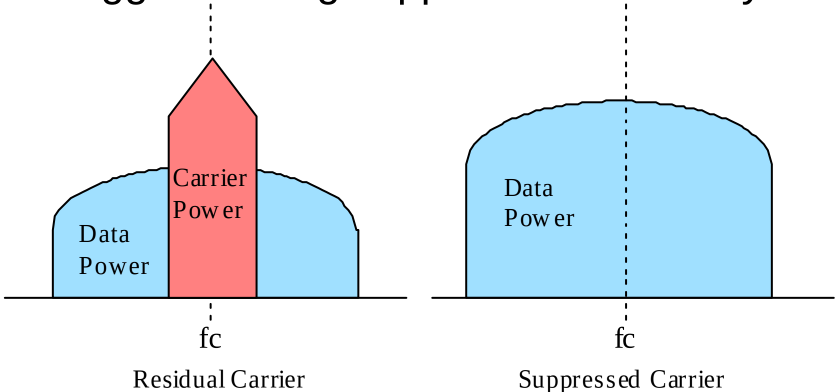
- Traditional synchronization circuits:
  - **Residual Carrier**: Utilize phase-lock Loops (PLL) to provide an accurate synchronization. (Used in NASA’s deep space comm. systems.)
  - **Suppressed-carrier:** Tracking loops such as the Costas loop require a larger SNR to track the carrier with a given accuracy.

Possible Synchronization Circuits

- **Phase-Lock Loop (PLL):**
  - Use residual carrier information inside the tracking loop to aid synchronization.
  - Loop SNR:

$$\frac{1}{\sigma_{\phi_c}^{\ 2}} = \rho_{PLL} = \frac{P_c}{N_o B_L}$$

    - B_L: Loop Bandwidth, P_c: Total Carrier Power,
    - N_o: Noise PSD $\varnothing_c$: Carrier Phase Estimation Error
  - There always exists an optimum (in the sense of *minimum average error probability*) split between Data and Carrier power .
    - If $m^2 = P_c / P_T$, typical systems require $m^2 \approx 0.1$or less [Simon96]
    - This trend suggests using suppressed-carrier systems, i.e. $m^2 = 0$



Possible Synchronization Circuits

- **Costas Loop**
  - Can track fully suppressed-carrier signals.
  - Loop SNR:

$$\frac{1}{\sigma_{\phi_c}^{\ 2}} = \rho_C \ . S_{L_C} = \frac{P_t}{N_o B_L}\left(1+\frac{1}{2R_d}\right)^{-1} = \frac{P_T}{N_o B_L}\left(1+\frac{N_o}{2P_T T_s}\right)^{-1}$$

B_L: Loop Bandwidth, P_t: Total Power, No: Noise PSD,

R_D: Input Data SNR, S_{LC}: Squaring Loss, T_s: Pulse Duration

  - Requires significantly larger *loop SNR* than a PLL to be able to track.
    - At low data SNRs, the SL can be large enough to prevent tracking.
  - For a fixed input data SNR , SL does not improve with decoder iterations.
  - For a wide input data SNR range, Costas loop systems are still more efficient (in the sense of *minimum average error probability*) than PLL circuits.
  - **Alternative Circuit:** design a suppressed carrier system for low data SNR that uses a PLL circuit instead of a Costas loop.

Information-reduced carrier-synchronization (IRCS)

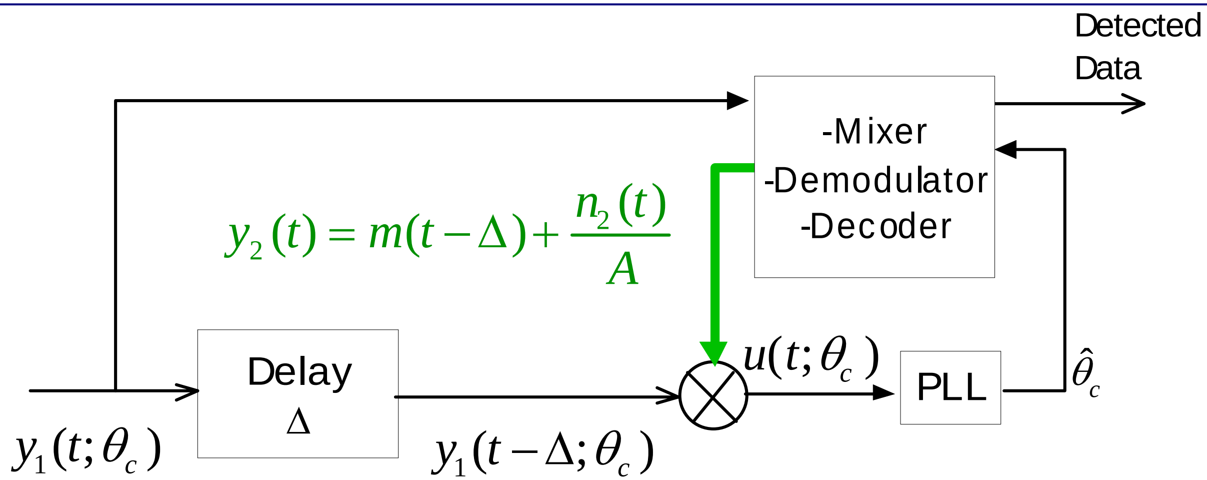
- Use a ***soft estimate*** of the instantaneous data symbol (and thus of the instantaneous phase modulation) to reduce the amount of randomness (information) in the signal being processed in the carrier loop. [Simon97]

- LDPC symbol estimates "wipe-off " modulated symbols in a ***decision directed*** loop to ***enhance the carrier information*** such that a classic PLL can provide increasingly accurate phase estimates over LDPC iterations.

- Latency penalty: tracking improves with increased iterations

- System complexity: No significant modifications to the current residual carrier recovery techniques used for BPSK/ QPSK modulation in NASA's deep-space network.

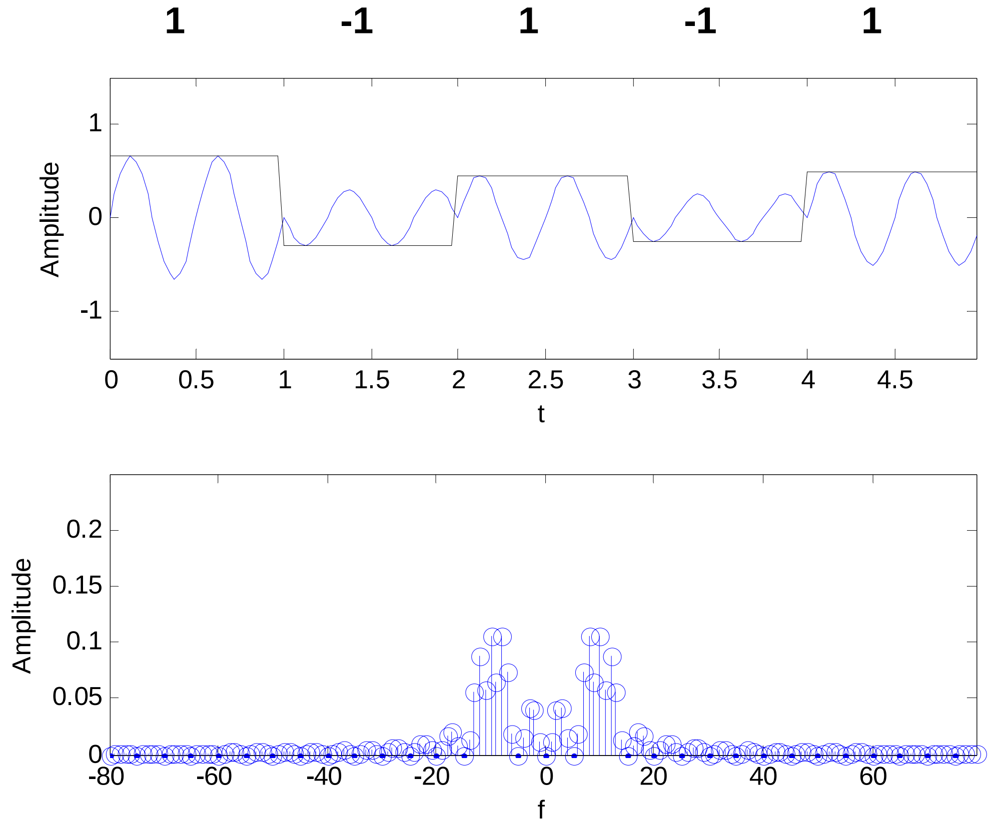
IRCS BPSK System Description



- BPSK Modulation: $m(t) = \sum_{k=-\infty}^{\infty} d_k p(t - kT_s)$
- Signal Input: $y_1(t;\theta_c) = \sqrt{2P}\,m(t)\sin(\omega_c t + \theta_c) + n_1(t)$
- AWGN Noise: $n_1(t) = \sqrt{2}\left[N_{c1}(t)\cos(w_c t + \theta_c) - N_{s1}(t)\sin(w_c t + \theta_c)\right]$
- IR Signal: $u(t;\theta_c) = \sqrt{2P}\sin(w_c t + \theta_c) + \text{ [Noise terms]}$

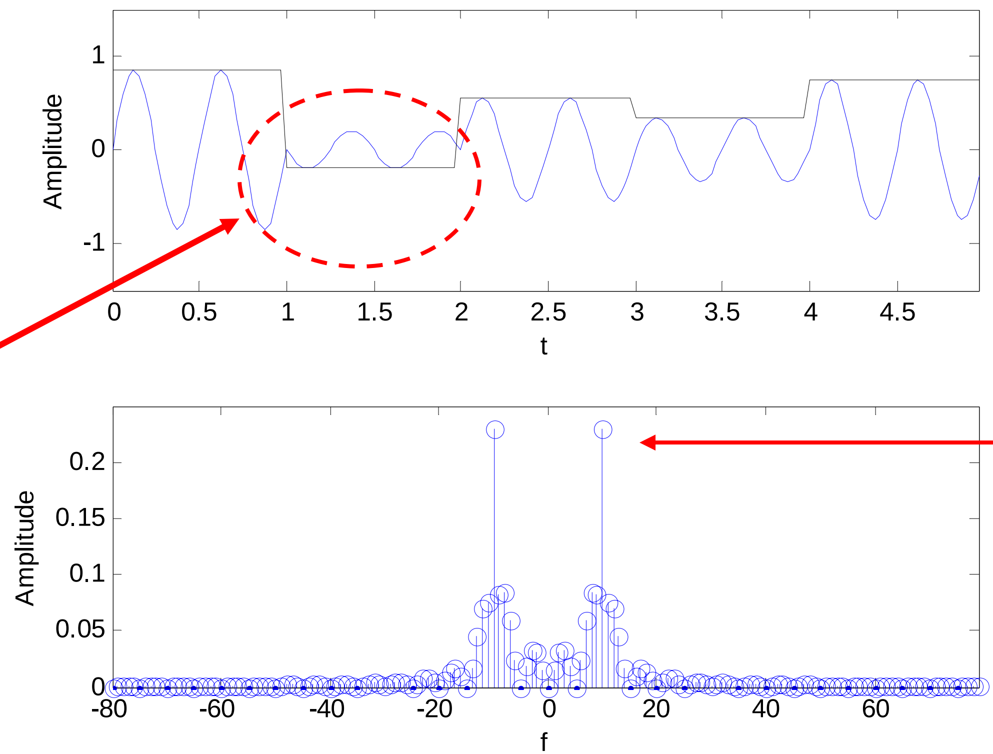
Carrier Detection Process

- Assume N=5 transmitted BPSK symbols
- Sample transmitted waveform = [1, -1, 1, -1 ,1]
- Plot shows received waveform *affected by symbol-wise noise*



Carrier Detection Process

- Modulation is removed by multiplying the received waveform by soft-estimated symbols from the decoder
- Symbol Information randomness is reduced
- Plot shows “IR” waveform after the first iterations

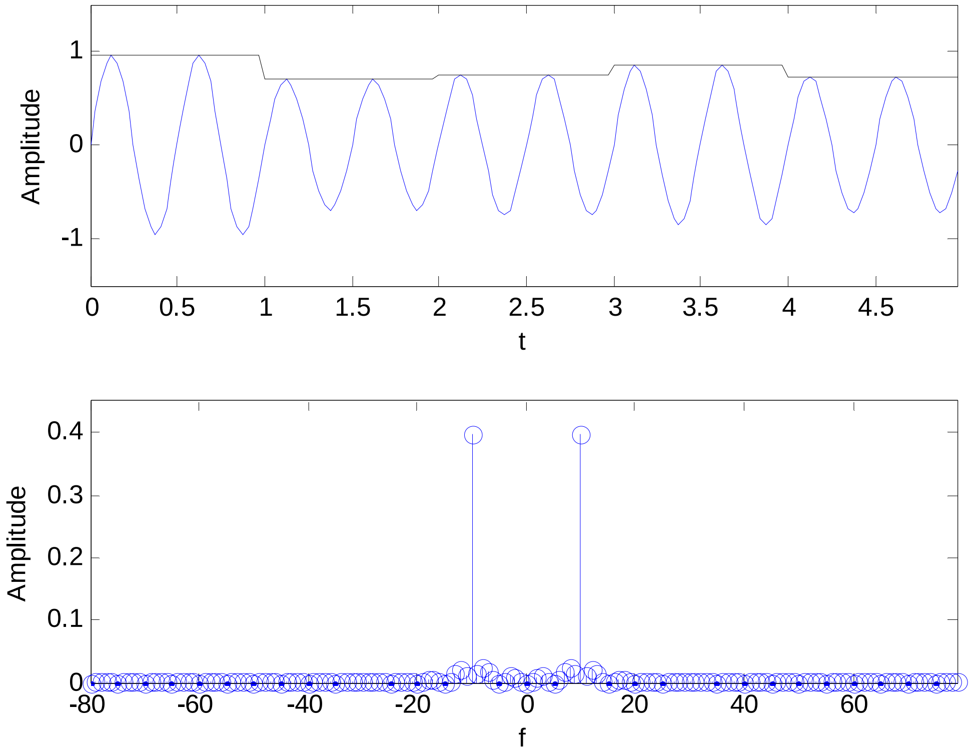


- **Soft Symbol information may still be incorrect**
- **Incorrect information has low reliability**

Unmodulated frequency spectrum begins to show the presence of a carrier tone.

Carrier Detection Process

- As the number of iterations increase, soft-symbol estimation becomes more accurate.
- Frequency spectrum has a distinctive tone that a PLL based circuit can now track.



Proposed Synchronization Circuit

- **Information Reduced Carrier Synchronization (IRCS)**
  - Can track fully suppressed-carrier signals
  - Loop SNR:

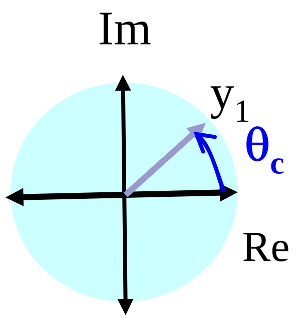
$$\frac{1}{\sigma_{\phi_c}^{2}} = \rho_{IRCS} \cdot S_{L_{IRCS}} = \frac{P_T}{N_o B_L}\left(1+\frac{\sigma^2}{A^2}\right)^{-1} = \Big|_{\text{LDPC}} \frac{P_T}{N_o B_L}\left(1+\frac{2}{A}\right)^{-1}$$

    - B_L: Loop Bandwidth, P_t: Total Power,
      $S_{L\ IRCS}$: Squaring Loss, A: Estimated Signal Amplitude
  - The ratio $\frac{A^2}{\sigma^2}$ represents the decoder soft-estimate data SNR.
  - *Symmetry condition:* For decoding of LDPC and turbo codes $\sigma^2=2A$. [Chung01]
  - Decoder data SNR increases with iterations causing:
    - $S_{L\ IRCS} \rightarrow 1$
    - Loop SNR approaches PLL performance using the total transmitted power for carrier estimation

Loop SNR Summary

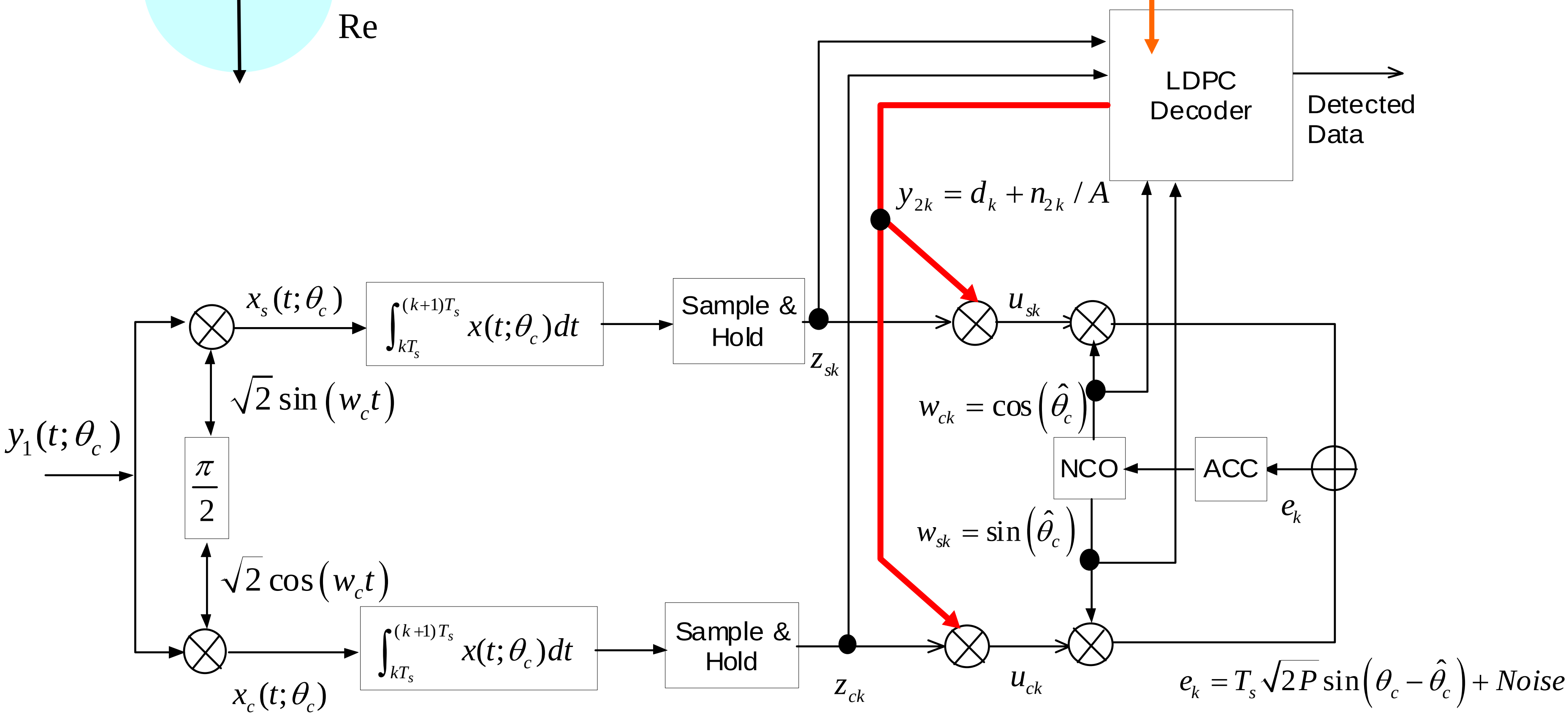
- PLL: $$\frac{1}{\sigma_{\phi_c}{}^2} = \rho_{PLL} = \frac{P_c}{N_o B_L}$$
  - Loop SNR exhibits No squaring loss
  - Utilizes carrier power for carrier estimation
- Costas Loop: $$\frac{1}{\sigma_{\phi_c}{}^2} = \rho_C \; .S_{L_C} = \frac{P_t}{N_o B_L}\left(1 + \frac{1}{2R_d}\right)$$
  - SL is independent of the iteration process, for a given SNR.
  - Suppressed carrier scenario
- IRCS: $$\frac{1}{\sigma_{\phi_c}{}^2} = \rho_{IRCS} \; .S_{L_{IRCS}} = \frac{P_T}{N_o B_L}\left(1 + \frac{2}{A}\right)^{-1}$$
  - SL approaches unity as the number of LDPC iterations increase
  - Suppressed carrier scenario

BPSK Digital Circuit Implementation



LDPC LLR Inputs:

$$Q_k = \frac{2}{\sigma_{LLR}^2}\left(z_{sk}w_{ck} + z_{ck}w_{sk}\right) \quad \text{where} \quad \sigma_{LLR}^2 = \frac{\left(\sqrt{PT_s}\right)^2}{2\dfrac{E_s}{N_o}}$$



$$x_c(t;\theta_c) = \sqrt{PT_s}\,m(t)\sin(\theta_c) + Noise(t;\theta_c)$$

$$x_s(t;\theta_c) = \sqrt{PT_s}\,m(t)\cos(\theta_c) + Noise(t;\theta_c)$$

$$z_{ck} = d_k \sin(\theta c) + Noise$$

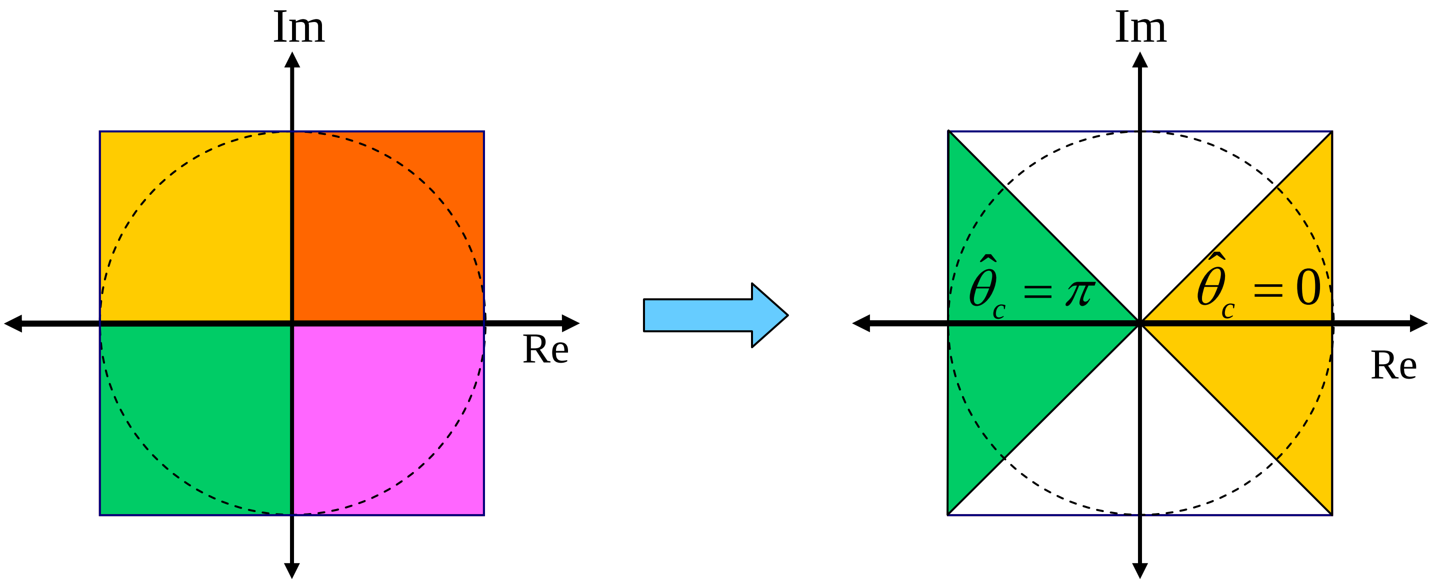
$$z_{sk} = d_k \cos(\theta c) + Noise$$

$$u_{ck} = A\sin(\theta_c) + Noise$$

$$u_{sk} = A\cos(\theta_c) + Noise$$

BPSK : Algorithm Initialization

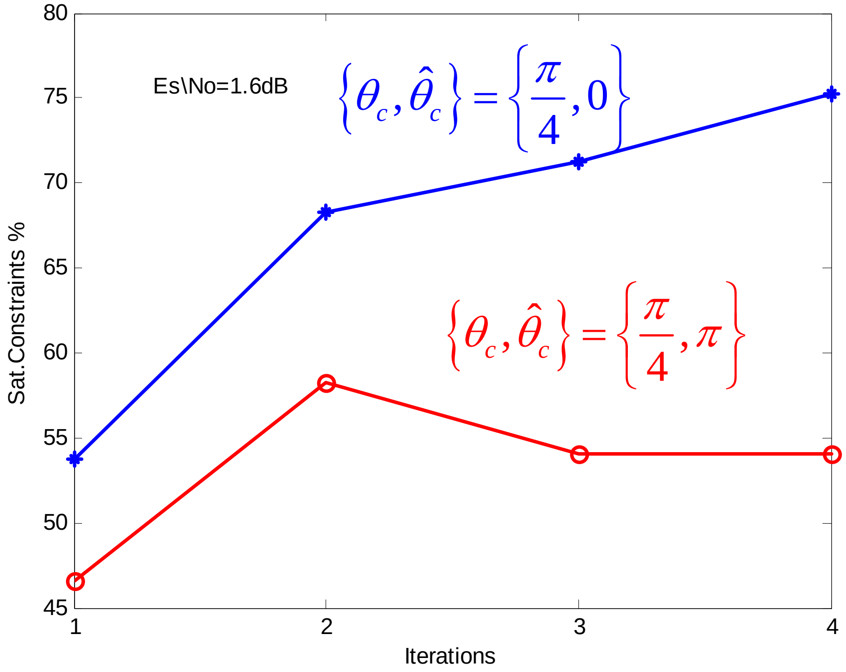
- **<u>Step 1:</u>** Resolve initial phase ambiguity
- Measure average power across a single codeword of the signals z_c and z_s.
  - Choose component with *higher power* to initialize the phase estimation process
  - An error of 180 degrees may remain

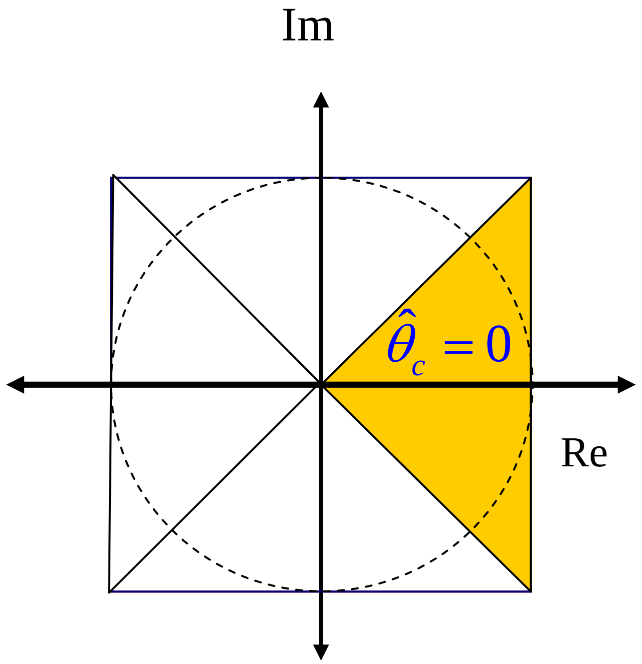


π Ambiguity

BPSK : Pilotless Phase Ambiguity Correction

- <u>Step 2:</u> Remove possible $180°$ offset
  - Run a single PLL pass
  - Run up to 4 LDPC iterations and choose the orientation that produces the maximum percentage of satisfied constraints on **odd degree check nodes** (even degree checks remain satisfied after a π rotation of its inputs)





BPSK Main Decoding Algorithm

- <u>Step 3:</u>

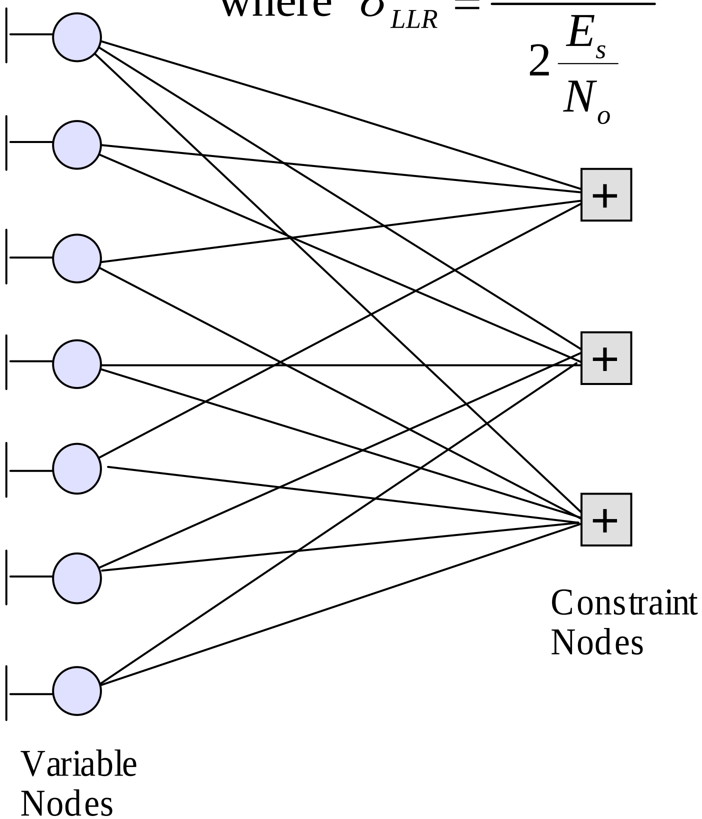
  For i=1 to ***Max_Iterations***

  1. Estimate Carrier Phase Offset
  2. For j=1 to ***LDPC_iter***
     - Update Variables
     - Update Constraints
  3. Update Variables
  4. Go to 1

- Performance plots in the next slides are shown for *LDPC_iter* ={1,2}
- BER/FER performance starts to degrade for cases where phase estimates are computed after a higher number of decoder iterations.

$$Q_k = \frac{2}{\sigma^2_{LLR}}\left(z_{sk}w_{ck} + z_{ck}w_{sk}\right)$$

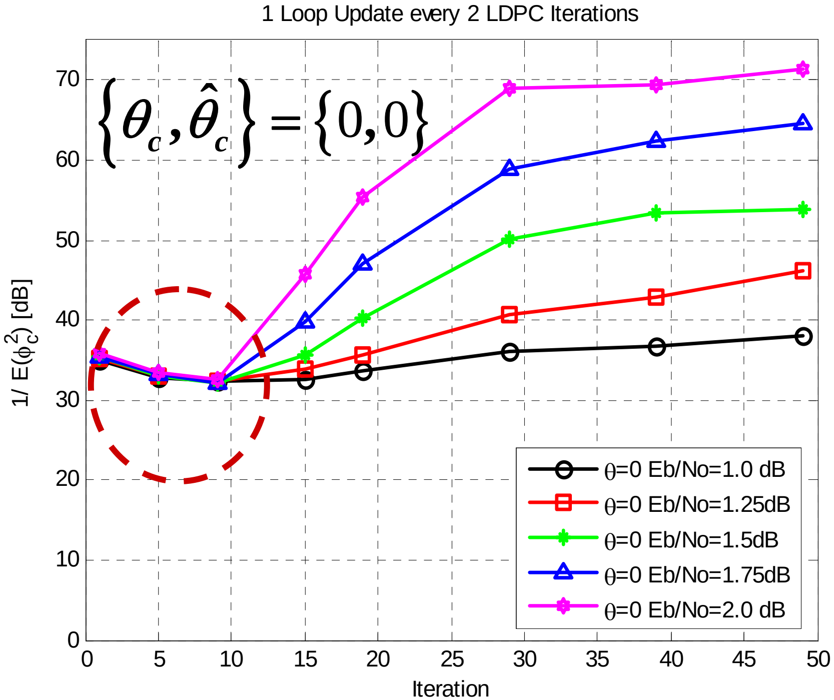
$$\text{where} \quad \sigma^2_{LLR} = \frac{\left(\sqrt{P}T_s\right)^2}{2\frac{E_s}{N_o}}$$

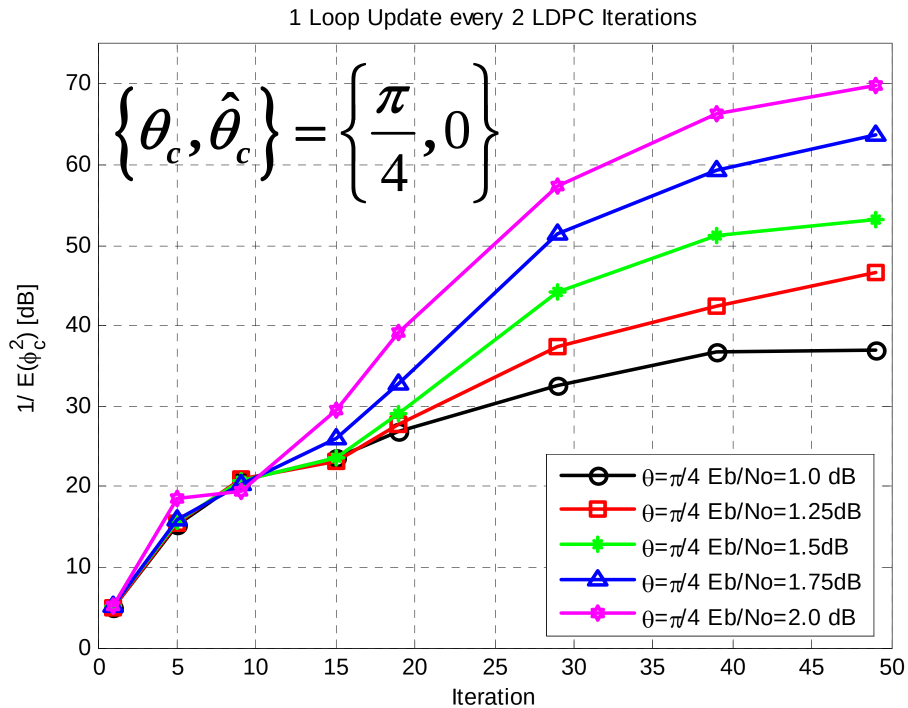


Experimental Results: Loop SNR

- Plot shows loop SNR vs Iterations. θ_c=0° and θ_c=45°

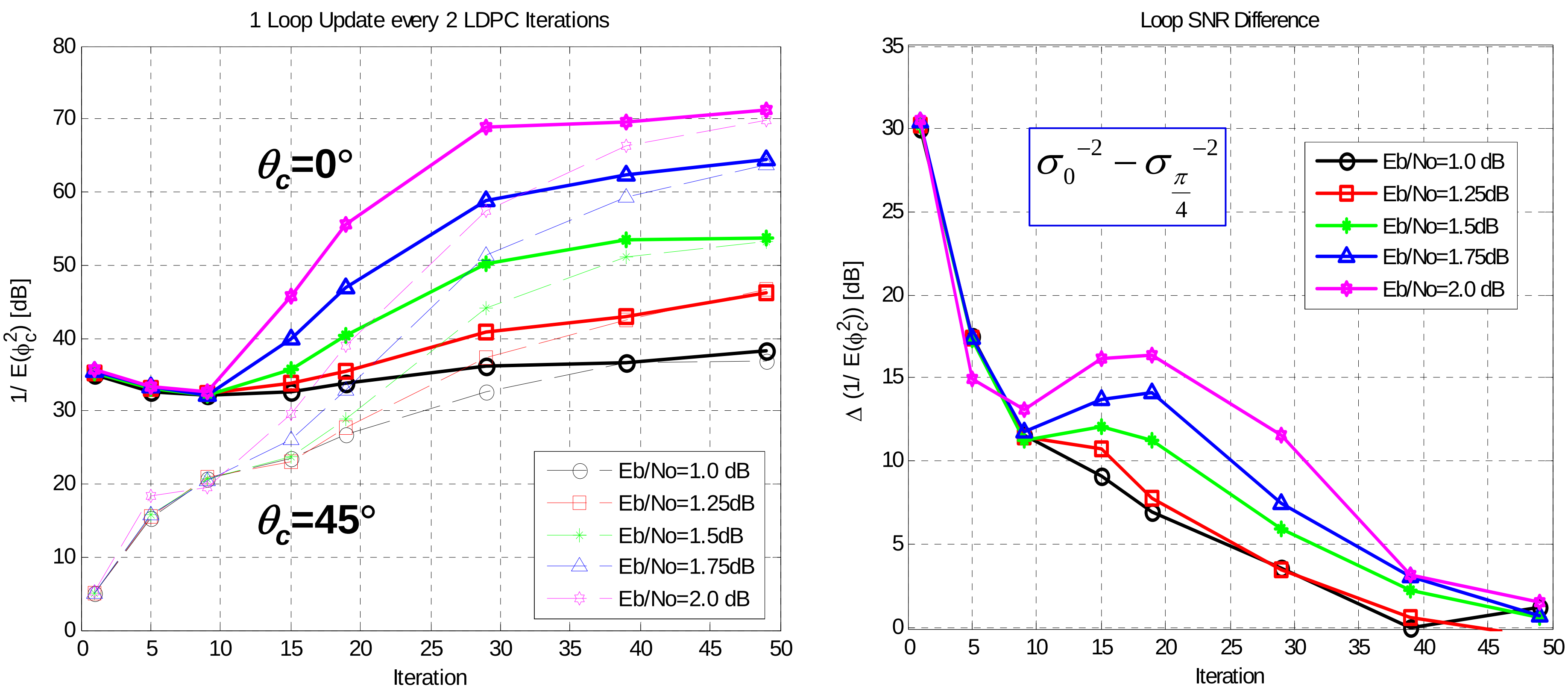
$$\text{Loop SNR} = \frac{1}{\sigma_{\phi c}^2}$$





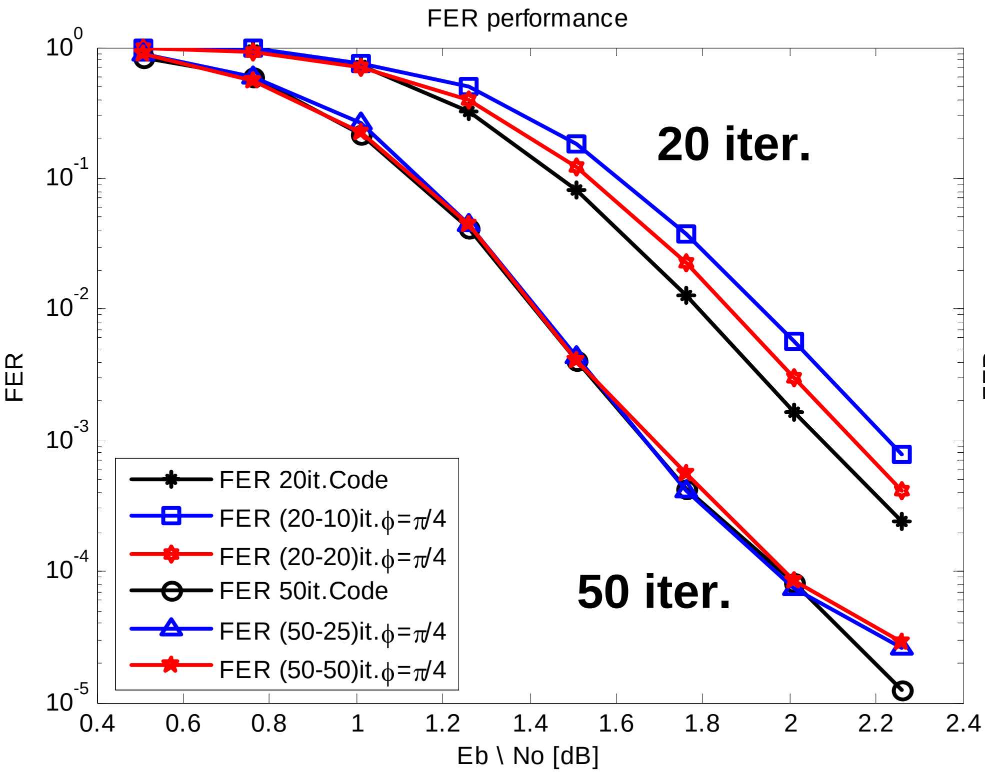
- Note the curious performance for the θ_c = 0° case.
- In this region the initially correct PLL's phase estimate is affected by poor initial LDPC soft-symbol estimates.
- Both LDPC estimates and loop-SNR dramatically improve after the 10th iter.

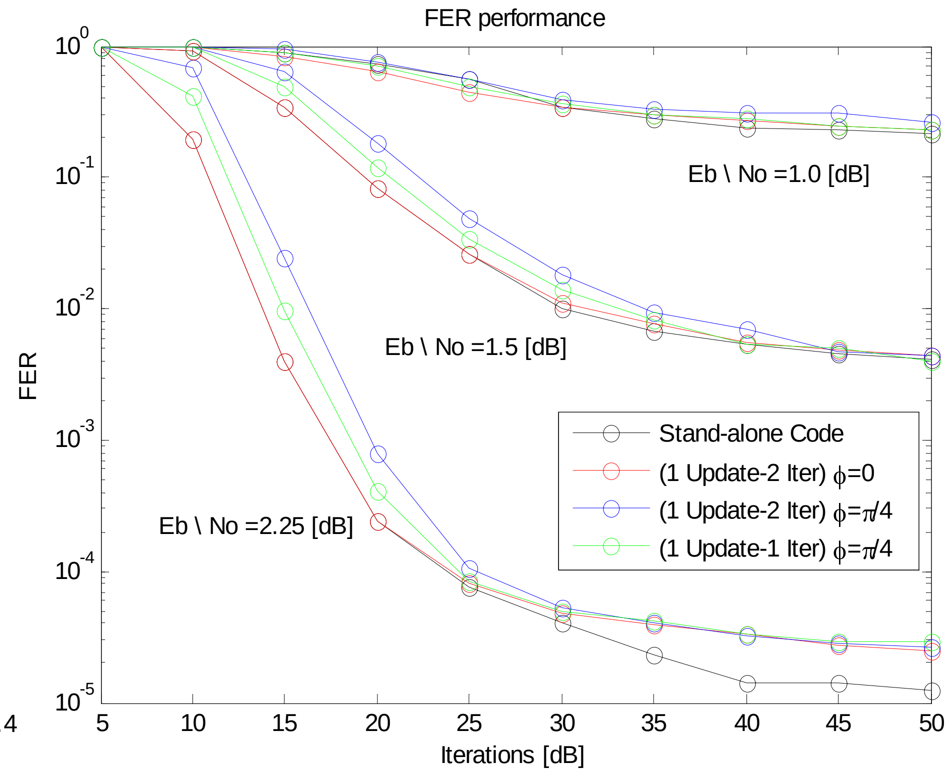
Experimental Results: Loop SNR



- ❑ Steady State is reached after 50 iterations
- ❑ As we will see in the next slide this means that
  - ❑ Some loss occurs with a reduced number of iterations.
  - ❑ After 50 iterations, a small marginal degradation in loop-SNR remains

BPSK Frame Error Rate Performance





20 Iterations

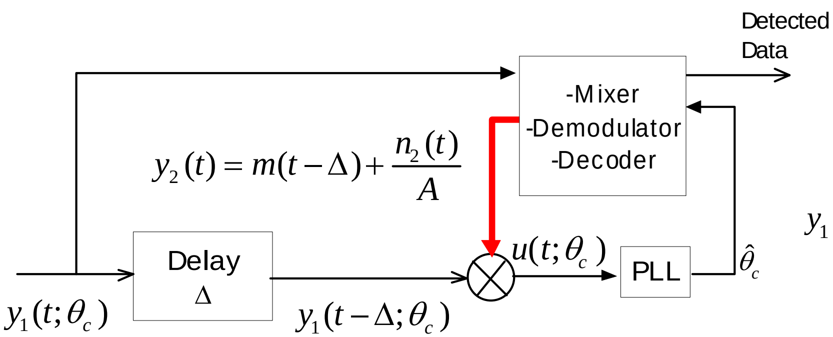
- Loop did not reach Steady State
- Performance loss at a FER of 1e-3 is
  - 0.15dB with a (20-10) = (1 Loop update every 2 LDPC iterations) scheduling
  - 0.07dB in the (20-20) = (1 Loop update every 2 LDPC iterations) scheduling

50 Iterations

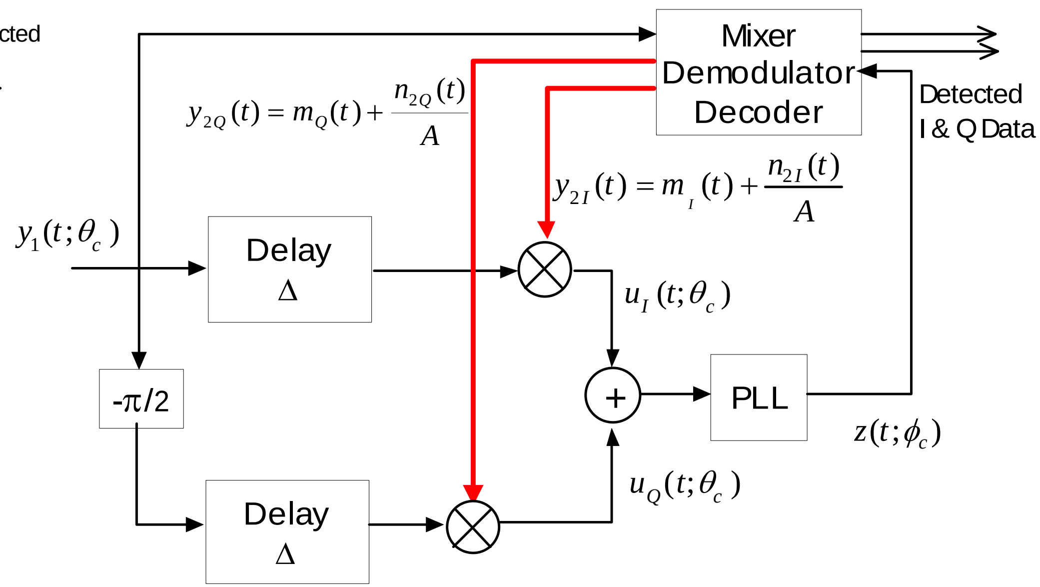
- Loop in Steady State
- Small performance difference after 50 iterations due to loop-SNR marginal degradation

QPSK Analog Circuit Description

BPSK



QPSK



- The QPSK IRCS carrier recovery circuit follows the same principles as its BPSK counterpart
- Symbol feedback is now done for the real and imaginary signal components

Squaring Loss (SL) for QPSK systems

- Recall the BPSK SL expression:

$$S_L \triangleq \left(1+\frac{\sigma^2}{A^2}\right)^{-1} = \left(1+\frac{2}{A}\right)^{-1}$$

- For our QPSK system :

$$S_L \triangleq \left(1+\frac{(1+R_d)\sigma^2}{A^2}\right)^{-1} = \left(1+\frac{2(1+R_d)}{A}\right)^{-1}$$

where the noise variance factor $(1+R_d)$ (R_D: Input Data SNR) comes from the presence of a quadrature (signal x noise) term. [Simon06]

- The penalty in performance due to the R_d term becomes insignificant for low symbol SNR scenarios.

- No 4th order (signal x noise) or (noise x noise) in the loop as in QPSK Costas or hard-decision IRCS loops.

Conclusions

- We have demonstrated a method for improving the carrier synchronization function for iterative BPSK using soft output information from an LDPC decoder .
- Motivation is to overcome the performance loss due to a noisy signal reference at low SNRs, characteristic of suppressed carrier loops such as the Costas loop.
- Steady state operation is reached after around 45 LDPC iterations.
- Performance degradation with respect to the perfect phase information case, in steady state and with a proper loop update schedule, is smaller than 0.1dB.

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