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High Speed Channel Coding Architectures for the Uncoordinated OR Channel

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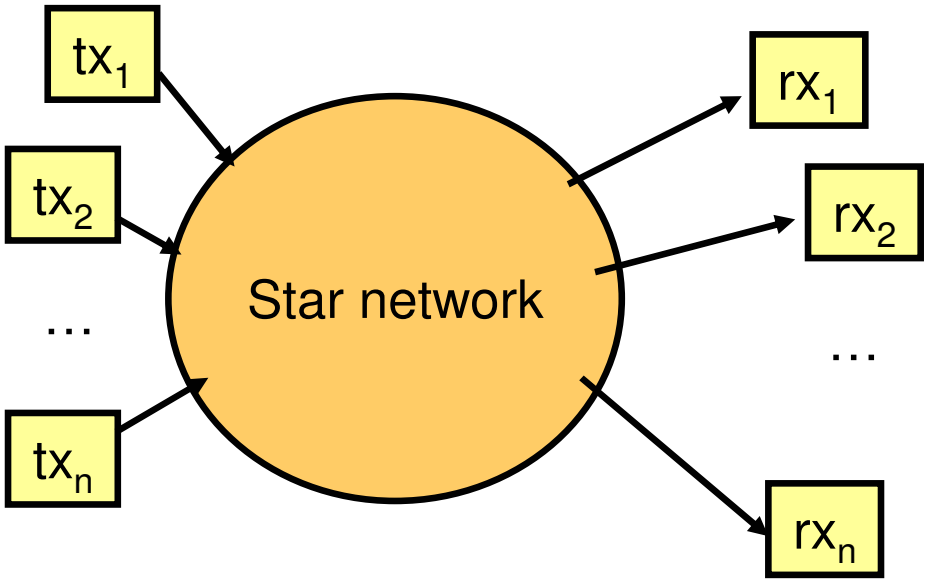
System Model

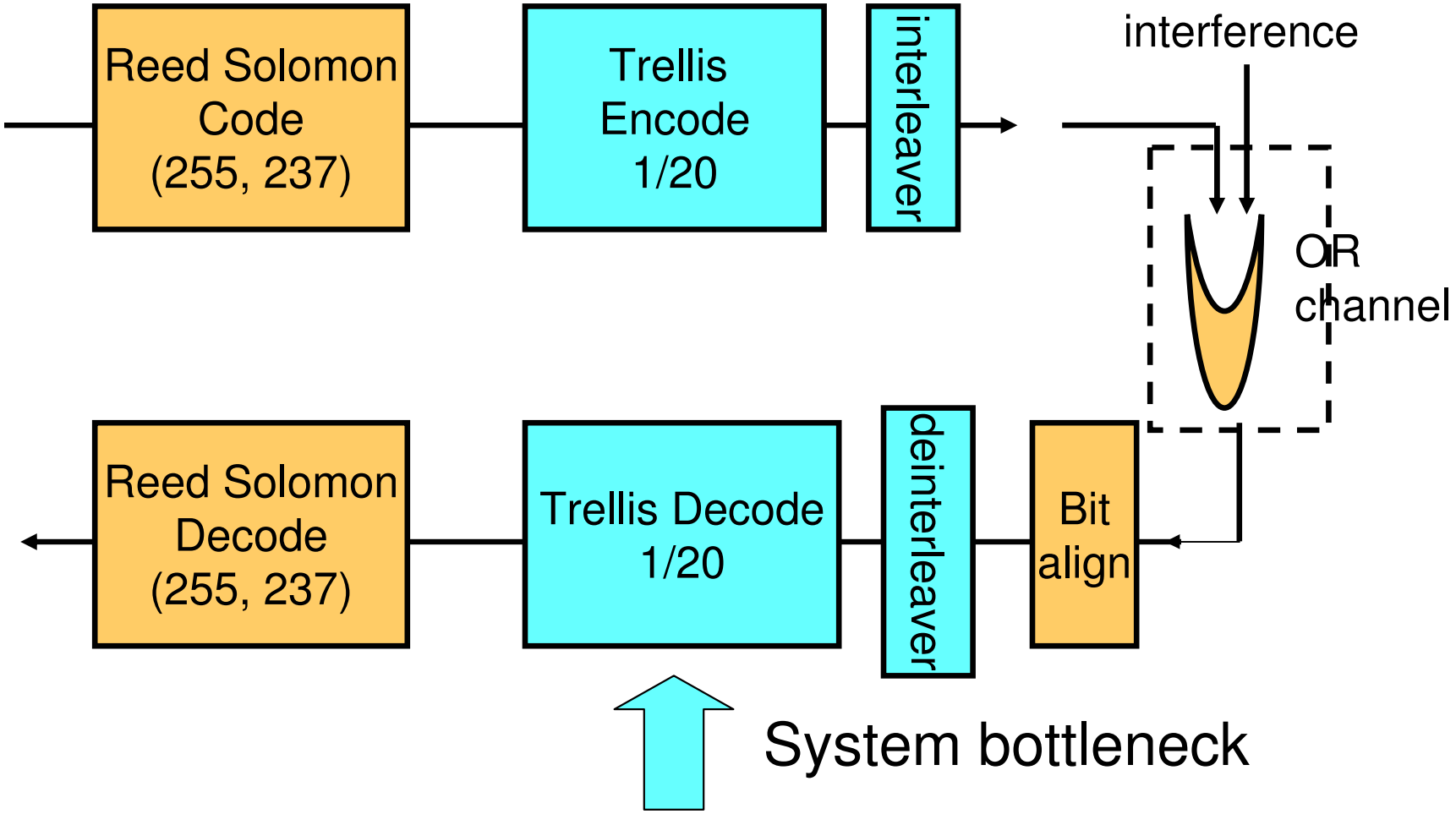


- Uncoordinated access: transmitters can transmit at any time with any code (chosen from a family) without informing anyone except the desired receiver

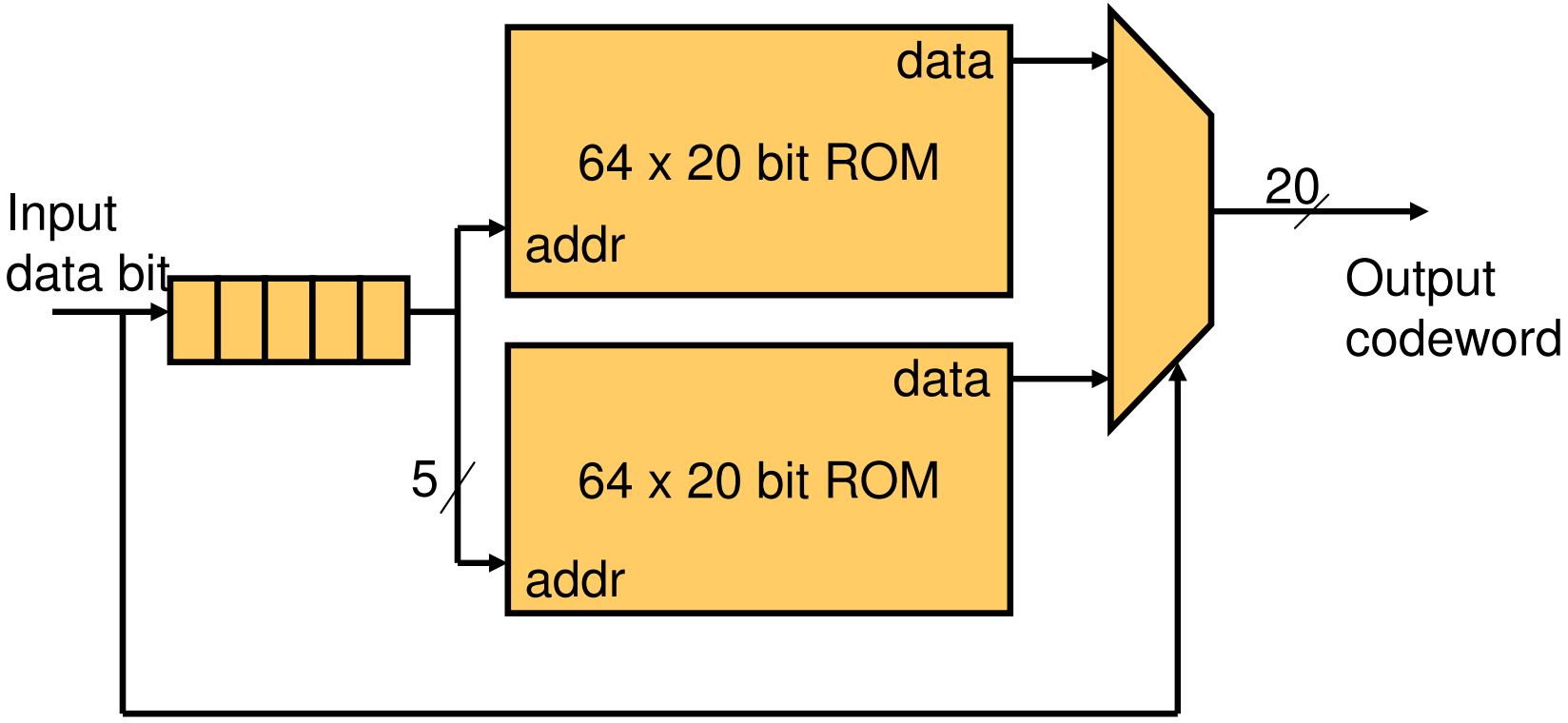
- Optical Channel:
  - 1 : light is transmitted
  - 0 : no light is transmitted

- Channel Interference: Noncoherent interference is assumed
  - 1 : bit will always be correctly received
  - 0 : bit can be corrupted by interference

Channel Coding Architecture

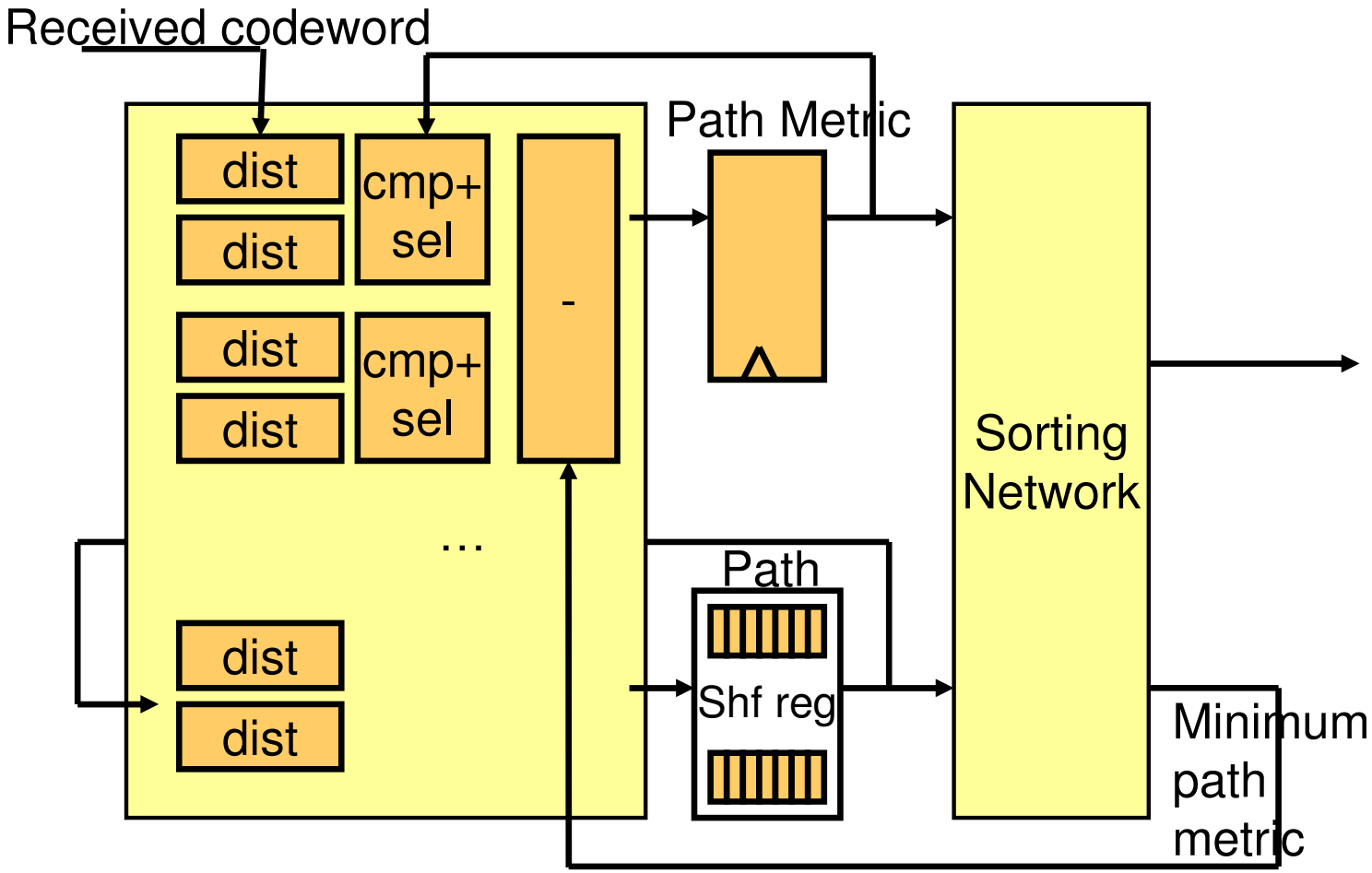


Trellis Encoder



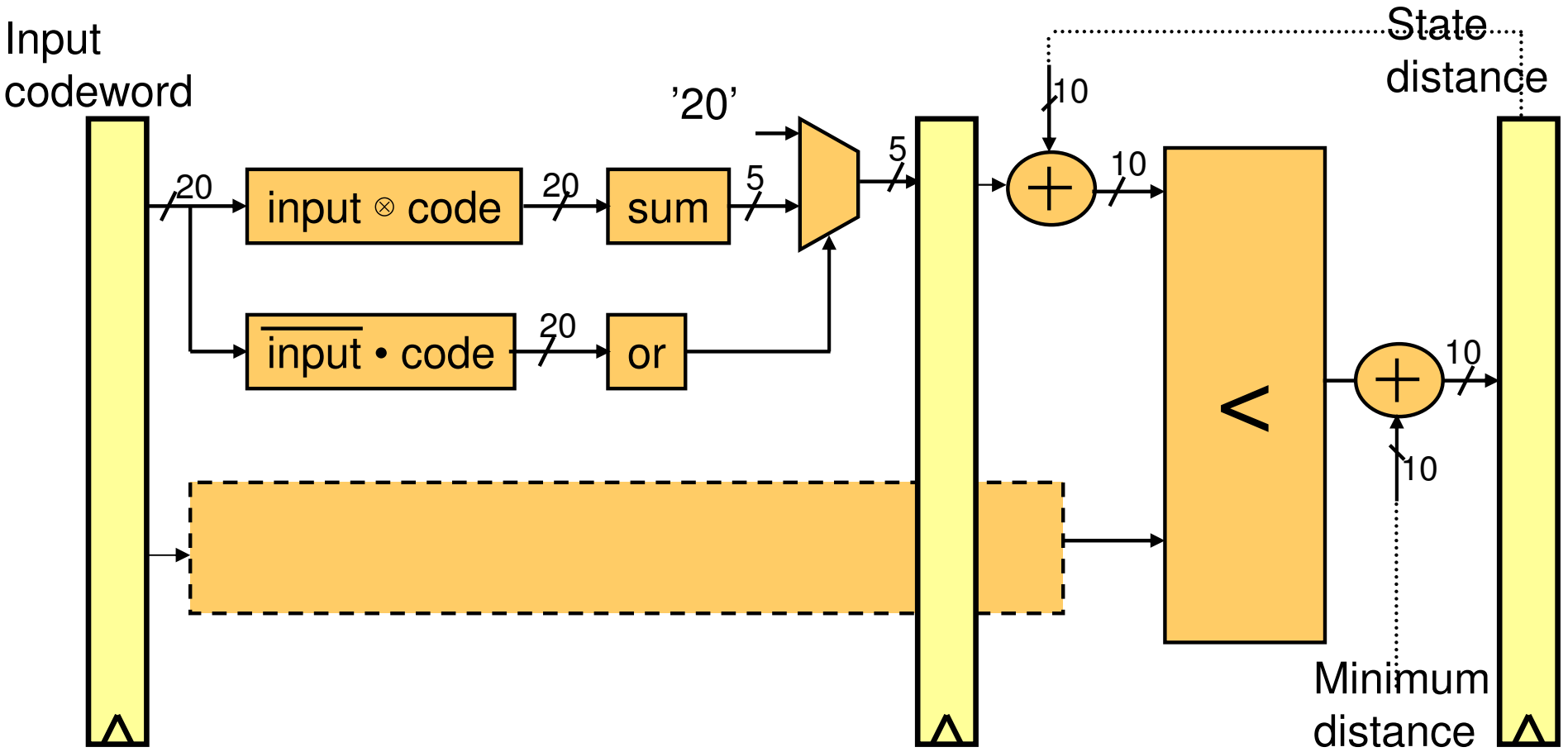
- Trellis code uses 20 bit words and 64 states
- Fast architecture consists of a shift register to index the codeword memories

Viterbi decoder architecture



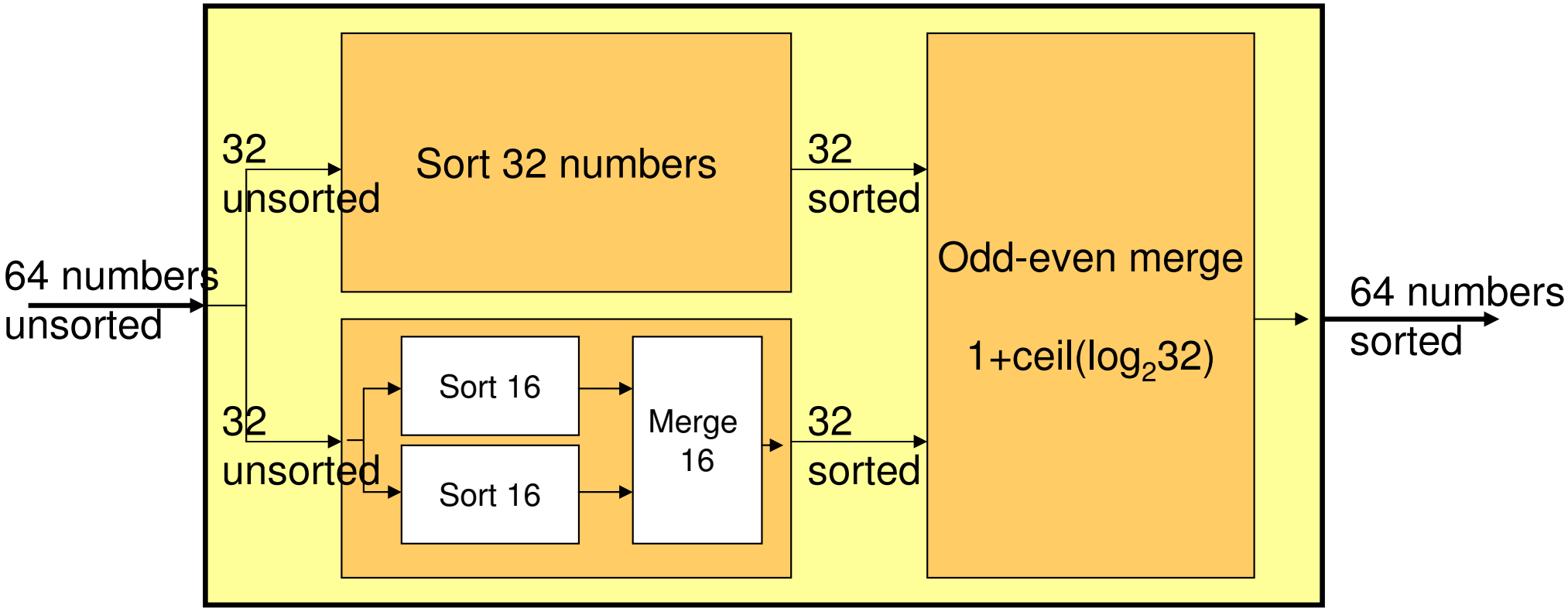
- All path metrics are calculated and sorted in parallel
- Operations are pipelined to achieve maximum throughput

Calculation of Path Metric



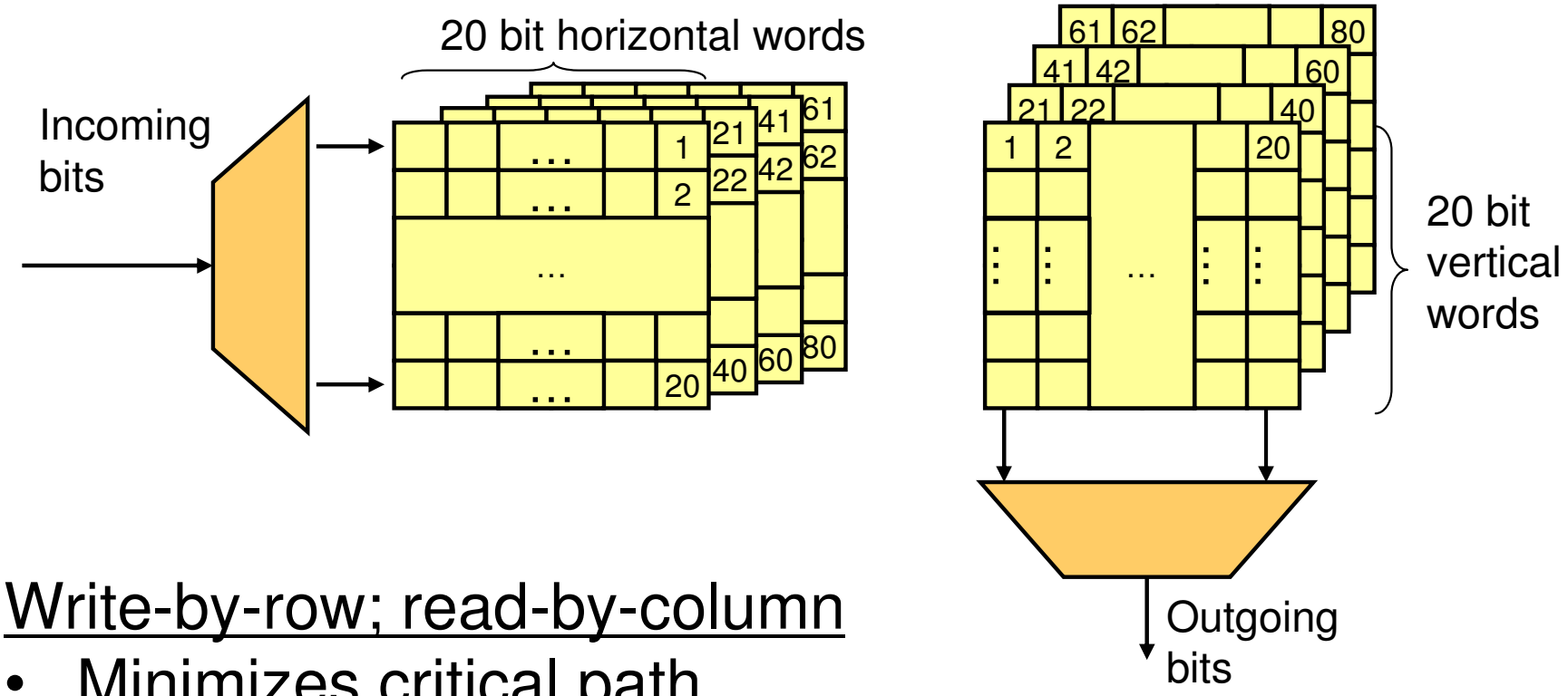
- Special logic is used to calculate path metric of OR channel
- Feedback path of accumulated path metric limits throughput

Sorting Network



- 64 path metrics are sorted using Batcher's algorithm
- Minimum time algorithm minimizes delay in the feedback path

Interleaver Architecture



Write-by-row; read-by-column

- Minimizes critical path
- Provides near zero cross correlation
- $(80!)^2$ different permutations possible

Implementation Results

VirtexII-Pro FPGA	Size (slices)	Critical Period (ns)
Transmitter		
Reed Solomon Encoder	189	5.3
NL-TCM Encoder	34	3.4
Interleaver	3389	7.7
Receiver		
Reed Solomon Decoder	3686	9.0
NL-TCM decoder	10504	10.3
Interleaver	3384	7.7

0.18um ASIC	Size (Kgates)	Critical Period (ns)
Transmitter		
Reed Solomon Encoder	3	1.6
NL-TCM Encoder	9	1.3
Interleaver	39	3.7
Receiver		
Reed Solomon Decoder	29	10.3
NL-TCM decoder	239	1.4
Interleaver	39	3.7

- FPGA able to operate at 2 Gbps channel throughput
- ASIC able to operate at 5.4 Gbps channel throughput

Conclusions

- Novel channel codes for the optical OR channel requires design of new architectures
- For optical throughputs, designs must parallelize and pipeline aggressively

  Viterbi
  - Duplication of path metric calculation
  - Efficient and pipelined sorting network

  Interleavers
  - Write-by-row, Read-by-column strategy
- 2.0 Gbps achieved in FPGA and 5.4 Gbps achieved in ASIC

More info at http://www.ee.ucla.edu/~herwin/ocdma2
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