Pb-free Solder for Electronic, Optical, and MEMS Packaging Manufacturing

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Review of Electronics Packaging Issues in ITRS 2001

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Based on the Assembly & Packaging chapter In ITRS 2001

Outline

- ITRS: Worldwide S/C industries efforts
- Packaging challenges
- Packaging requirements
  - Embedded passives
  - Optoelectronics packaging
  - MEMS packaging
  - RF & mixed signal packaging
  - Flip chip packaging
- Pb-free solder benefits and challenges
- Conclusions

ITRS: Worldwide S/C Industries Efforts

- Extremely expensive S/C fabs ($ 2^+ billions)
  - All tools up & running in minimum time span
  - All materials and consumable available
  - Technologies and designs ready for production
  - Packaged ICs meet perf. & reliab. targets
  - Packaged ICs within targeted manuf. cost
- Aggressive and realistic 15-year roadmaps
  - Focuses on common goals (manufacturing readiness)
  - Addresses environmental concerns (Pb-free solder, … etc.)
- Worldwide participation

Packaging Challenges

- Organic substrates: Tg, dielectric loss, planarity & warpage at processing temperature, moisture absorption, …
- Underfill for FC pkg: adhesion, moisture absorption, higher operating temperature (automotive applications)
- Chip, packaging & substrate co-design: digital & analog mixed signal, transient thermal analysis, thermo-mechanical analysis, electrical power disturb, signal integrity, EMI, commercial EDA supplier support
- Impact of Cu / low-k on packaging: wire bond, FC and underfill on Cu & low-k wafers (adhesion, material strength, … etc.)
- Pb-, Sb- & Br-free packaging materials

Embedded Passives Challenges

- Need cost, performance, or functionality advantages w.r.t. discrete or on-chip passives implementation
- Need sheet resistivity stability through product life
- On-chip decap on Si ICs & top-surface decap on III-V ICs
- Embedded inductors have high-Q value
  - Design to avoid flux linkage and coupled noise concern
- Embedded antennas, baluns, filters, resonators are likely, since they are too large to integrate into IC.

Optical Interconnect & Packaging Challenges

- Optical fiber long-haul & city-wide networks
  - *2.5 Gb/s* to *10 Gb/s* to *40 Gb/s* to *160 Gb/s*
  - *Small electrical signal* from optical receivers
- Low cost solution for access networks
  - Lower data rate
  - Non-hermetic packaging
  - Alignment relaxation & automatic assembly (eliminate pig-tailed components, …)
- Extremely low cost for fiber-to-curb (or to-home)
  - Competitive solutions: xDSL, cable, LMDS, MMDS, …

Optical Fiber Backbone

- High precision & high power optical devices
  - Passive devices: AWG, filter, splitter, cross-connect, …
  - Active devices: laser, modulator, detector, attenuator, …
- *Active temperature control* to assure
  - Correct wavelength (laser diode)
  - Correct wavelength spacing (adjacent optical waveguides)
- *Alignment* between single mode fiber to laser diode or photonic detector
  - *High precision placement*
  - *Controlled die adhesive curing* at assembly
- Hermetic packaging (device surface, optical path, …)

MEMS Packaging

- MEMS applications:
  - Automotive, medical, telecommunications, consumer electronics, …
- Conventional packaging issues:
  - Environmental protection, signal integrity, mechanical support, thermal management, …
- Special packaging issues:
  - Signal & energy changing elements
  - Absolutely no moisture in certain MEMS devices
  - Access to chemical or biological environments in others
  - Testing of packaged MEMS devices

RF & Mixed Signal Packaging

- Prevalent applications of low cost mobile products
- Extending performance of WB packages by design opimization
- Further improvements needed:
  - Lower dielectric loss
  - Flip chip package to minimize EMI & shielding cost
  - Direct conversion (no IF filter) radio architecture
  - Control of electrical parameter variability at higher frequency
  - Integrated electrical simulation capability (chip & package) to drive down design cycle time
  - MEMS for filter, switch, oscillator, …

Broadband Cross-point Switches

- 12.5 Gbps 20 x 20 asynchronous crosspoint switch
  - 80 high data rate I/Os for 40 differential pairs
  - Using NRZ (non-return to zero), signal level may switch from 1.25E9 to 1.25E10 times per second (in contrast to narrow band tuning in RF)
  - Input capacitance (including ESD) less than 0.4 pF
- Request inclusions in ITRS 2003
  - Design-TWG to provide broadband roadmap
  - PIDS-TWG (devices) to provide ESD roadmap
  - Test-TWG to address testing issues & protection
  - AP-TWG to address large number of high data rate I/Os

Flip Chip Packaging & Tradeoffs

- WB (peripheral I/O) packaging
  - *Lower cost* substrate
  - *Smaller IC size* for *low I/O* applications
  - Trading *lower cost packaging substrate* for *larger chip* for *intermediate I/O* applications
- FC (area array I/O) packaging
  - Higher density (*higher cost*) substrate
  - Voltage/ground pads in *chip interior* for *high power* applications
  - *High I/O* applications
  - Wafer-level packaging (*WLP*) in *low I/O* applications
  - *Minimize EMI* for *RF* applications (*low I/O*)

ITRS Technology Node - Year of Production

- ITRS 2001 Executive Summary (page 55)
  - Year of PRODUCTION is the year in which leading chip manufacturers begin shipping volume quantities (10K per month) of product manufactured with qualified production tooling and processes and is followed within three months by a second manufacturer.

Chip-to-Package Interconnect

Year	2001	2002	2003	2004	2005	2006	2007
Technology Node	130nm	115	100	90nm	80	70	65nm
Chip Interconnect Pitch (um)							
Wire bond---ball	45	35	30	25	20	20	20
Wire bond---wedge	40	35	30	25	20	20	20
TAB	40	40	40	40	30	30	30
Flip chip (area array) for Cost-performance and High-performance	160	160	150	150	130	130	120
Flip chip for Handheld, Low-cost, and Harsh	150	130	120	110	100	90	80

I/O Pad Allocation and Chip Current

- Flip-chip I/O pads (*WB not for high power chip*)
  - Signal pads (20%) at 0.2 mm pitch
  - Voltage pads (40%), interior pads at 0.28 mm pitch
  - Ground pads (40%), interior pads at 0.28 mm pitch
- Chip pad passivation opening: 0.08 mm dia.
  - 1.34% of chip area for signal passivation opening
  - 2.68% of chip area for voltage passivation opening
  - 2.68% of chip area for ground passivation opening (*70 Amperes for 10 mm x 10 mm chip*)
- Sn/Ag/Cu (Pb-free) solder will help

Electromigration Current Density

- On-chip interconnect
  - *1.1E6* Amp/cm^2 (2002 needs in ITRS 2001)
  - 1.3E6 Amp/cm^2 (2003 needs in ITRS 2001)
  - 1.5E6 Amp/cm^2 (2004 needs in ITRS 2001)
  - 1.7E6 Amp/cm^2 (2005 needs in ITRS 2001)
  - 1.9E6 Amp/cm^2 (2006 needs in ITRS 2001)
  - 2.1E6 Amp/cm^2 (2007 needs in ITRS 2001)
- Chip-to-package interconnect
  - Eutectic Sn/Pb solder
  - *2.6E3* Amp/cm^2 (ITRS 2000 update)
  - Pb-free solder ?????

Current Limits of 63Sn/37Pb Solder Bumps

(based on ITRS 2000 update)

Bump Pitch	Passivation Opening (chip pad)	Current Limit for 100,000 hour MTTF at Bump Temperature of 100 C
250 um	85 um	150 mA
200 um	80 um	130 mA
150 um	65 um	90 mA

Pb-free Solder Benefits for FC Packaging

- Eliminate alpha-particle containing solders (Pb)
  - Cosmic ray still a concern (low flux density)
    - Protons
    - Cosmic alpha particles
    - Neutron-silicon atom recoil
  - Solutions:
    - ECC to correct single error (either hard or soft error)
    - System design to correct 1 hard error + 1 soft error & to scrub off soft errors in main memory at regular interval
- Improve current density (electromigration)

Pb-free solder Challenges

- Higher reflow temperature (chip to BGA as well as BGA to PWB)
  - Compatible PWB & PBGA
  - Comparable cost with standard PWB & PBGA
- Higher Sn content
  - Less ductile than Pb (solder with 90% Pb or higher)
  - Different or thicker barrier layer in UBM

Conclusions

- Low cost packaging of optical components for mass market
- Special packaging issues for different MEMS applications
- Further improvements needed in RF and broadband applications
- Pb-free solders bring benefits and challenges