Nonlinear Time and Temperature Dependent Analysis of the Lead-Free Solder Sealing Ring of a Photonic Switch

J. Lau, Z. Mei, S. Pang, C. Amsden, J. Rayner and S. Pan

Agilent Technologies, Inc.
5301 Stevens Creek Blvd.
Santa Clara, CA 95052

PURPOSES

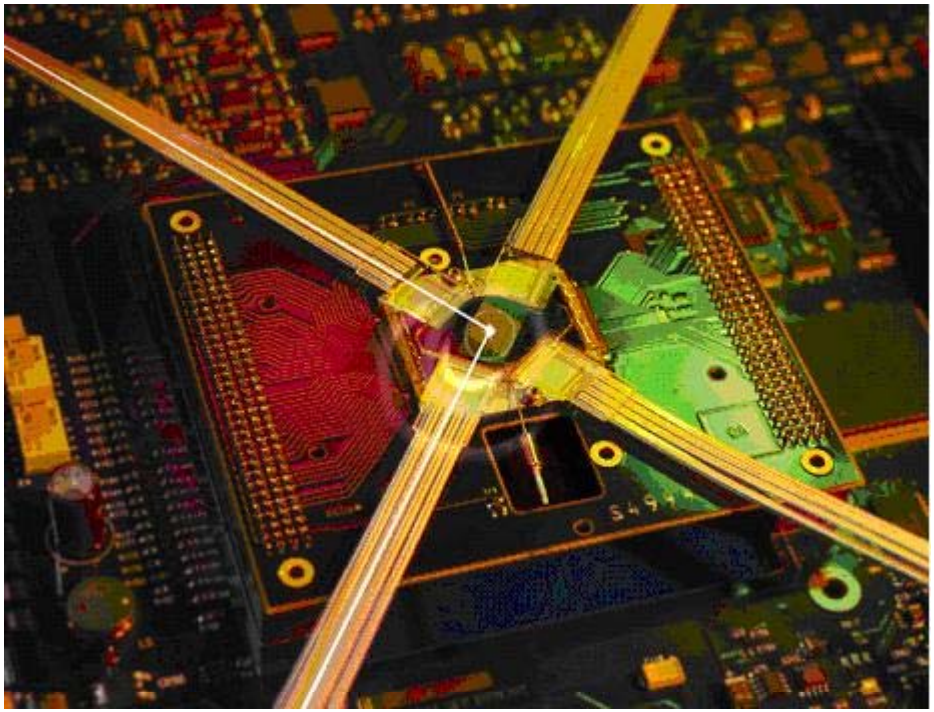
To determine the thermal-fatigue life of the lead-free solder sealing ring of a photonic switch under shipping/storing/handling conditions.

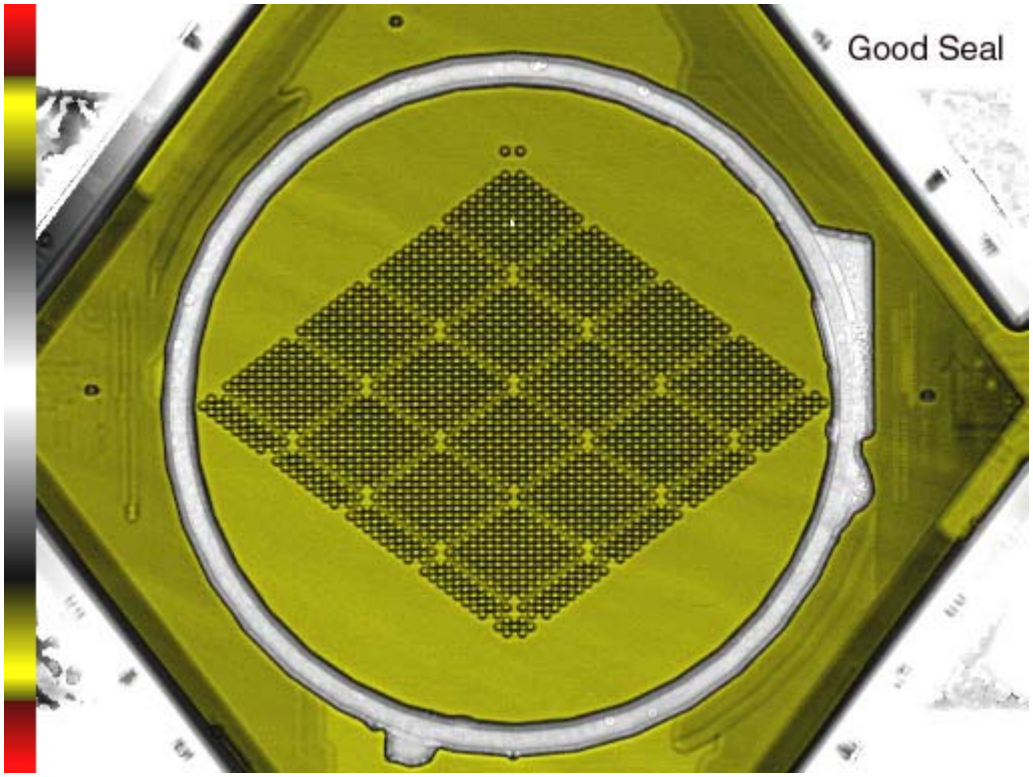
The 48wt%Sn-52wt%In and 100wt%In solders are assumed to obey the Garofalo-Arrhenius creep constitutive law. The creep responses such as the ***creep strain energy density range per cycle*** are determined.

In order to determine the thermal-fatigue life of the solder sealing ring of the photonic switch, a relationship between the number of cycle-to-failure (N_f) and the strain energy density range per cycle is needed. Thus, ***isothermal fatigue tests*** of the solder sealing ring are performed.

In order to increase the confidence of the finite element analysis procedures, material properties, and boundary conditions, some of the simulation results are compared with the ***experimental results measured by the Twyman-Green interferometry*** method.

CONTENTS




Good Seal

Agilent's All-Optical Switch

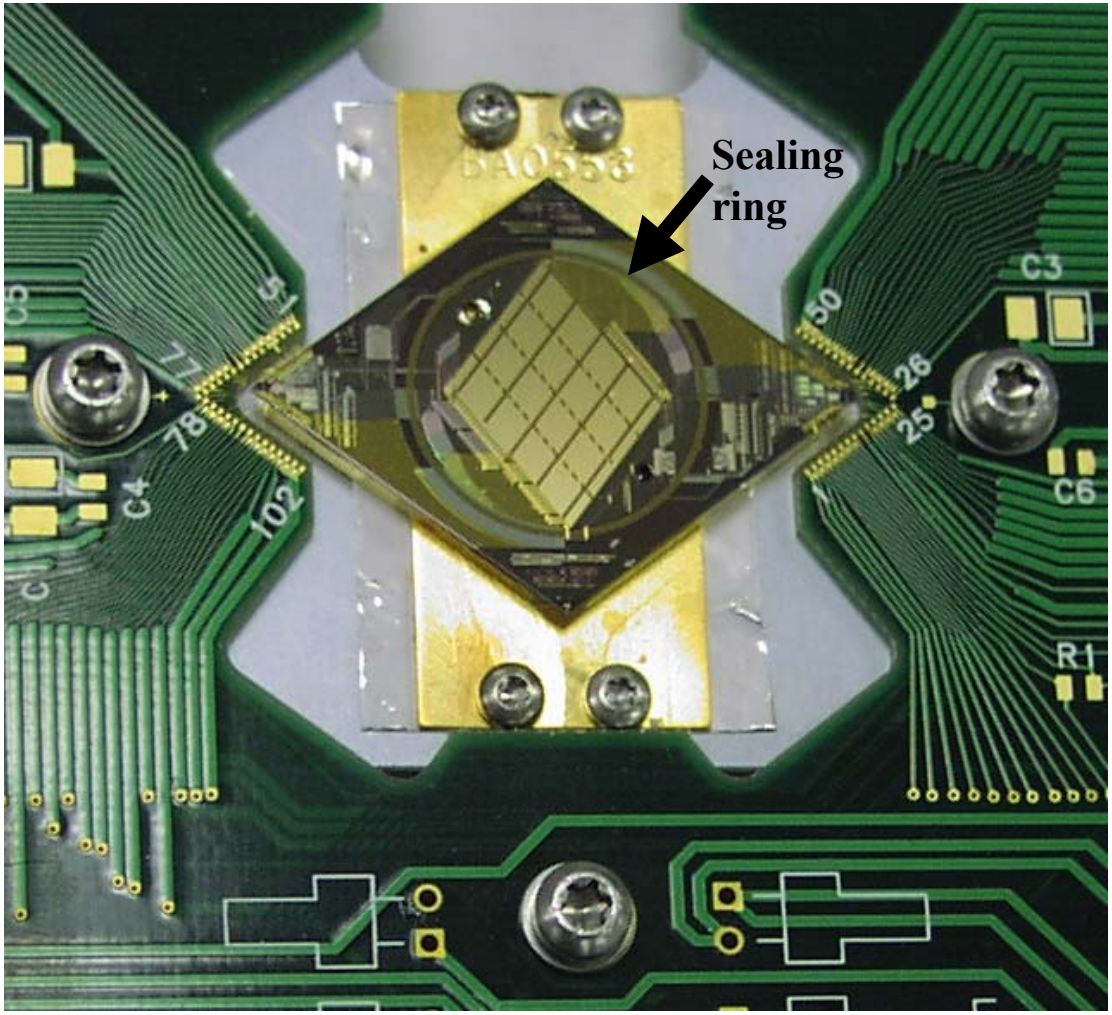
A silica-based planar lightwave circuit (PLC) chip, which contains two intersecting arrays of waveguides, with trenches etched into each crosspoint.

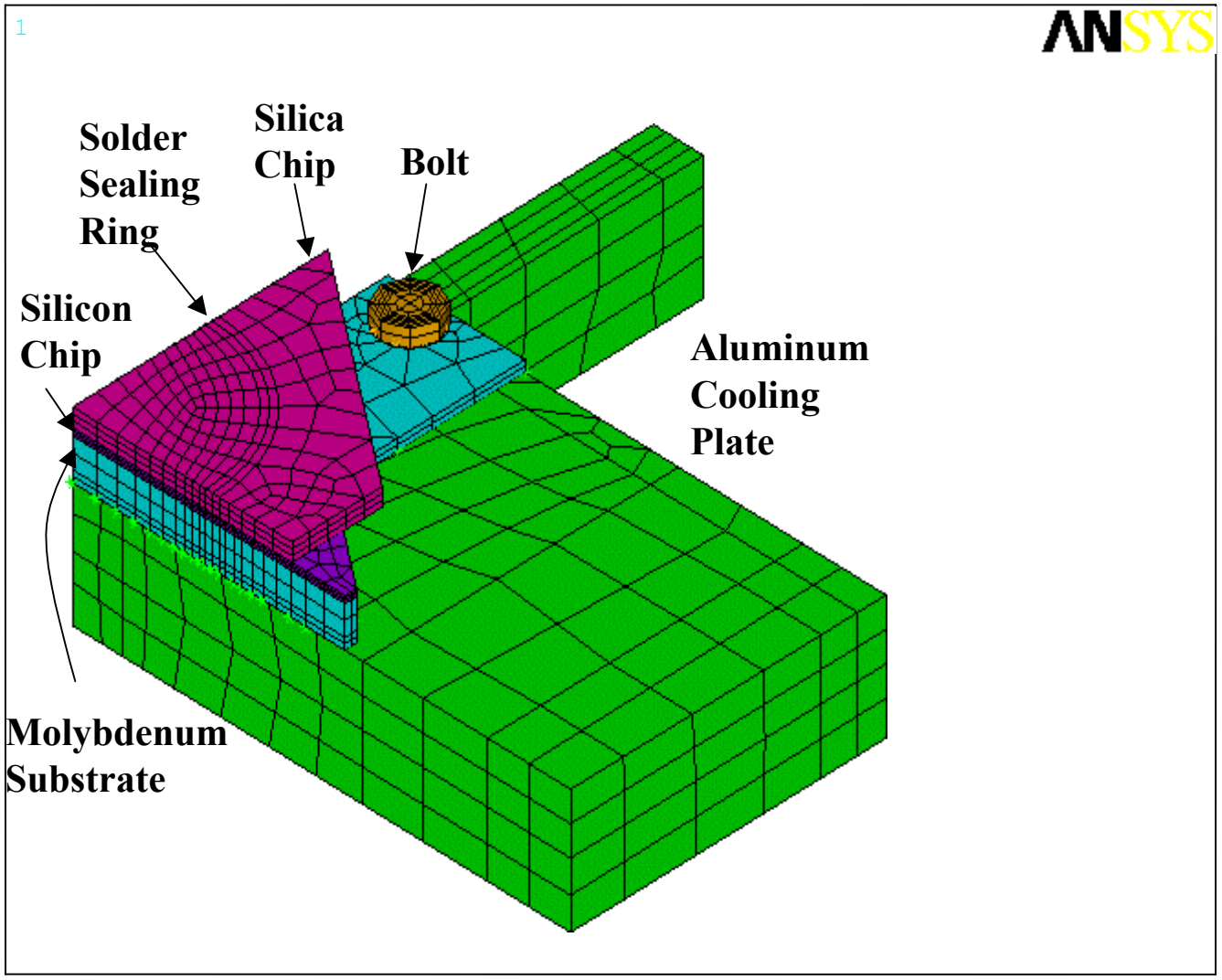
A silicon-based actuator chip, which contains a matching pattern of electrically addressed resistive elements.

These two chips are hermetically sealed together with the 48Sn-52In solder ring.

At the default state, the trenches, along with the rest of the sealed space between the silica and silicon chips, are filled with a liquid whose refractive index matches the waveguides and properties are suitable for bubble creation and control. Optical signals passing along any guide on the silica chip simply pass on through.

However, by activating a resistive element on the silicon chip, a bubble can be created at that crosspoint, so that total internal reflection occurs at the side-wall of the corresponding trench, and switching is achieved.

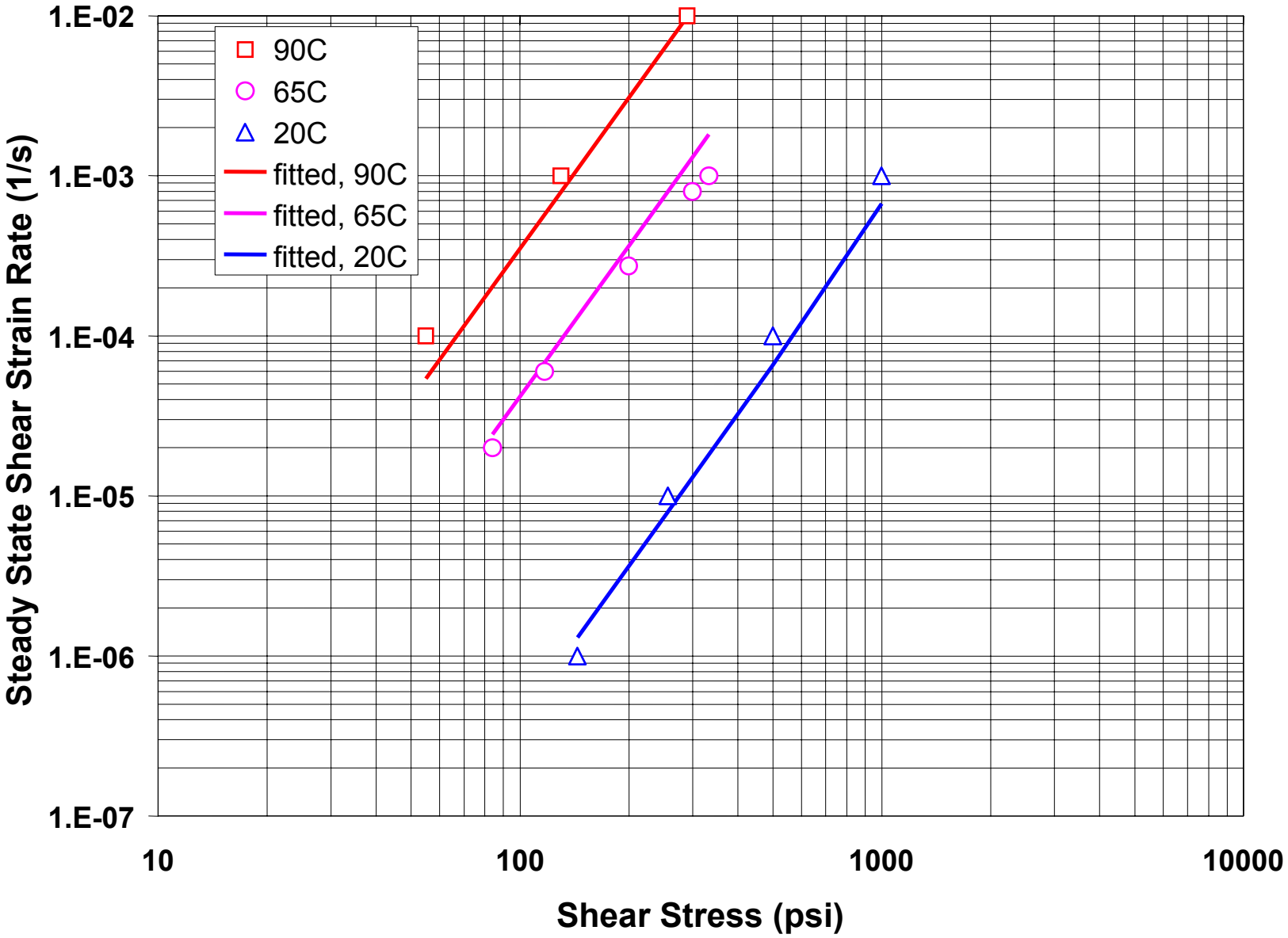

Sealing
ring
C3
C6
R1
C4
C1
C8
51
77
78
102
50
26
25


1
ANSYS
Solder
Sealing
Ring
Silica
Chip
Bolt
Silicon
Chip
Aluminum
Cooling
Plate
Molybdenum
Substrate

Material	Young's Modulus (GPa)	Poisson's Ratio	Coefficient Of Thermal Expansion (ppm/^{0}C)	Yield Strength (MPa)	Tensile Strength (MPa)	Elongation (%)	Thermal Conductivity (W/m-^{0}K)	Density (g/cm^3)	Specific Heat (cal/g-^{0}K)	Creep
Molybdenum (Mo)	**355** [1]	**0.3** [7]	**4.8** [1]	**552** [1]	**655** [1]	**2.5** [3]	**139** [1]	**10.24** [7]	**0.06** [7]	**No**
Silicon (Si)	**163.3** [1]	**0.28** [1]	**2.5** [1]	**34.5** [1]	**185** [1]		**165.43** [1]	**2.4** [2]	**0.169**	**No**
48Sn-52In	**30.5** [8]	**0.36** [8]	**28** [1]					**7.3** [11]		**Yes**
100 In	**11** [9]	**0.45** [9]	**32.1** [6]				**82** [4]	**7.3** [4]		**Yes**
Silica Fused Quartz (SiO_2)	**72.4** [3]	**0.14** [3]	**0.5** [3]	**66.9** [3]	**75.9** [3]		**0.33** [3]	**2.2** [3]		**No**
Aluminum 6061-T6	**70.3** [3]	**0.35** [7]	**23.2** [3]	**10.3** [7]	**45** [7]	**12** [7]	**237** [3]	**2.7** [7]	**0.211** [7]	**No**

Notes:

1. *Solder Joint Reliability of BGA, CSP, Flip Chip, and Fine Pitch SMT Assemblies*, John Lau and Yi-Hsin Pao, McGraw-Hill, 1997.
2. *Electronic Packaging and Interconnection Handbook*, Charles A. Harper, McGraw-Hill, 2000.
3. *Materials Handbook for Hybrid Microelectronics,* J. A. King, Teledyne Microelectronics, 1988.
4. www.webelements.com, 2001.
5. *Ball Grid Array Technology*, John Lau, McGraw-Hill, 1995.
6. *Microvias for Low Cost and High Density Interconnects*, John Lau and Ricky Lee, McGraw-Hill, 2001.
7. *Mark's Standard Handbook for Mechanical Engineers*, Eighth Edition, McGraw-Hill, 1978.
8. Average of Sn and In from Note 4.
9. *Technical Bulletin of Pure Indium*, Indium Corporation of America, 2001.
10. *Superplastic Creep of Low Melting Point Solder Joints*, Z. Mei and J. W. Morris, J. of Electronic Materials, 21(4): 401-407, 1992.
11. *Solder Paste in Electronics Packaging*, Jennie Hwang, Van Nostrand Reinhold, 1989.


90C
65C
20C
fitted, 90C
fitted, 65C
fitted, 20C
1.E-02
1.E-03
1.E-04
1.E-05
1.E-06
1.E-07
Steady State Shear Strain Rate (1/s)
10
100
1000
10000
Shear Stress (psi)

Garofalo-Arrhenius Creep Constitutive Equation:

$$\frac{d\gamma}{dt} = C\left[\frac{G}{\Theta}\right]\sinh\left[\omega\frac{\tau}{G}\right]^{n}\exp\left[-\frac{Q}{k\Theta}\right]$$

γ is the creep shear strain,
$d\gamma/dt$ is the creep shear strain rate,
t is the time,
C is a material constant,
G is the temperature-dependent shear modulus,
Θ is the absolute temperature (^{o}K),
ω defines the stress level at which the power law stress dependence breaks down,
τ is the shear stress,
n is the stress exponent,
Q is the activation energy for a specific diffusion mechanism,
k is the Boltzmann's constant (8.617 x 10^{-5} eV/^{o}K).

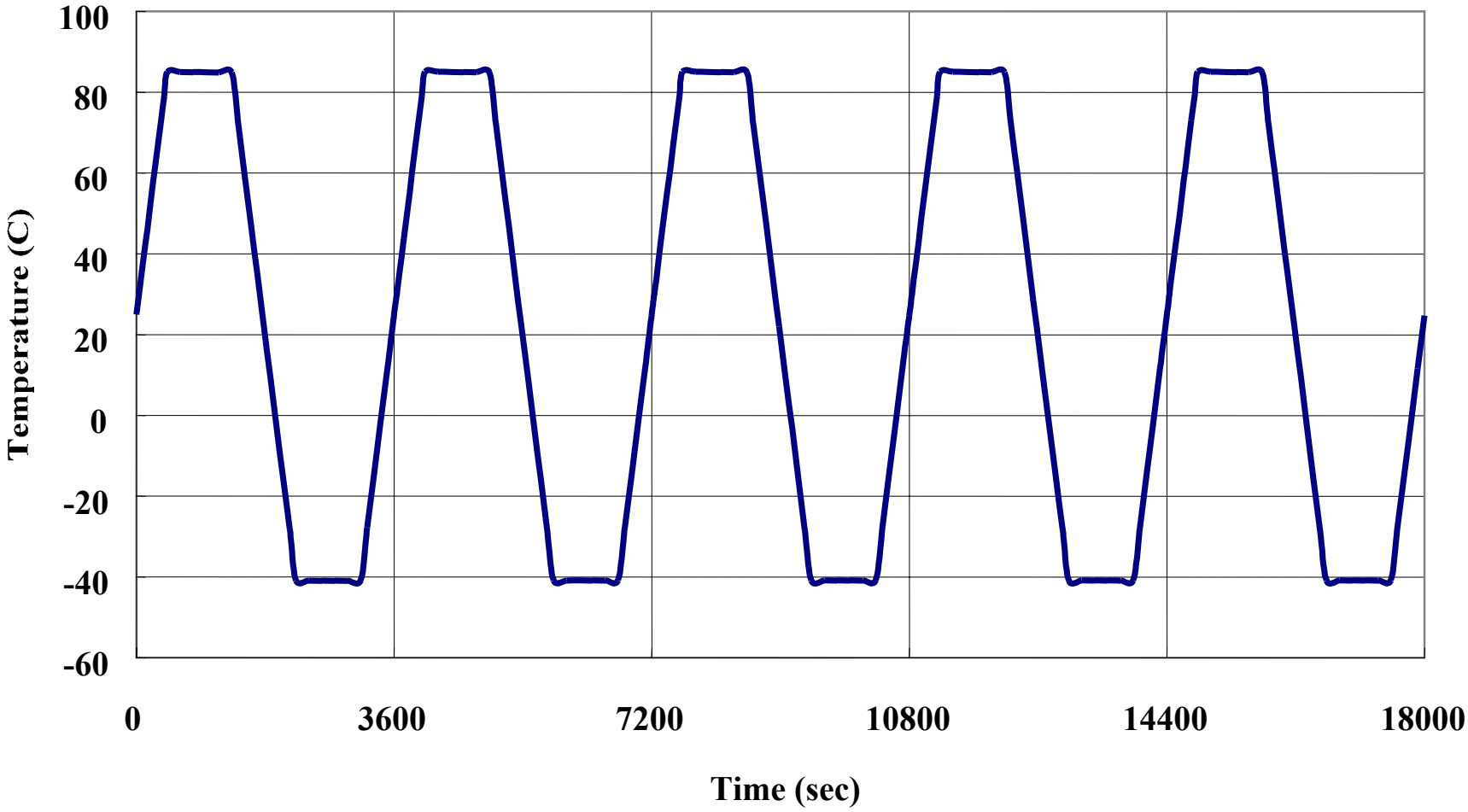
$$\frac{d\varepsilon}{dt} = C_1 [\sinh(C_2\sigma)]^{C_3} \exp\left(-\frac{C_4}{T}\right)$$

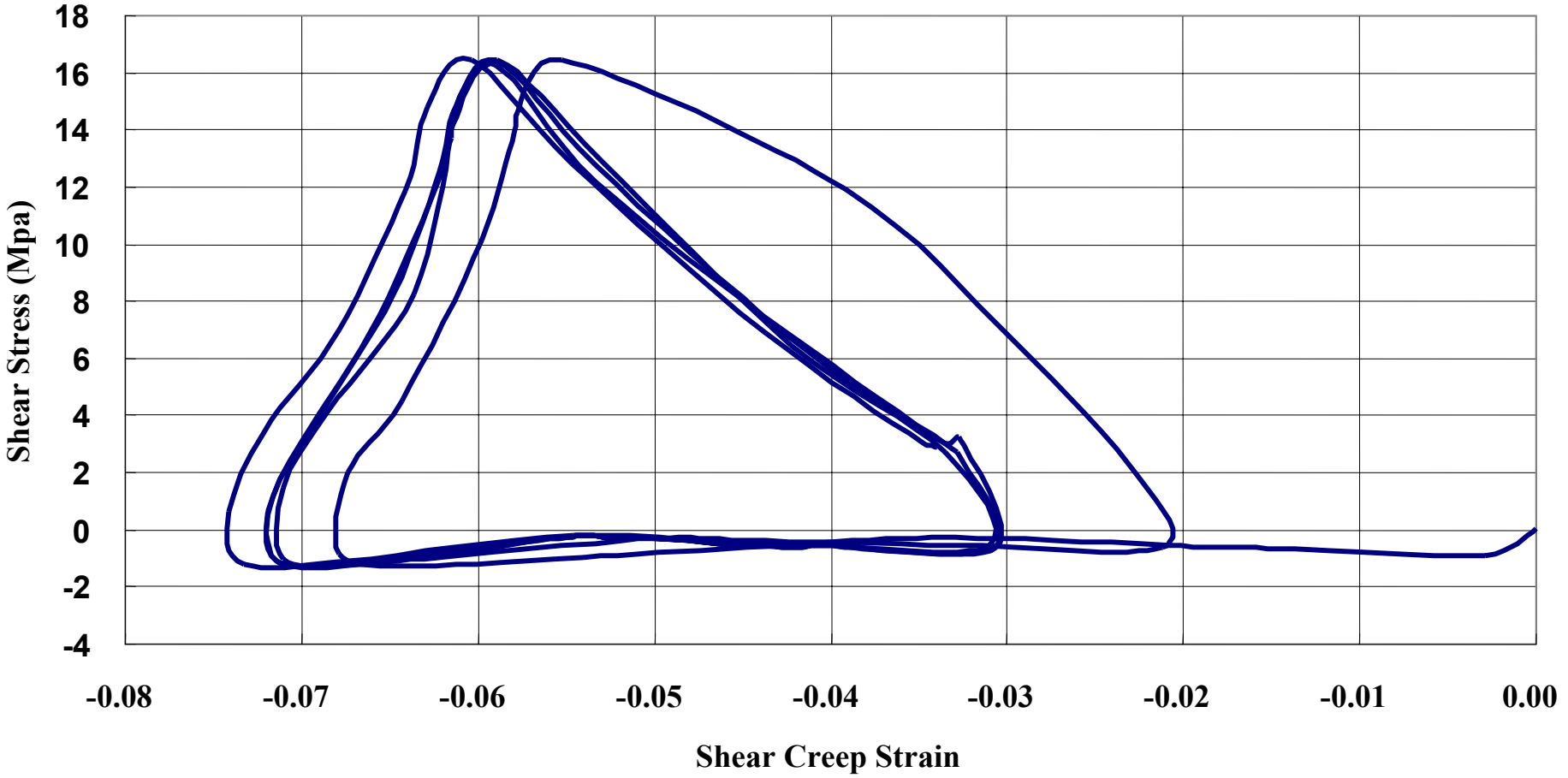
For 100wt%In solder

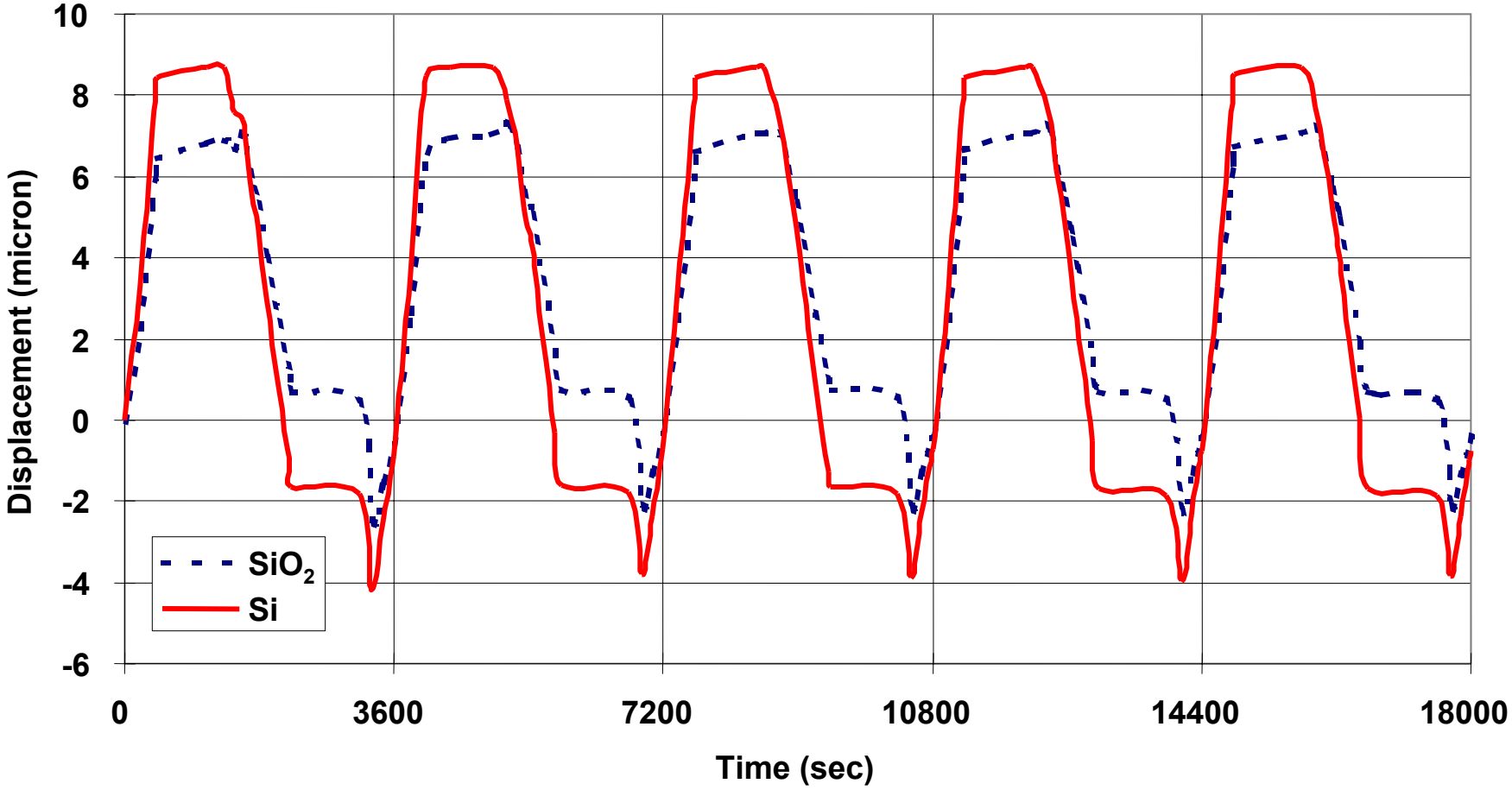
$$C_1 = 2.5357x10^{11}(593 - T)/T$$
$$C_2 = 1/(5{,}234.84 - 8.648T)$$
$$C_3 = 3.1103$$
$$C_4 = 9{,}704.9$$

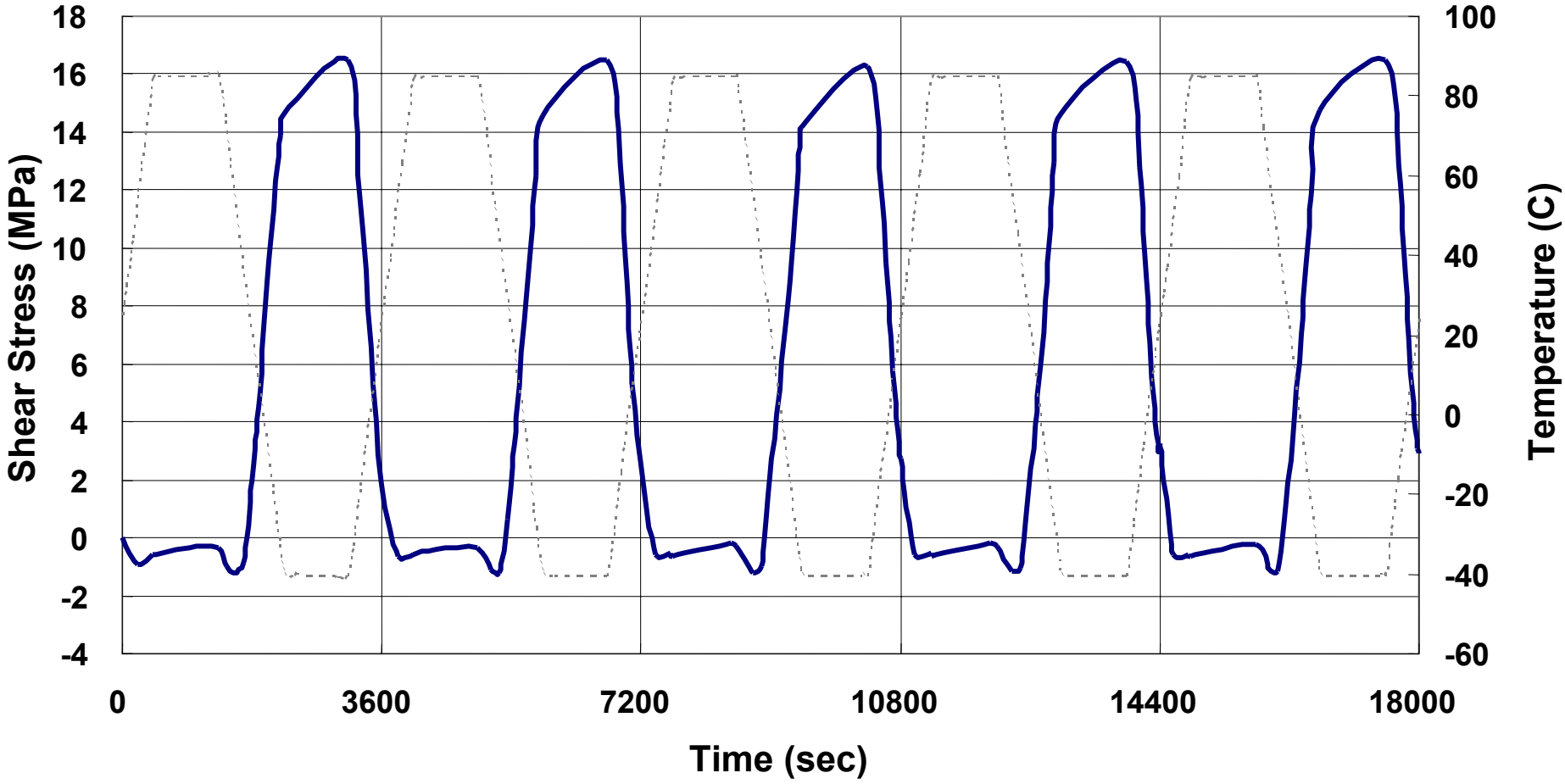
For 48wt%Sn-52wt%In solder

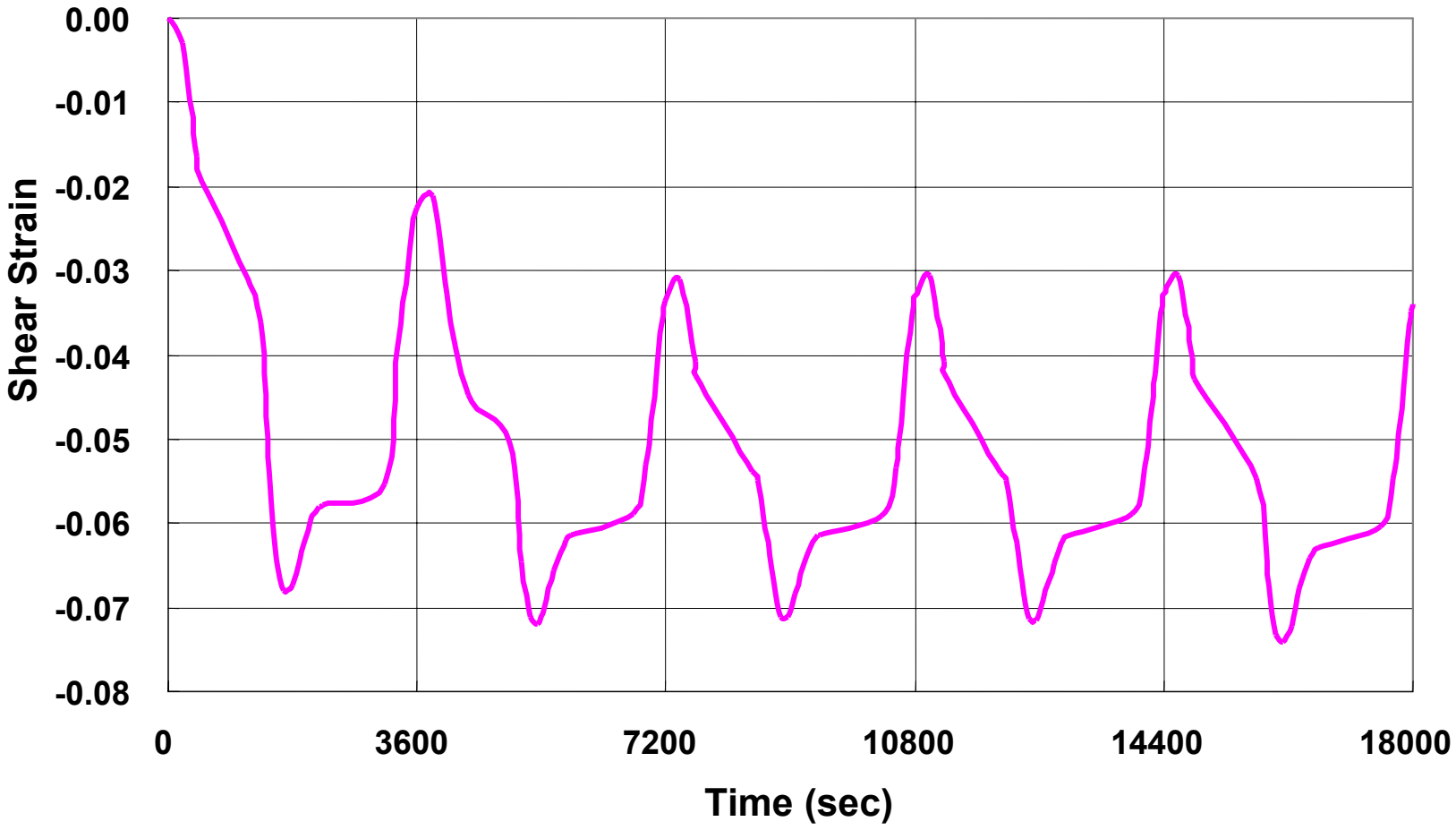
$$C_1 = 40{,}647\ (593 - T)/T$$
$$C_2 = 1/(274 - 0.47\ T)$$
$$C_3 = 5$$
$$C_4 = 8{,}356$$

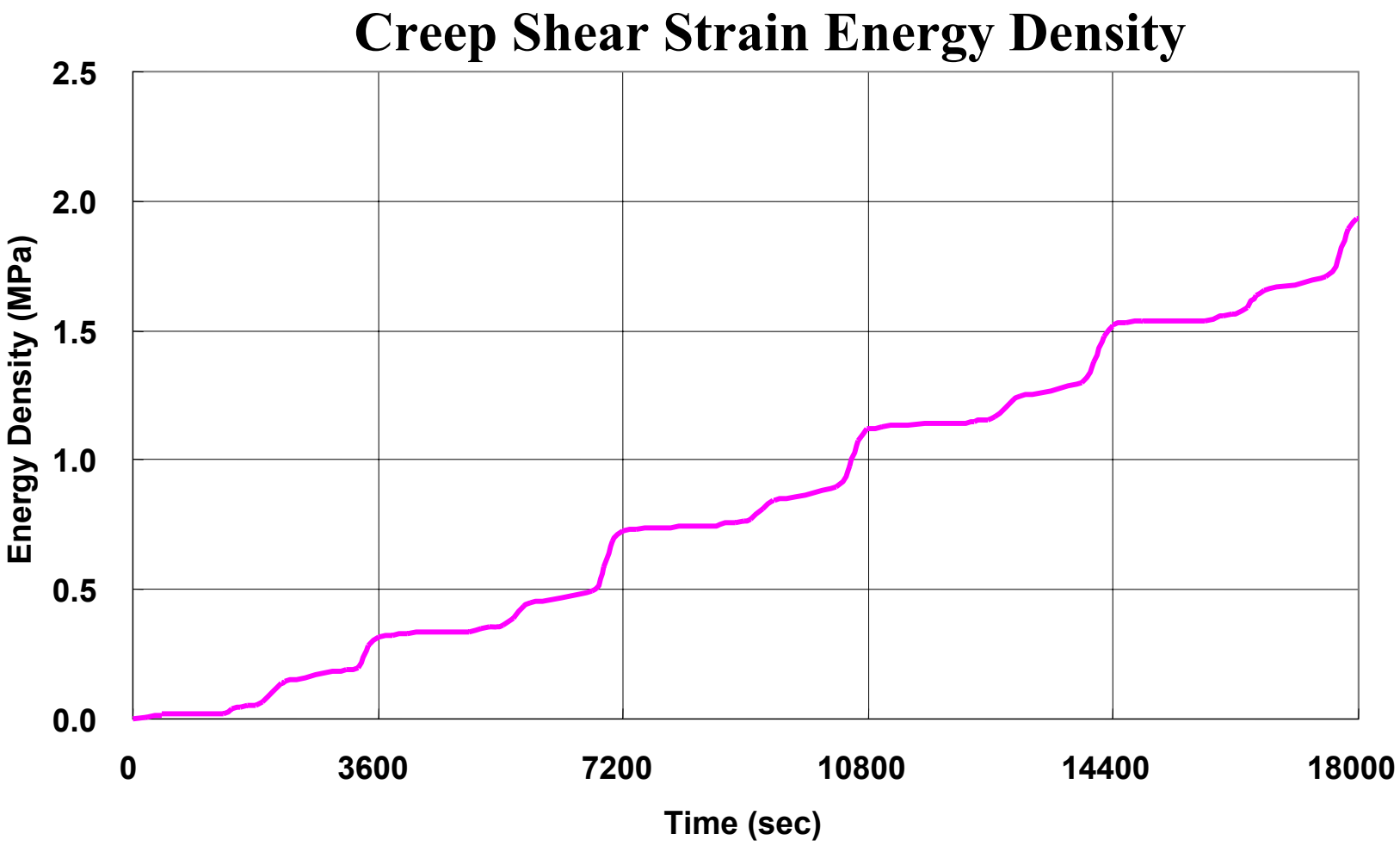

100
80
60
40
20
0
-20
-40
-60
Temperature (C)
0
3600
7200
10800
14400
18000
Time (sec)

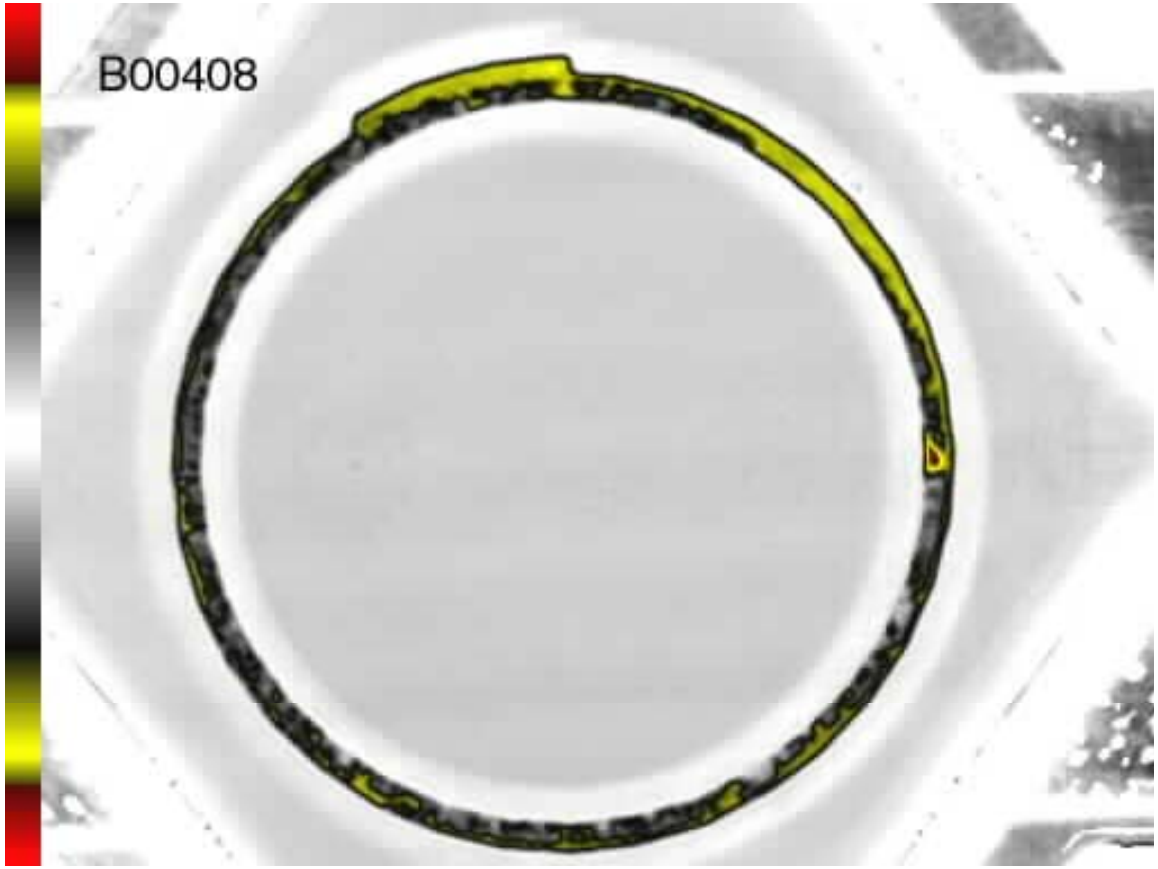

18
16
14
12
10
8
6
4
2
0
-2
-4
Shear Stress (Mpa)
-0.08
-0.07
-0.06
-0.05
-0.04
-0.03
-0.02
-0.01
0.00
Shear Creep Strain


10
8
6
4
2
0
-2
-4
-6
Displacement (micron)
0
3600
7200
10800
14400
18000
Time (sec)
SiO2
Si


Shear Stress (MPa)
18
16
14
12
10
8
6
4
2
0
-2
-4
Temperature (C)
100
80
60
40
20
0
-20
-40
-60
0
3600
7200
10800
14400
18000
Time (sec)


0.00
-0.01
-0.02
-0.03
-0.04
-0.05
-0.06
-0.07
-0.08
Shear Strain
0
3600
7200
10800
14400
18000
Time (sec)


Creep Shear Strain Energy Density
2.5
2.0
1.5
1.0
0.5
0.0
Energy Density (MPa)
0
3600
7200
10800
14400
18000
Time (sec)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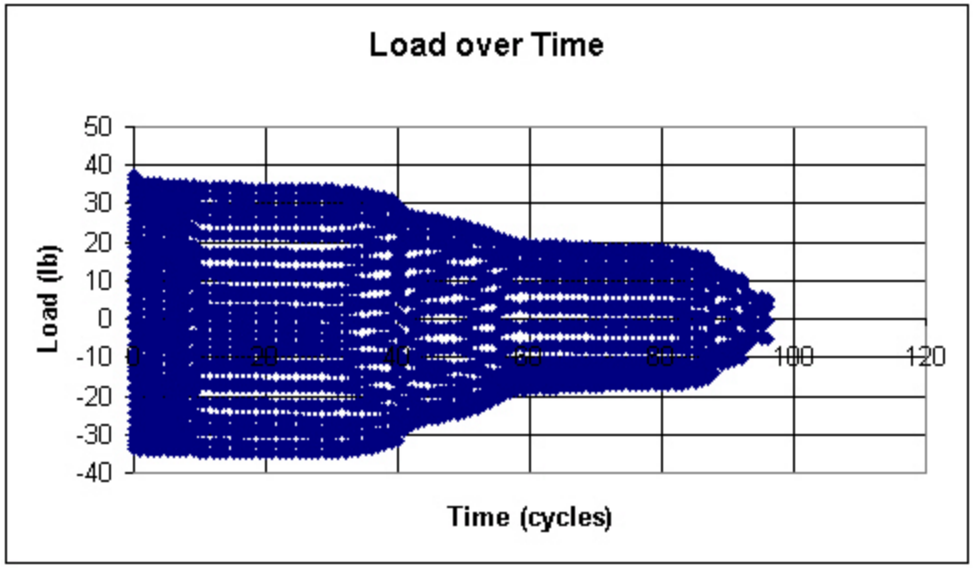
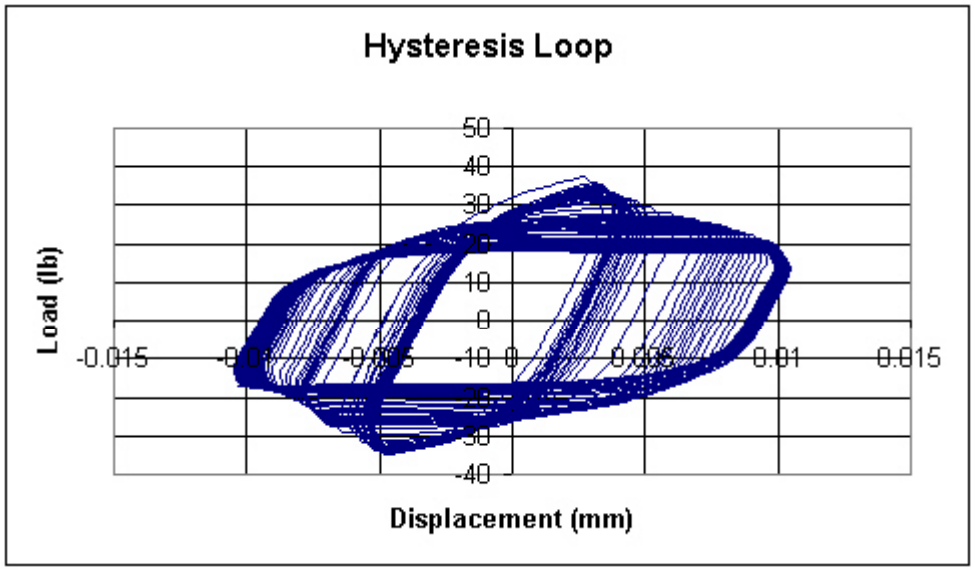
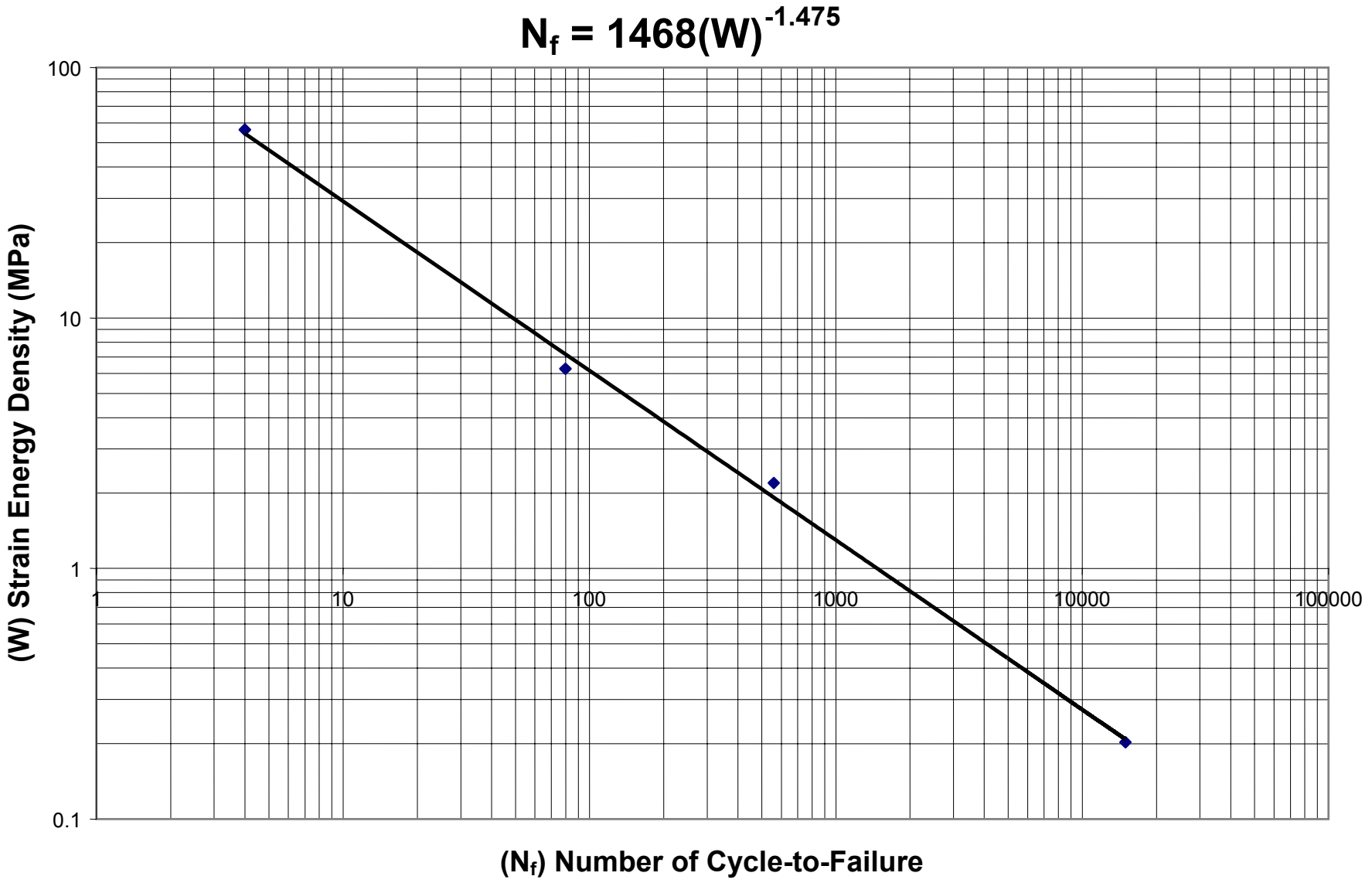
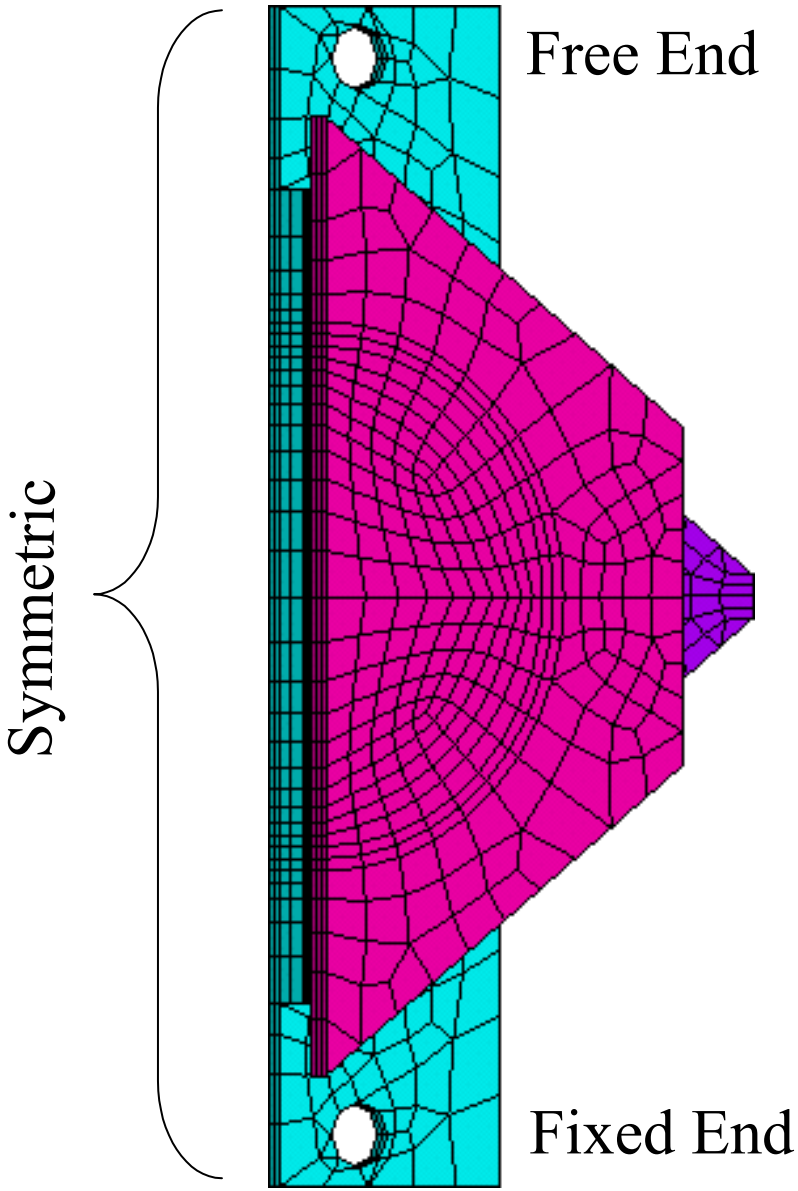
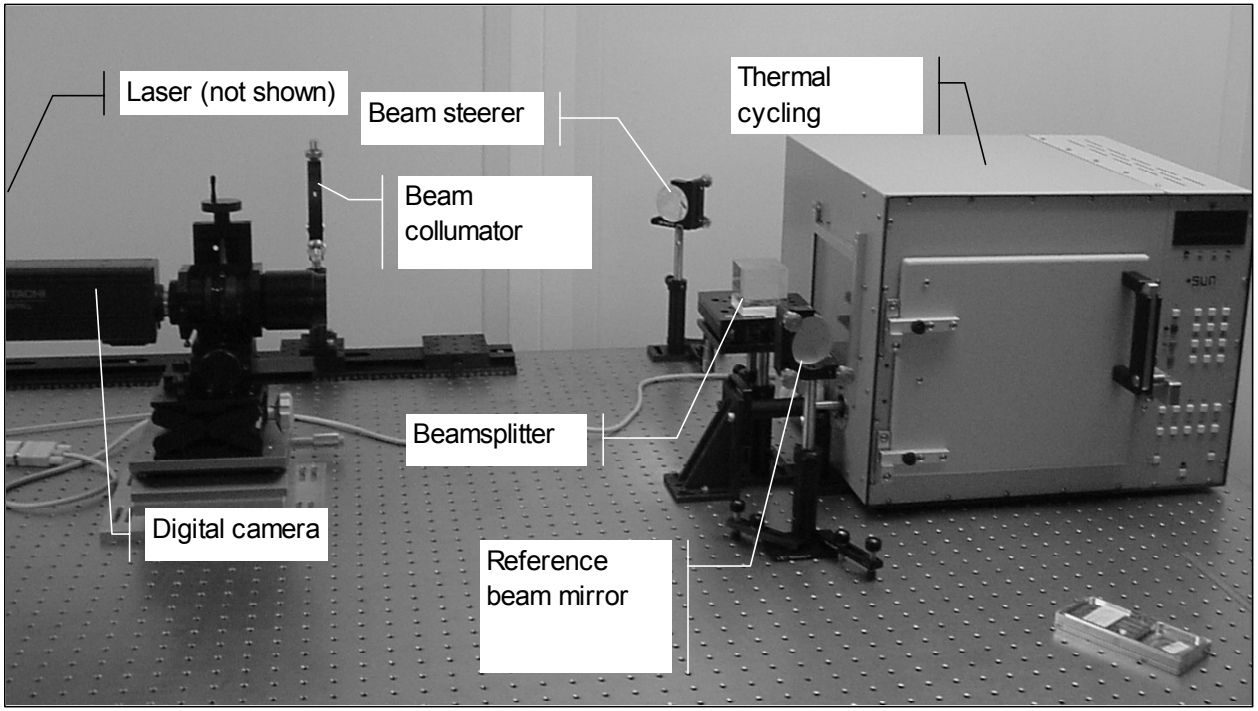
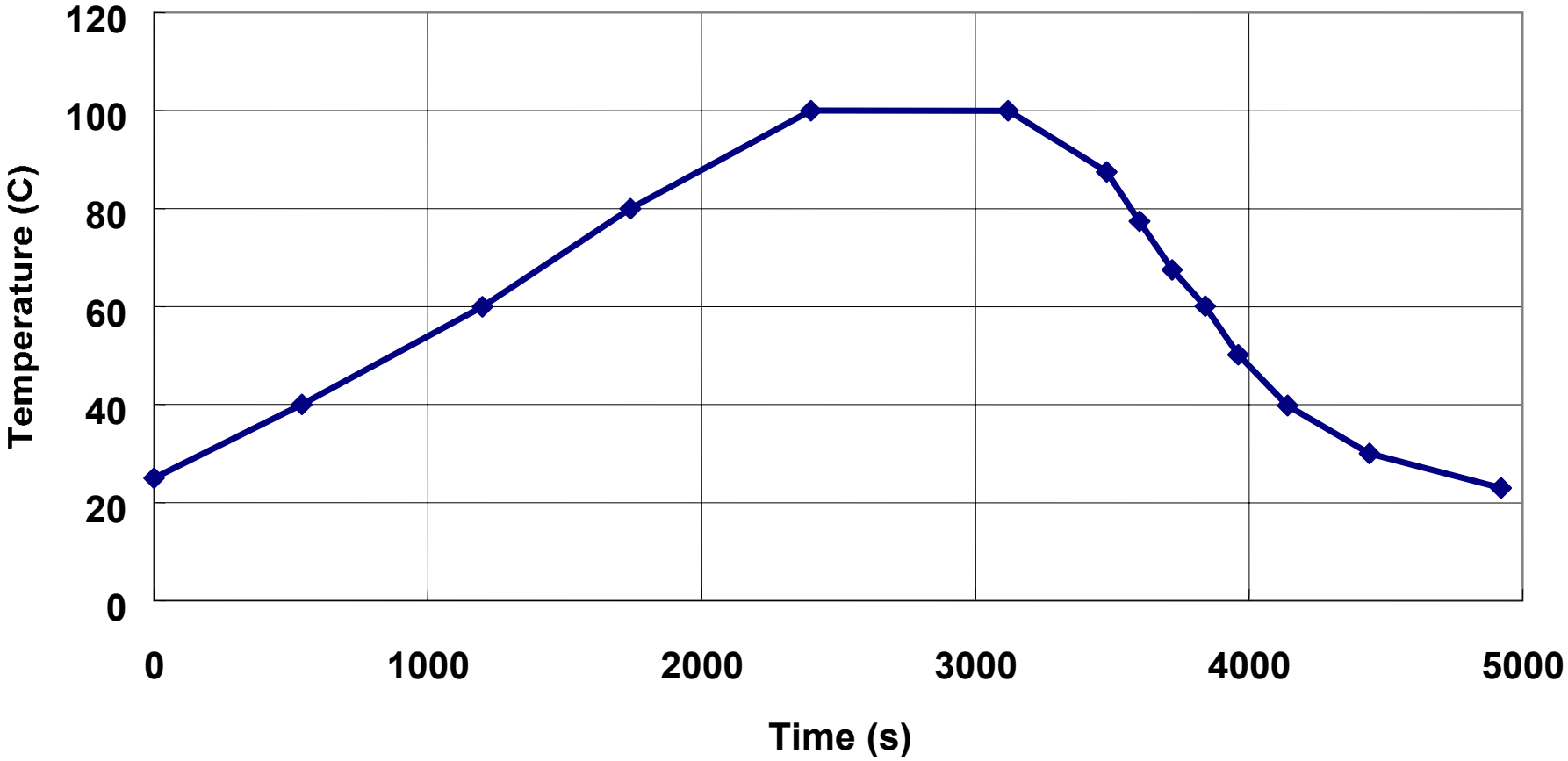

Load over Time
Load (lb)
50
40
30
20
10
0
-10
-20
-30
-40
0
20
40
60
80
100
120
Time (cycles)

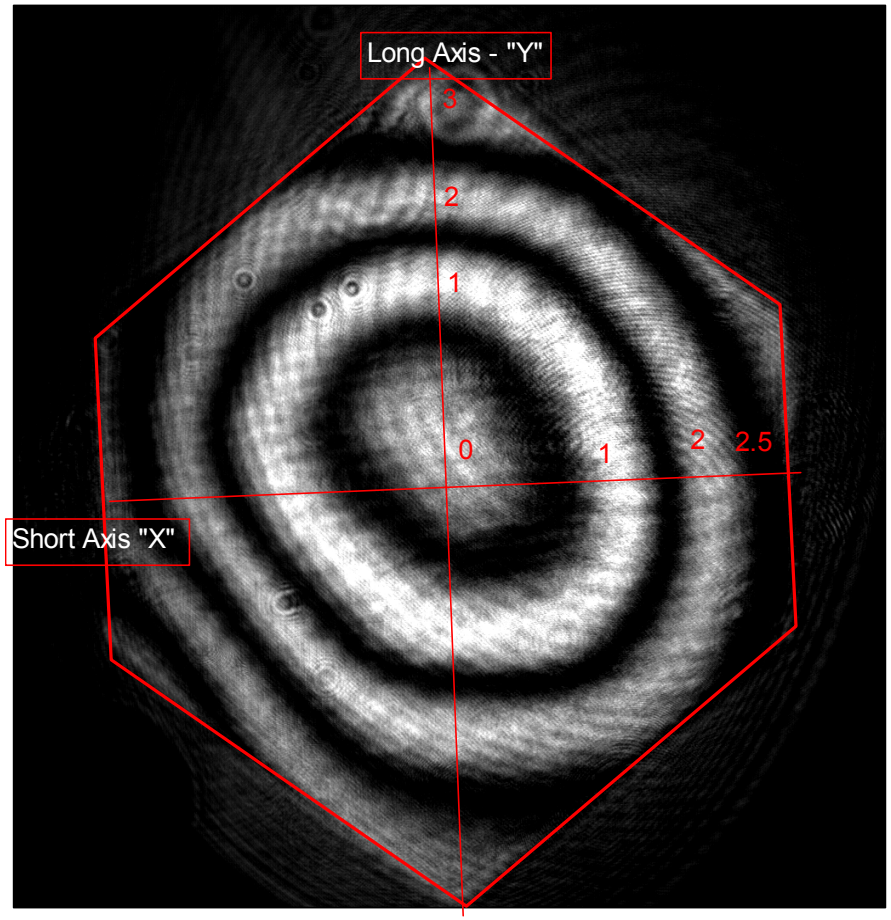

Hysteresis Loop
Load (lb)
50
40
30
20
10
0
-10
-20
-30
-40
-0.015
-0.01
-0.005
0
0.005
0.01
0.015
Displacement (mm)

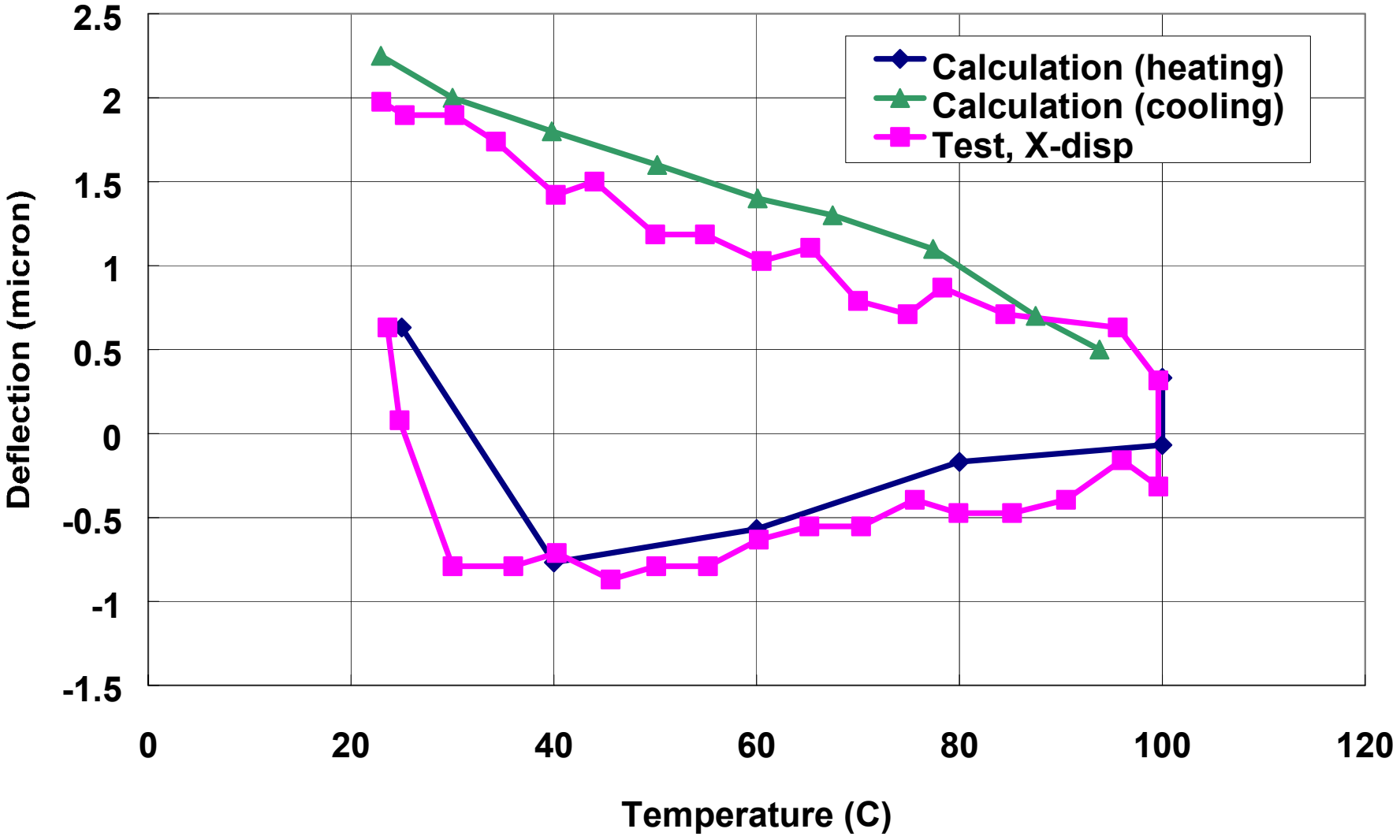

$N_f = 1468(W)^{-1.475}$
100
10
1
0.1
1
10
100
1000
10000
100000
(W) Strain Energy Density (MPa)
(N_f) Number of Cycle-to-Failure


Free End
Symmetric
Fixed End


Laser (not shown)
Beam steerer
Thermal cycling
Beam collumator
Beamsplitter
Digital camera
Reference beam mirror


120
100
80
60
40
20
0
Temperature (C)
0
1000
2000
3000
4000
5000
Time (s)


Long Axis - "Y"
3
2
1
0
1
2
2.5
Short Axis "X"


Calculation (heating)
Calculation (cooling)
Test, X-disp
Deflection (micron)
2.5
2
1.5
1
0.5
0
-0.5
-1
-1.5
0
20
40
60
80
100
120
Temperature (C)

SUMMARY

- A systematic method for determining the thermal-fatigue life of the solder sealing ring in a photonic package has been provided.
- A creep constitutive equation for the 48Sn-52In solder has been obtained.
- Confidence of the present analysis procedures, material properties, boundary conditions and results has been demonstrated by comparing with experiment results obtained by the Twyman-Green interferometry method.
- The fatigue material property (number of cycle-to-failure vs strain energy density per cycle) for the 48Sn-52In has been determined by the isothermal shearing fatigue tests.
- By combining the finite element results (strain energy density per cycle) and the fatigue test results, the average thermal-fatigue life of the solder ring is determined to be 4,000 cycles. This is more than adequate for shipping/storing/handling the photonic package.

Thermal Analysis of Vertical-Cavity Surface-Emitting LED/VCSEL Assembly with Lead-Free Flip Chip Interconnects

John H. Lau
Agilent Technologies, San Jose, CA, USA

S.W. Ricky Lee
Hong Kong University of Science & Technology
Clear Water Bay, Kowloon, Hong Kong

PhoPack2002, Stanford University, CA, USA
7/14/2002

Objectives

- To determine the effects of interconnect materials and ambient temperature on the steady-state temperature distribution of a 2x2 area array parallel vertical-cavity surface-emitting LED/VCSEL assembly.
- The light sources are deposited on a GaAs chip, which is mounted on a Si-substrate with four flip chip solder joints.
- Two kinds of solders, namely, 63Sn-37Pb and 80Au-20Sn, are studied.

Outline of Presentation

- Introduction and Overview
- Description of Assembly Configuration
- Finite Element Modeling
- Thermal Analysis and Discussion
- Concluding Remarks

Introduction

Fiber-Optic Communication Systems

* Light Sources
* Optical Fibers
* Optical Receivers

The electrical signal is converted into the optical signal through the ***light source***.

The optical signal is transmitted through the ***optical fiber***.

The optical signal is converted back into the electrical signal through the ***optical receiver***.

Light Sources

Most of the light sources are based on the electron-hole recombination in semiconductor materials. This recombination results in the release of energy (in the form of another photon), which can take place:

- **SPONTANEOUSLY such as the light-emitting diodes (LEDs), which are used for very short distance such as chip-to-chip communications with plastic fibers.**

- **As a result of an EXTERNAL STIMULUS such as the semiconductor lasers, which are used for long distance telecommunications.**

For both LEDs and semiconductor lasers, they can collect the light in the direction parallel to the p-n junction and are called the edge-emitting diodes and edge-emitting lasers, respectively.

They can also collect the light in the direction perpendicular to the p-n junction and are called the surface-emitting diodes and vertical-cavity surface-emitting lasers (VCSELs), respectively.

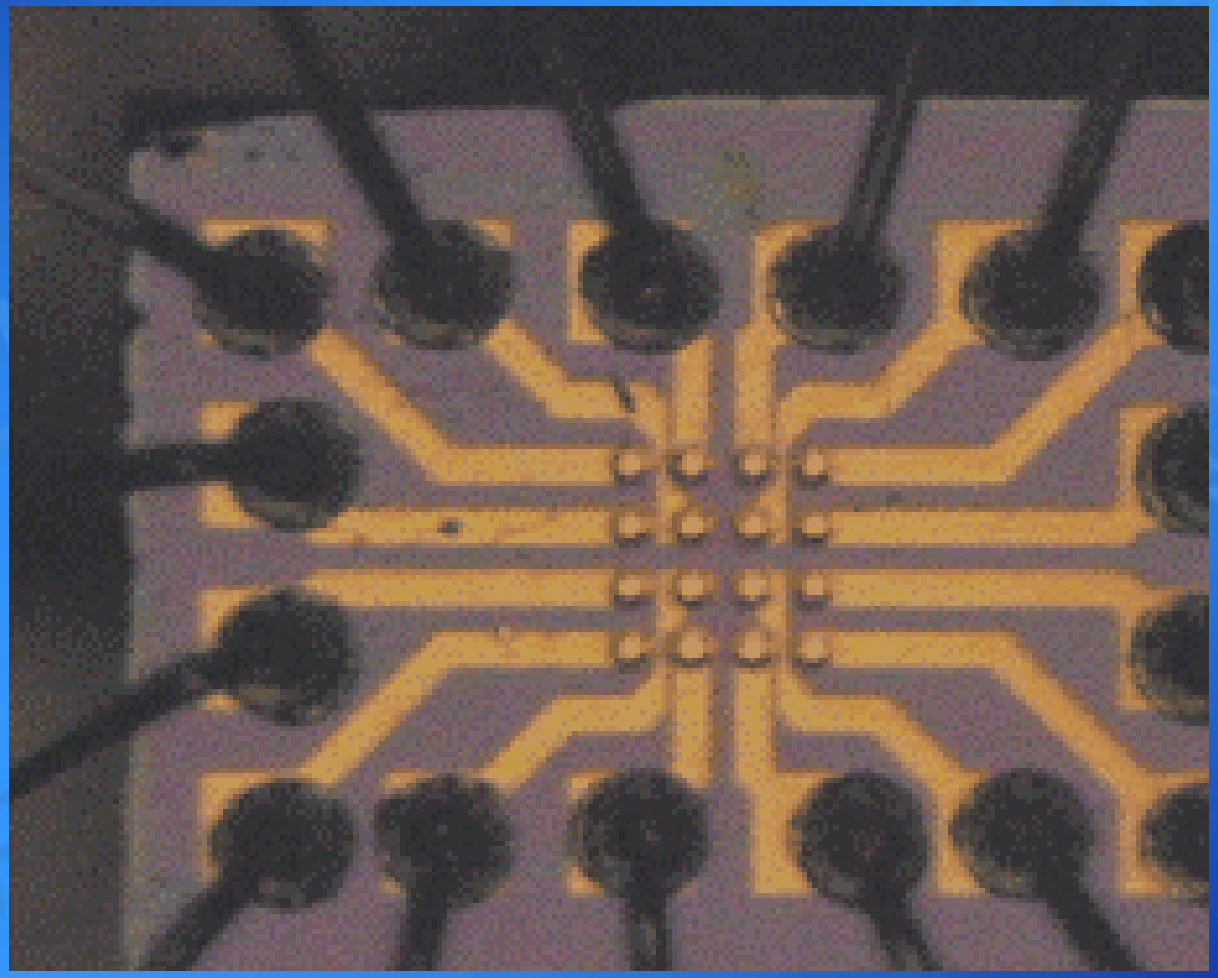
One of the advantages of surface-emitting light sources is that they can be used in parallel optics that offer low-cost interconnection with perhaps the best use of backplane space in a network system.

In principle, the wavelength in the infrared region has the advantage of integrating large 2-D emitter arrays with active (such as CMOS driver) components. This is because the semiconductor becomes transparent in this wavelength region and, therefore, the device can emit lights through the substrate.

This feature yields to the possibility of applying the conventional flip chip technology to the LED/VCSEL assembly.

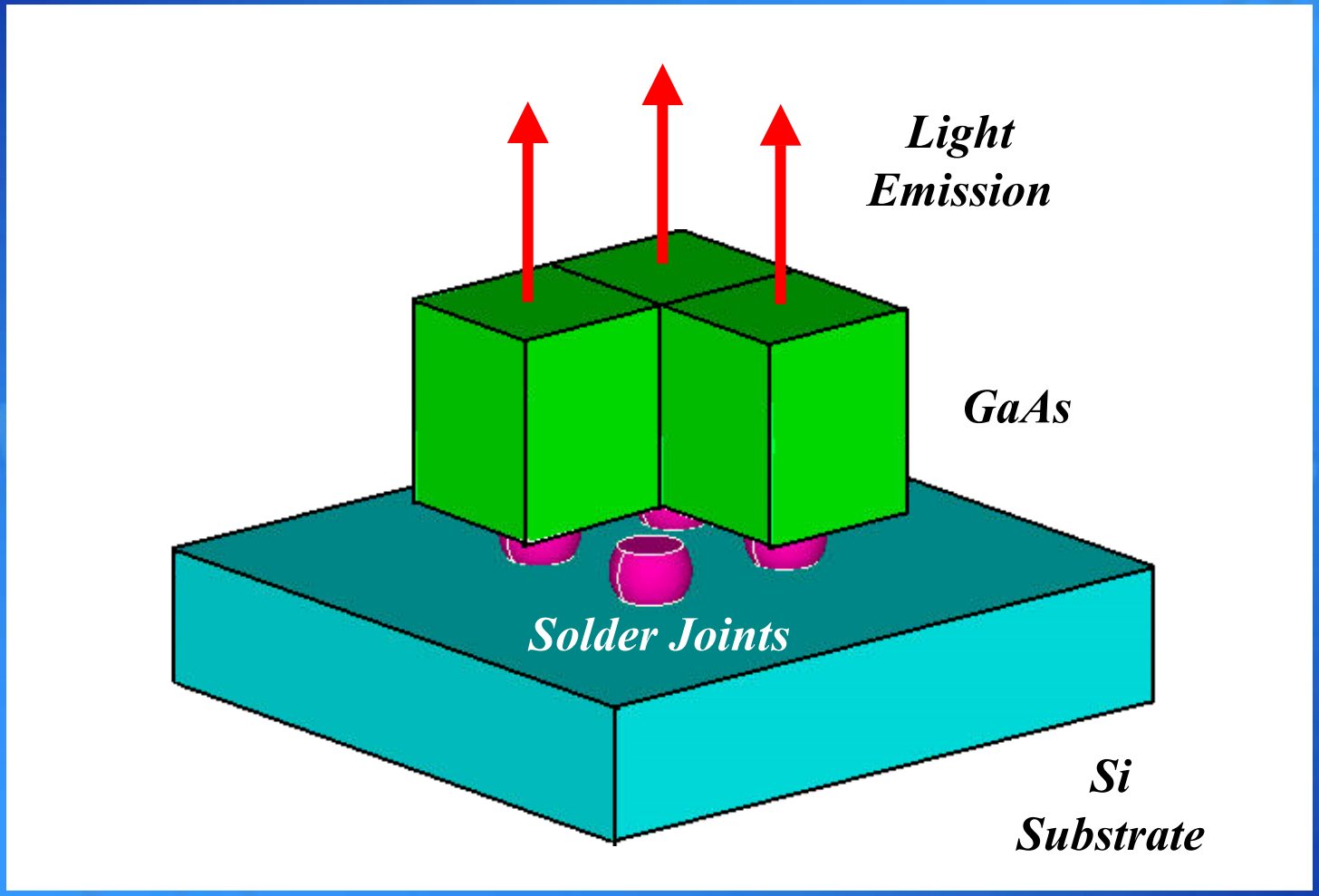
One of the major advantages of solder-bumped flip chip technology is the self-alignment capability.

4x4 VCSEL Array with 16 Wire Bonds



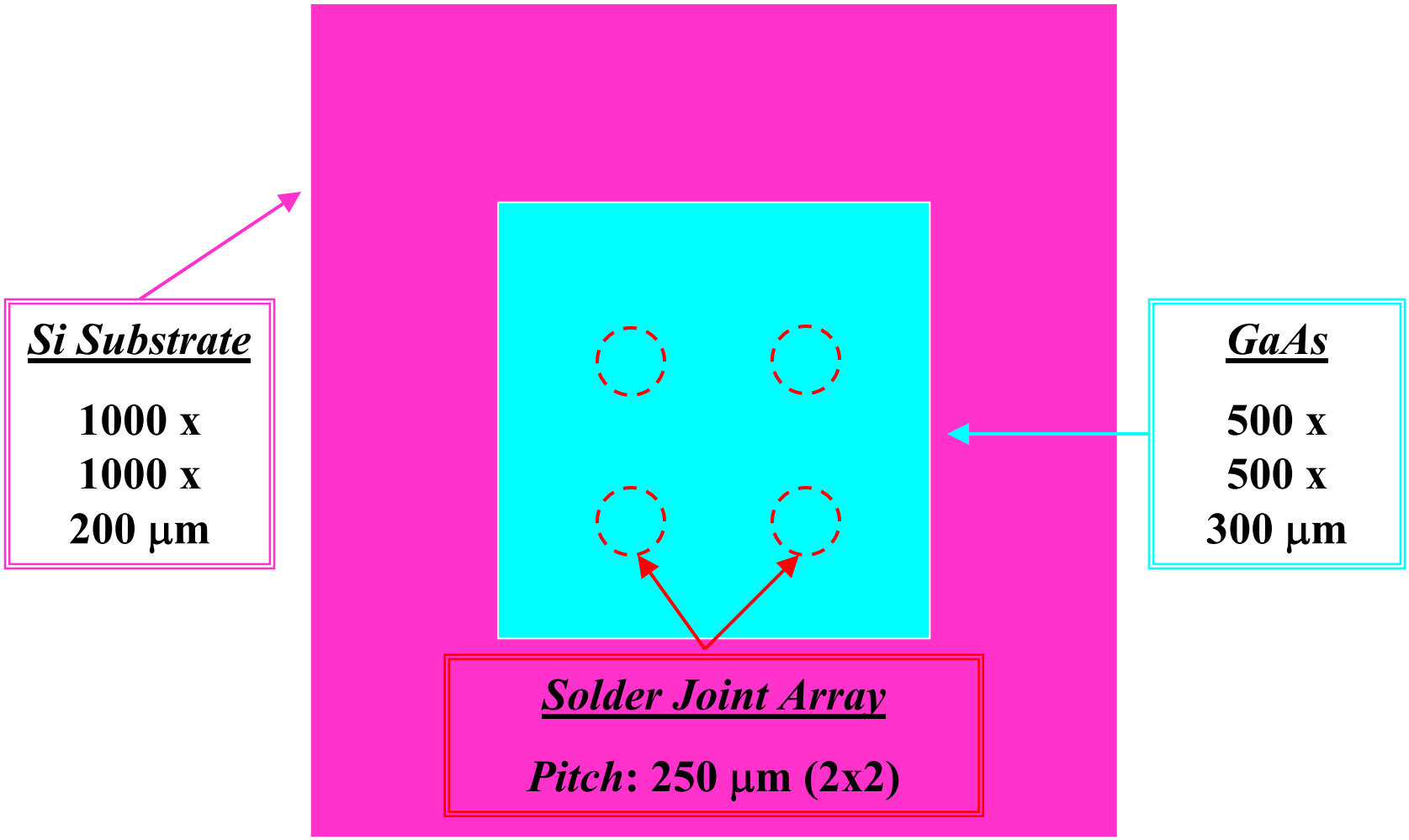
Courtesy of Honeywell

Configuration of VCSEL Assembly

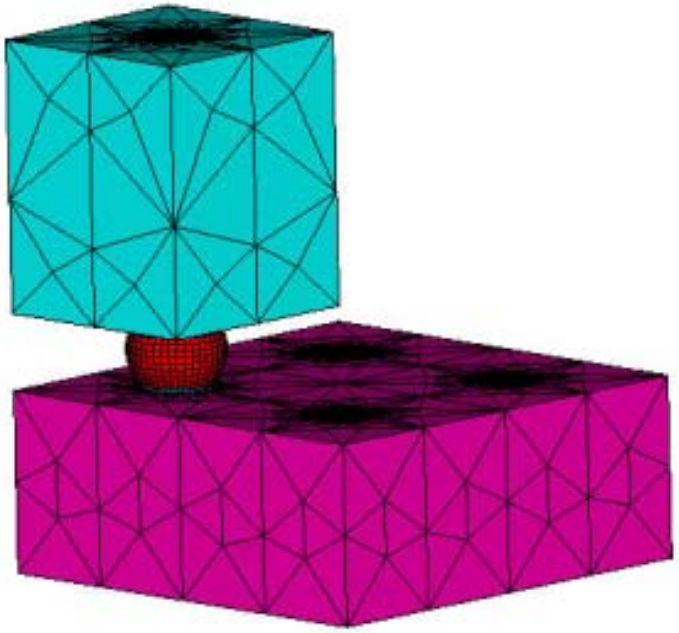


(A quarter of the GaAs chip is removed to observe the solder joints)

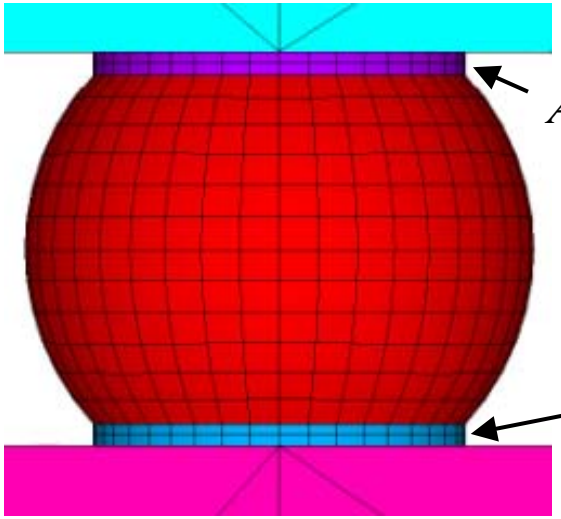
Dimensions of VCSEL Assembly



Finite Element Meshes

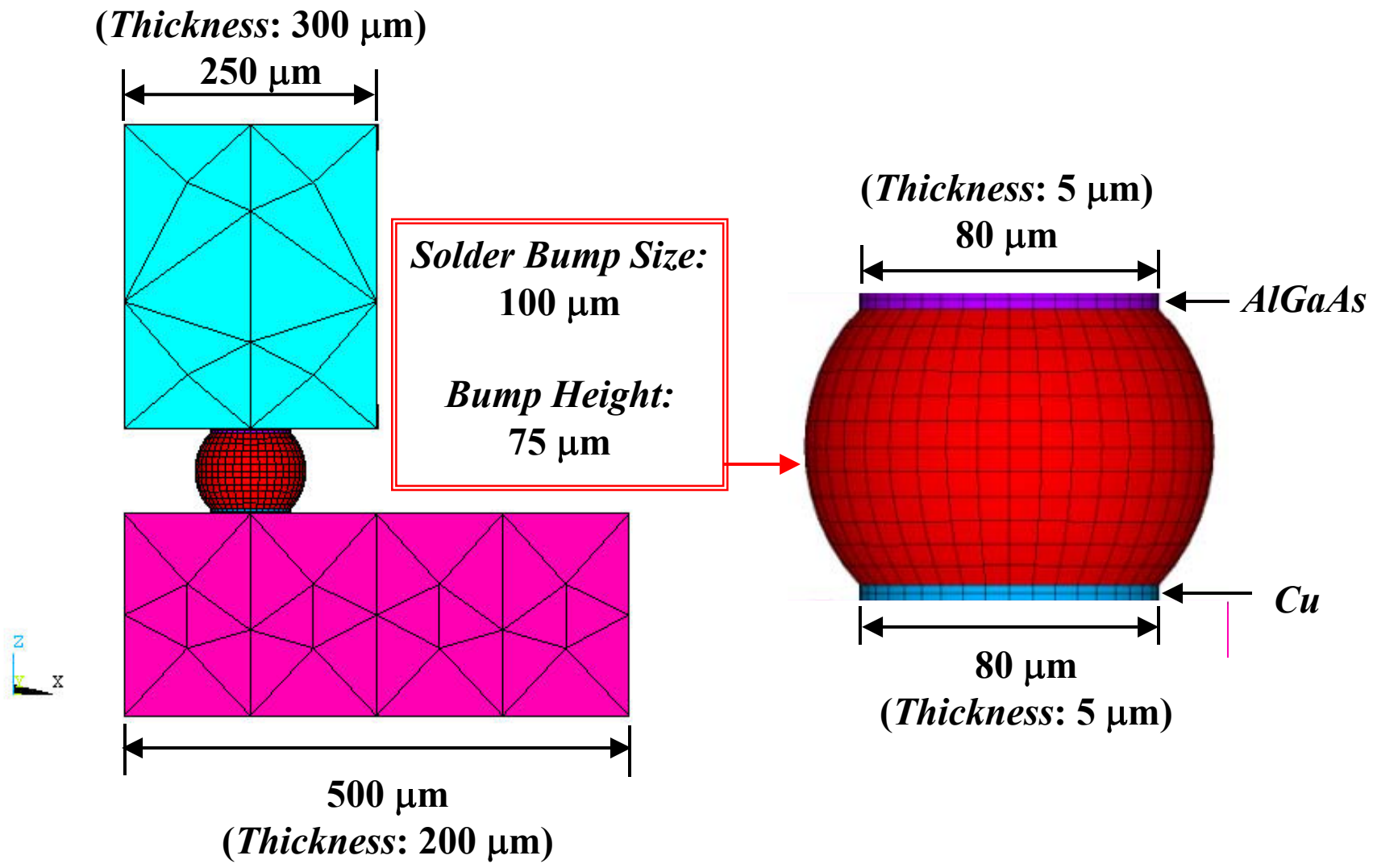


Finite Element Mesh of a Quarter Whole VCSEL Assembly



Local Finite Element Mesh of AlGaAs/Solder Joint/Cu Pad

Dimensions of Finite Element Model



Finite Element Thermal Analysis

ANSYS V. 5.7

SOLID70 3-D 8-node Element

Steady-State Thermal Conduction

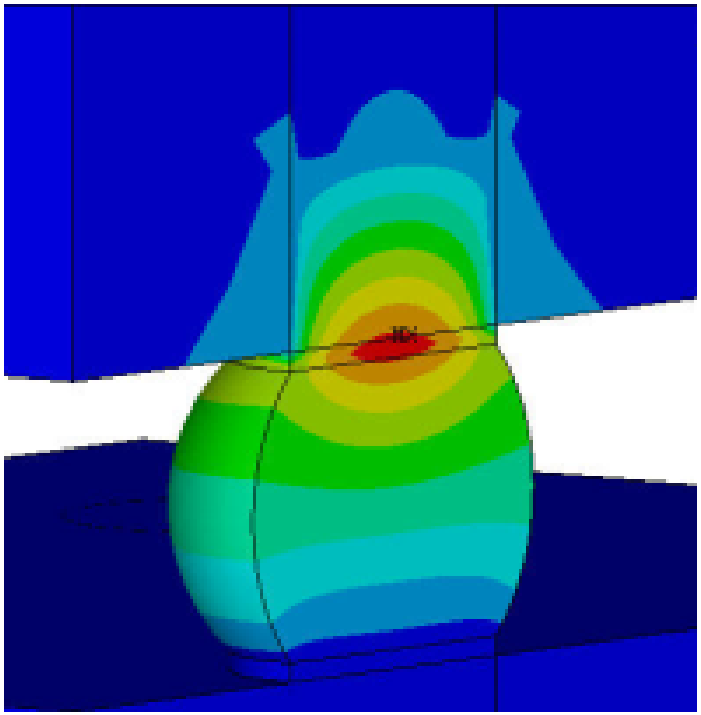
Heat Source: AlGaAs (1 mW)

Ambient Temperature: 27°C or 55°C

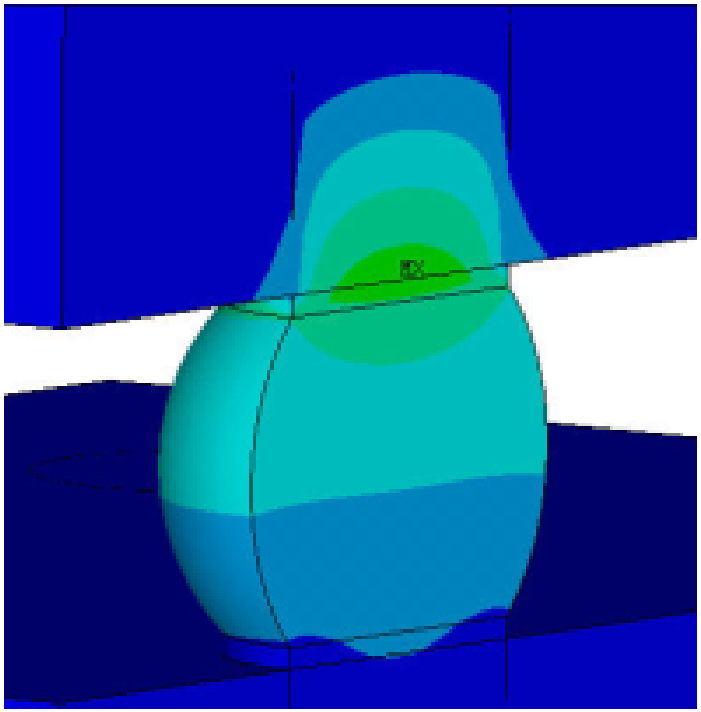
Thermal Conductivity for Modeling

Materials	Thermal Conductivity (W/m•K)
GaAs	33.7
AlGaAs	33.67
63Sn-37Pb	50.6
80Au-20Sn	251
Cu	400
Si	165

Temperature Contours (I)



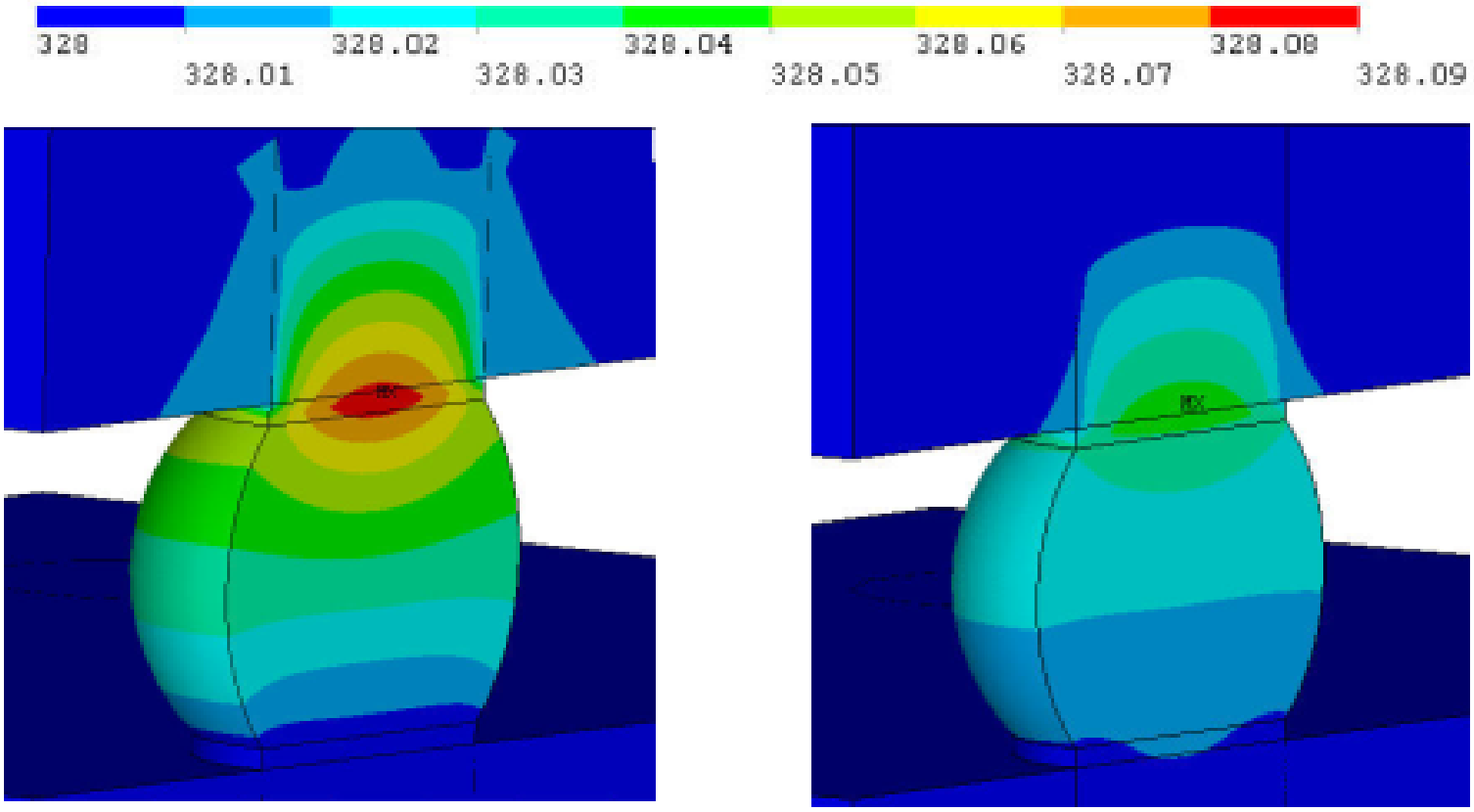
63Sn-37Pb



80Au-20Sn

Ambient Temperature = 27°C

Temperature Contours (II)



63Sn-37Pb

80Au-20Sn

Ambient Temperature = 55°C

Consideration of Heat Convection

Heat-Transfer Coefficients

Ambient Temperature = 25°C

The back of the GaAs Chip = 1.017×10^{-5} W/°C-mm^2
The side of the GaAs Chip = 2.662×10^{-5} W/°C-mm^2
The top of the GaAs Chip = 2.662×10^{-5} W/°C-mm^2
The back of the Si Chip = 2.163×10^{-5} W/°C-mm^2
The side of the Si Chip = 2.662×10^{-5} W/°C-mm^2
The top of the Si Chip = 1.017×10^{-5} W/°C-mm^2

Ambient Temperature = 55°C

The back of the GaAs Chip = 0.982×10^{-5} W/°C-mm^2
The side of the GaAs Chip = 2.596×10^{-5} W/°C-mm^2
The top of the GaAs Chip = 2.596×10^{-5} W/°C-mm^2
The back of the Si Chip = 2.142×10^{-5} W/°C-mm^2
The side of the Si Chip = 2.596×10^{-5} W/°C-mm^2
The top of the Si Chip = 0.9817×10^{-5} W/°C-mm^2

Concluding Remarks

- A new configuration of VCSEL assembly using solder-bumped flip chip interconnects is proposed
- A 3-D FE thermal analysis is performed to investigate the effect of solder materials and ambient temperature.
- 80Au-20Sn is a better choice than 63Sn-37Pb solder.
- The change of ambient temperature does not affect the pattern of temperature contours.