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Journal of Crystal Growth 310 (2008) 562–569
JOURNAL OF CRYSTAL GROWTH
www.elsevier.com/locate/jcrysgro

Selective area metalorganic vapor-phase epitaxy of gallium arsenide on silicon

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Received 19 September 2007; received in revised form 30 October 2007; accepted 6 November 2007
Communicated by R.M. Biefeld
Available online 19 November 2007

Abstract

The selective area, metalorganic vapor-phase epitaxy of gallium arsenide on silicon substrates was investigated. Low-temperature arsenic passivation of the silicon surface was realized at 650 °C. A two-step growth method was used to deposit the GaAs films with an optimum nucleation temperature of 400 °C. Layers nucleated at 350 °C or below were found to be polycrystalline whereas those nucleated at 400 °C and above were single crystal. The X-ray diffraction full-width-at-half-maximum decreased from 890 to 775 arcsec for a 1.0-μm-thick GaAs layer grown on unpatterned versus patterned Si (1 0 0) wafers. The 77 K photoluminescence peak position was 1.489 and 1.498 eV for a 1.0-μm-thick GaAs layer on unpatterned and patterned substrates, respectively. Based on the photoluminescence peak shift, we find that selective area growth of GaAs on Si improves film crystallinity while reducing the in plane strain in the film by 35%.

PACS: 68.55.Jk; 81.05.Ea; 81.15.Gh

Keywords: A3. Metalorganic chemical vapor deposition; A3. Selective epitaxy; B2. III–V Materials

1. Introduction

The growth of compound semiconductor devices on silicon substrates has long been a goal of the electronics industry. Successful monolithic integration of heterojunction and/or optoelectronic devices onto silicon-integrated circuits would allow for new and improved architectures with much greater functionality [1–5]. However, the large lattice and thermal mismatches, 4% and 63%, respectively, for GaAs on Si, and the presence of a polar/non-polar interface result in high dislocation densities in the III–V materials. These dislocations should be reduced to below $1\times10^{-5}\,\mathrm{cm}^{-2}$ in the active region of the device [5]. Much research has been devoted in solving these problems, with the best results obtained by using thick buffer layers of graded composition [6–8], by thermal annealing [9–12], and by growing the III–V semiconductors on patterned substrates [6,13,14].

Gallium arsenide films grown on silicon using graded buffer layers combined with thermal annealing have brought the dislocation density down to $\sim2\times10^{-6}\,\mathrm{cm}^{-2}$ [15]. However, the thick buffer layer can be time and materials intensive, and thermal annealing might harm previously deposited Si devices. An alternative approach to reducing the dislocation density is to decrease the epitaxial area with an inert mask [16–19]. This method, known as selective area epitaxy (SAE), has been shown to extend the critical thickness of heteroepitaxial growth [17]. Moreover, the mask can act as a barrier for the propagation of threading dislocations [19]. Metalorganic vapor-phase

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doi:10.1016/j.jcrysgro.2007.11.056

epitaxy is well suited for patterned growth of III–V compound semiconductors on silicon as the precursors show good selectivity for decomposing on the silicon and not on the silicon nitride mask [20–22]. Incoming precursor molecules that adsorb on the mask diffuse across the surface to an exposed silicon window and incorporate into the growing film [20].

In this paper, we examine the growth of gallium arsenide on blanket and patterned Si (1 0 0) substrates. Arsenic passivation of the silicon surface was realized at 650 °C. The optimum nucleation temperature for the two-step growth of GaAs on Si was measured to be 400 °C. Deposition on patterned versus unpatterned substrates led to improved material properties as measured by X-ray diffraction (XRD) and photoluminescence (PL).

2. Experimental methods

Silicon (1 0 0) substrates with a resistivity of 0.01 Ω cm and miscut 4° towards the [1 1 0] were used in these experiments. The substrates were cleaned in a 1:1:1 solution of electronic grade $HCl:H_2O_2:H_2O$ for 5 min prior to a 5.0 vol% HF dip to remove organic contaminants and the native oxide. Long trench patterns were produced on bare silicon using photolithography with a positive AZ-5214 resist. Trenches running along the [1 1 0], [$\bar{1}$ 1 0], and 45° towards the [1 1 0] direction were created using silicon nitride as the mask material. Two and five micron wide trench widths were examined, with windows separated by 4–20 μm. The HF used for patterned substrates was diluted to <1% to prevent unintentional etching of the mask. After the wet chemical treatment, the samples were immediately introduced into a Veeco Discovery TurboDisc 125 MOVPE reactor.

The clean, deoxidized Si (1 0 0) substrates were passivated with arsenic in the MOVPE reactor using tertiarybutylarsine (TBAs). The samples were exposed to 4.0×10^{-4} mol/min of TBAs at 650 °C for 2 min, followed by a 10 min anneal in flowing hydrogen. Gallium arsenide films were deposited on the passivated surface by a two-step growth method using trimethylgallium (TMGa) and TBAs. A low-temperature nucleation layer was grown at a V/III ratio of 10 and temperature of 250–550 °C, while the second-step growth was conducted at a V/III ratio of 26 and 630 °C. A deposition rate of 1.2 μm/h was observed on the unpatterned substrates.

After Si passivation and growth of GaAs, the samples were cooled to room temperature and transferred directly to an ultrahigh vacuum system where the surfaces were characterized by low energy-electron diffraction (LEED) and X-ray photoelectron spectroscopy (XPS). Next, the samples were removed from the UHV chamber and examined by XRD, PL and atomic force microscopy (AFM). The LEED patterns were obtained on a Princeton Instrument reverse-view LEED. The XPS data was taken with a physical electronics spectrometer with a hemispherical analyzer and multichannel detector. Core level spectra of the Si 2p, O 1s, Ga $2p_{3/2}$, and As $3d_{5/2}$ peaks were collected using Mg K_α X-rays with $hv = 1253.6$ eV. All spectra were taken in small area mode with a 7° acceptance angle and 23.5 eV pass energy. The XRD measurements were made on a Bede D^3 high-resolution diffractometer using Cu K_α X-rays. PL measurements were performed on a Phillips PLM 100 spectrometer using the 488 nm line of an argon laser. Atomic force micrographs were obtained on a Veeco Dimension 3100 atomic force microscope in tapping mode.

3. Results

The unpatterned Si (1 0 0) surface exhibited a LEED pattern after the wet chemical treatment as shown in in Fig. 1(a). After exposure to TBAs in the reactor at 650 °C, the surface becomes passivated with arsenic and reconstructs to a mixed phase $(1 \times 2)/(2 \times 1)$ as shown in Fig. 1(b). This LEED pattern is analogous to that produced previously by MOVPE at temperatures from 850 to 900 °C, and by MBE at 650–850 °C [23–25].

Shown in Fig. 2 is a plot of the Si 2p photoelectron peaks for the untreated, chemically cleaned, and arsenic passivated Si surfaces. Peaks for the untreated and wet-cleaned Si surfaces include deconvolution spectra. On the untreated substrate, a large peak associated with SiO_2 at 103 eV and a small shoulder associated with SiO at ~101 eV is observed. These are due to the native oxide present. After wet chemical treatment, the SiO_2 peak disappears, but the SiO shoulder at 101 eV remains, indicating a residual surface oxygen content of ~2.0%. However, after arsenic passivation this shoulder is absent from the Si peak. The arsenic coverage can be estimated by the peak-to-peak ratio of the As 3d (not shown) and Si 2p peaks of the XPS spectrum. In our case, the (As 3d)/(Si 2p) ratio is 0.21, indicating a full monolayer of As coverage on the Si surface [23].

Following passivation, gallium arsenide was deposited on the substrate. A 20-nm-thick nucleation layer was deposited at a reduced temperature followed by a 180-nm-thick GaAs film grown at 630 °C. Shown in Fig. 3 is a plot of the XRD full-width-at-half-maximum (FWHM) of the epilayer as a function of nucleation temperature. A sharp drop in the FWHM is observed between 350 and 400 °C. Full-spectrum XRD scans indicate polycrystalline facets for nucleation temperatures of 350 °C and below, whereas at 400 °C or above the films were found to be crystalline with a single orientation along the [0 0 1] direction. However, note that the FWHM increases monotonically with nucleation temperatures beyond 400 °C.

The surface quality of blanket GaAs films deposited on Si were examined *in situ* using LEED. A GaAs substrate was processed simultaneously with the Si substrate during arsenic passivation, 400 °C nucleation, and 630 °C growth. Shown in Fig. 4 are the LEED patterns obtained for a 200-nm-thick GaAs film grown on Si (1 0 0) and GaAs (0 0 1). The $c(4 \times 4)$ LEED pattern obtained on the GaAs/Si sample is indistinguishable from that obtained for GaAs/

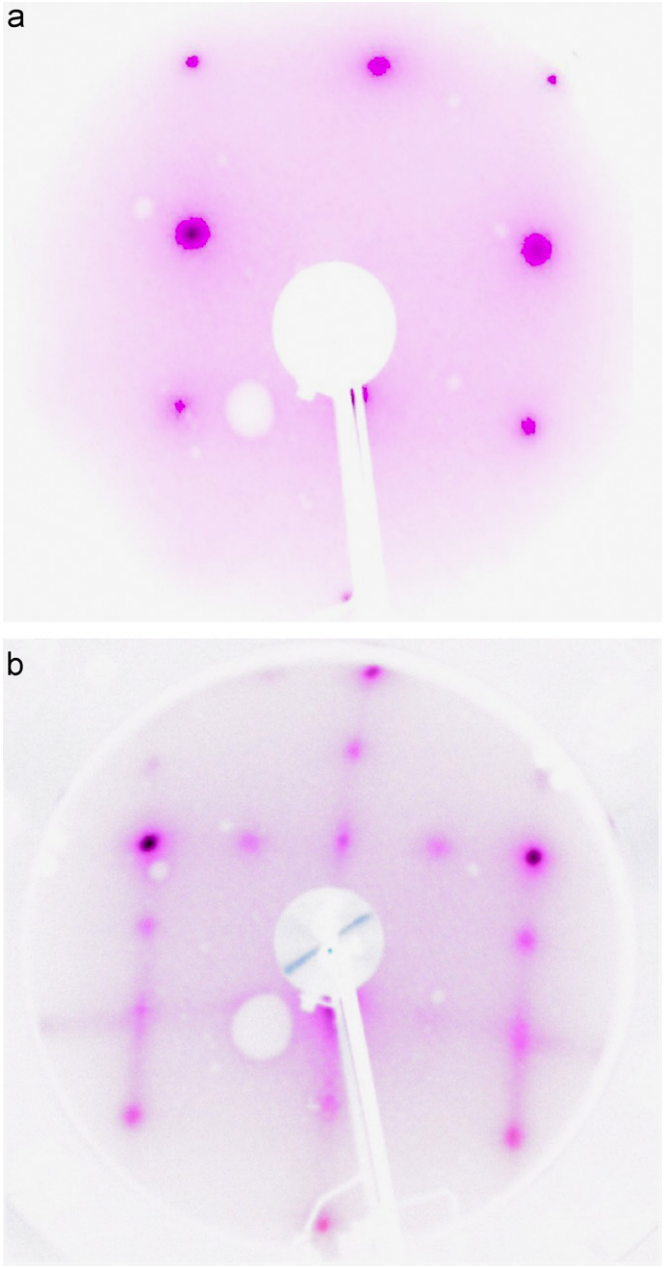

Fig. 1. Low-energy electron diffraction patterns observed for (a) chemically cleaned Si (1 0 0) at 48 eV, and (b) arsenic passivated Si (1 0 0) at 41 eV.

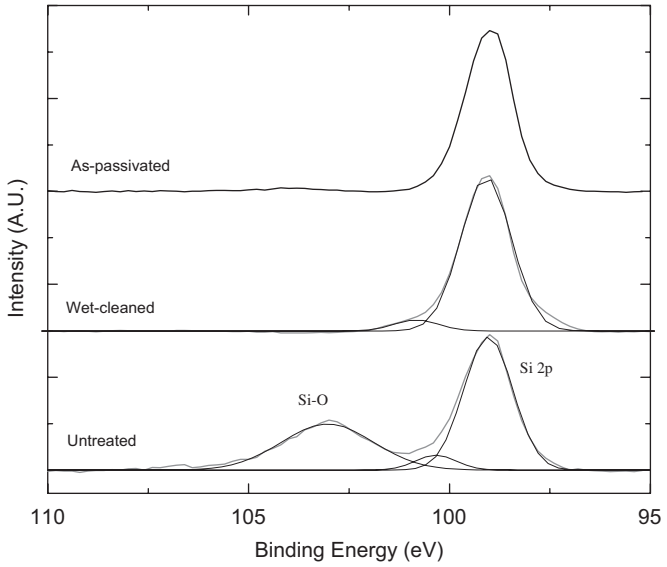

Fig. 2. X-ray photoelectron spectra of the Si 2p peak for the untreated, chemically cleaned, and arsenic passivated surfaces.

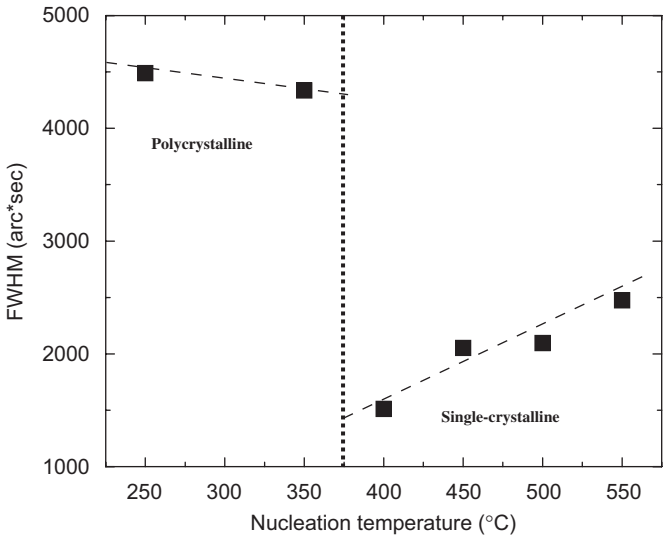

Fig. 3. X-ray diffraction measured full-width-half-maximum for 200-nm-thick GaAs films growth on Si as a function of nucleation temperature.

GaAs. Similar, but weaker, GaAs/Si LEED patterns were observed for nucleation temperatures of 450 and 500 °C. Based on the results shown here and in Fig. 3, subsequent deposition of GaAs on patterned Si (1 0 0) was performed with nucleation at 400 °C.

Shown in Fig. 5 is an atomic force micrograph of an Si substrate patterned with trenches along the [1 1 0] direction. The nitride mask is approximately 120 nm thick and the trench sidewalls are vertical as indicated by the linescan in the figure. The trench width and separation distance equal 2.2 and 3.8 μm, respectively. The root-mean-squared (RMS) roughness over a 10 μm^2 area of the exposed silicon in the trench is 5.6 nm. Note that this silicon has a native oxide on it. Excellent pattern transfer was repeated over the entire substrate for all trench widths and separation distances.

Gallium arsenide films were deposited on the patterned substrate using identical conditions developed for the unpatterned silicon substrates above. Shown in Fig. 6 is an atomic force micrograph of GaAs deposited into 2.0-μm-wide trenches spaced apart by 16.0 μm and oriented in the [1 1 0] direction. Note that the x and y axes are not to scale. Excellent selectivity is achieved with minimal GaAs nucleation on the nitride mask. Growth in trenches aligned along the $[\bar{1}\,1\,0]$ and 45° towards [1 1 0] exhibit similar surface features. The RMS roughness over a 10 μm^2 area of GaAs in this figure is 26.6 ± 1.3 nm. This may be compared

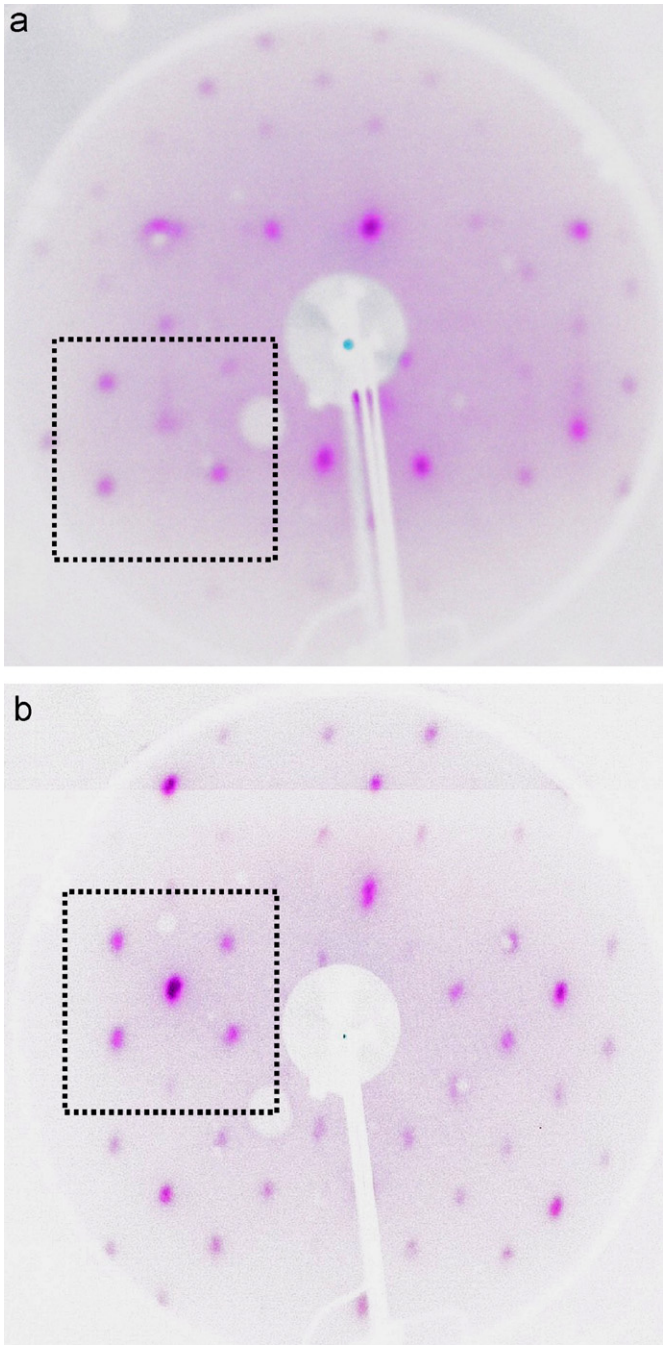

Fig. 4. Low energy electron diffraction patterns observed for a 200-nm-thick GaAs film deposited simultaneously on (a) Si (1 0 0), 39 eV and (b) GaAs (0 0 1), 44 eV. The $c(4\times4)$ unit cell is outlined.

to the RMS roughness measured for blanket GaAs films on Si (1 0 0), which is equal to 23.6 ± 1.2 nm. One will notice when looking at the linescan of Fig. 6 that the GaAs strips are not vertical, but instead are tapered with a base and top width of 8.0 and 4.0 μm, respectively, and with a height of 1.2 μm.

The base width of GaAs deposited in 2.0-μm-wide trenches increases with mask separation distance is shown in Fig. 7. In the case of 4.0 μm separations, adjacent GaAs strips nearly coalesce. Gallium arsenide strips oriented

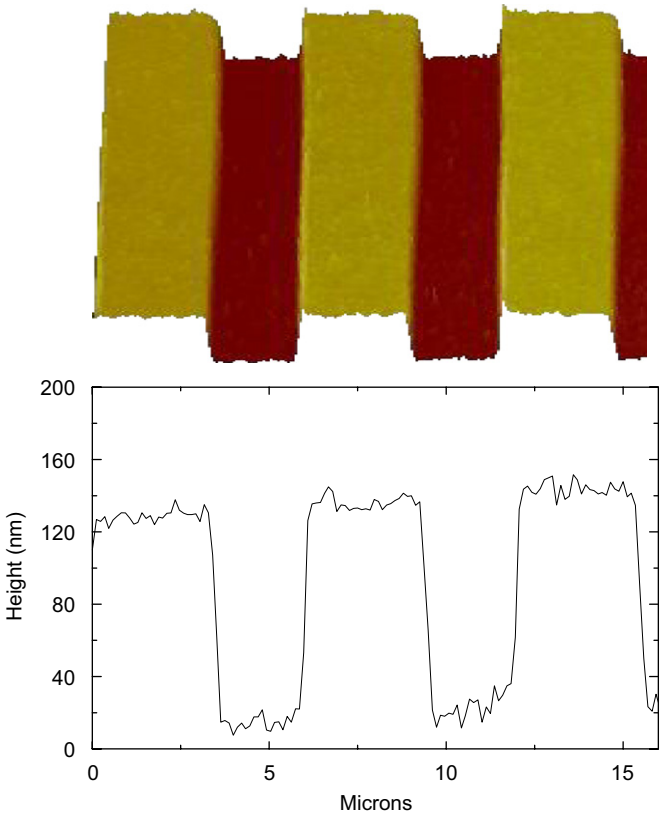

Fig. 5. Atomic force micrograph and linescan of 2.0-μm-wide trenches separated by 4.0 μm of silicon nitride along the [1 1 0] direction. Scan size $16\times16\,\mu m^2$.

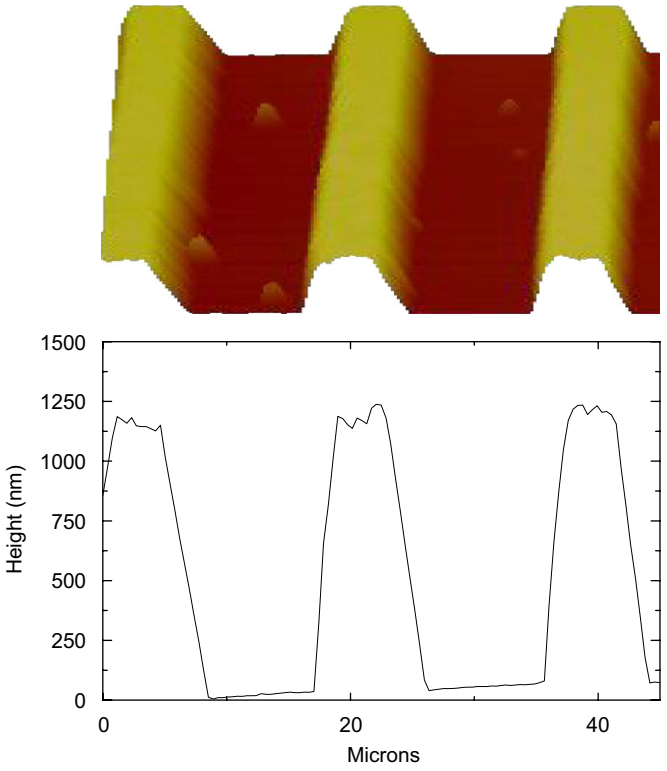

Fig. 6. Atomic force micrograph and linescan of GaAs deposited on 2.0-μm-wide trenches separated by 16.0 μm of silicon nitride along the [1 1 0] direction. Scan size $45\times45\,\mu m^2$.

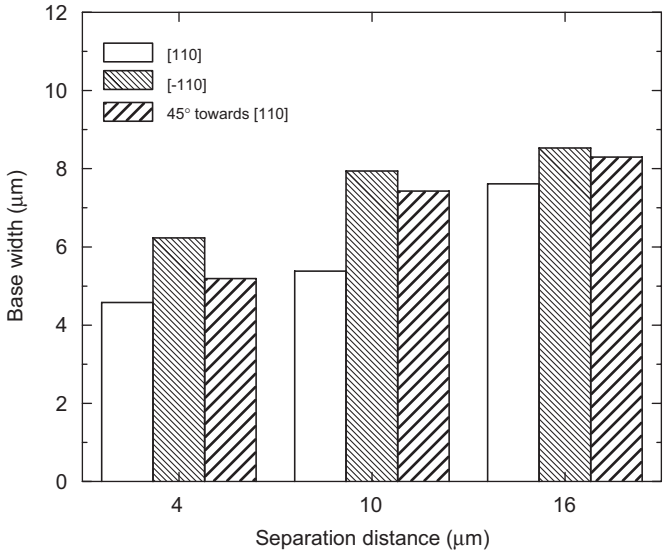

Fig. 7. Base widths of GaAs deposited on 2.0-μm-wide trenches as a function of separation distance and trench orientation.

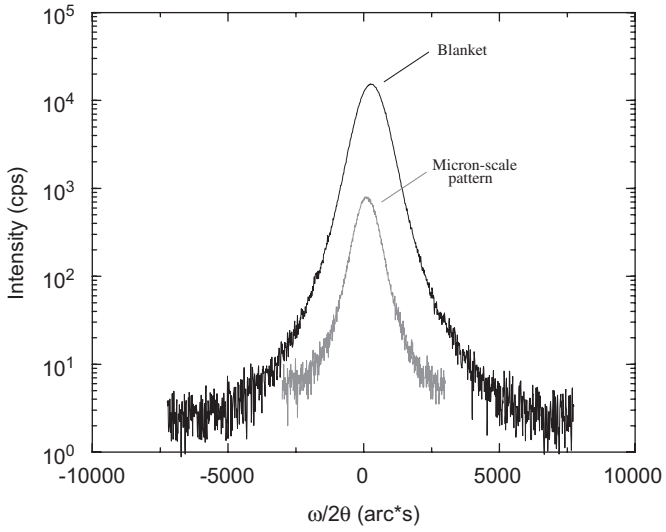

Fig. 8. X-ray diffraction rocking curves for GaAs deposited on blanket and patterned Si (1 0 0) substrates. The film thickness is 1.0 μm.

along the [$\bar{1}$ 1 0] and 45° towards the [1 1 0] directions are wider than those oriented along the [1 1 0].

The XRD rocking curves about the (0 0 4) reflection of GaAs films deposited on unpatterned and patterned Si (1 0 0) substrates are shown in Fig. 8. The epilayer thickness in each case was 1.0 μm. The FWHM of these two films is 890 and 775 arcsec, respectively. A 13% reduction in the FWHM is observed for growth on the patterned substrate. Note that the lower intensity from the patterned sample is due to a reduced sample area.

Scanning electron micrographs corresponding to the samples examined in Fig. 8 are presented in Fig. 9. The patterned sample shown in Fig. 9b consists of 2.0-μm-wide trenches oriented along the [1 1 0] separated by 14 μm of

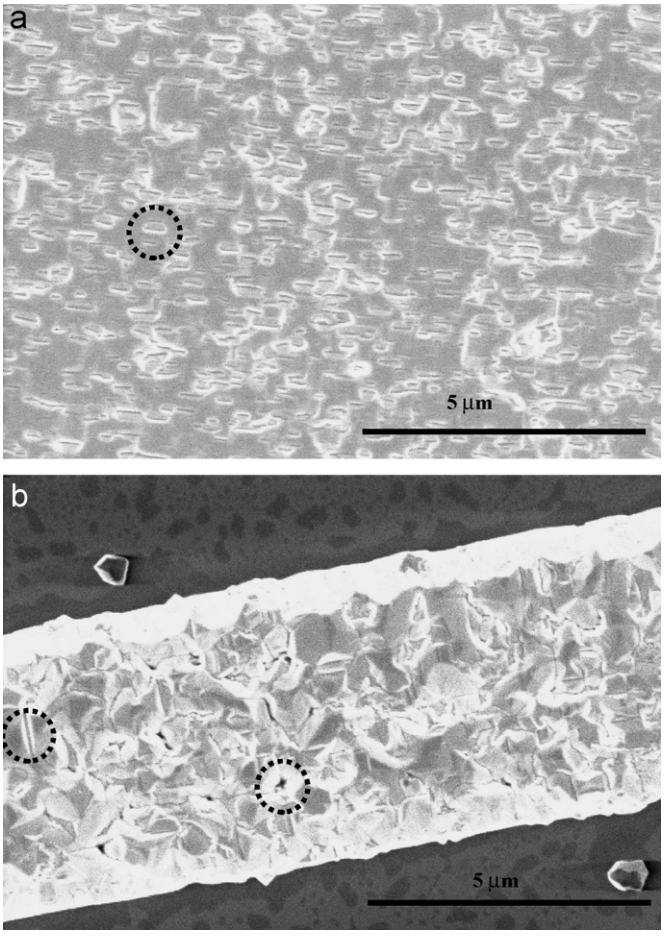

Fig. 9. Scanning electron micrograph of 1.0 μm GaAs deposited on (a) unpatterned, and (b) patterned Si substrates. Rectangular block, pinhole, and boundary defect structures are circled.

silicon nitride. Clearly, both surfaces are rough and exhibit a high density of defect structures. These structures appear as rectangular blocks, pinholes, and boundaries as indicated in the figures. A rough estimate of the density of these structures is 7.7×10^{8} and $5.5\times10^{8}\,cm^{-2}$ for Fig. 9(a) and (b), respectively.

Low-temperature (77 K) PL peak positions, FWHM, and thicknesses for GaAs films grown on GaAs (0 0 1), unpatterned Si (1 0 0), and patterned Si (1 0 0) are listed in Table 1. The peak position for a 2.0-μm-thick GaAs film shifts from 1.513 ± 0.002 to 1.484 ± 0.002 eV for growth on GaAs and Si substrates, respectively. A reduced shift is seen for 1.0-μm- thick GaAs layers. The observed red shift on Si substrates is due to biaxial strain. The larger red shift for the 2.0-μm-thick versus 1.0-μm-thick GaAs layer on unpatterned Si indicates an increase in strain with film thickness. On the other hand, growing GaAs on patterned Si results in less of a shift of the PL peak. The peak position for 1.0 and 2.0 μm GaAs grown on patterned silicon is 1.498 and 1.500 eV, respectively. In this case, less strain is observed for the thicker film.

Table 1
Low-temperature (77 K) photoluminescence peak position, FWHM, and film thickness for GaAs films deposited on GaAs and Si substrates

Substrate	Peak position (eV)	FWHM (meV)	Thickness (μm)
GaAs (0 0 1)	1.513±0.001	22±3	2.0
Si (1 0 0) 4°→[1 1 0]	1.489±0.002	37±4	1.0
Si (1 0 0) 4°→[1 1 0]	1.484±0.002	25±3	2.0
μm patterned Si (1 0 0) 4°→[1 1 0]	1.498±0.002	32±3	1.0
μm patterned Si (1 0 0) 4°→[1 1 0]	1.500±0.002	39±4	2.0

4. Discussion

Low-temperature passivation was achieved by exposing the hydrogen-terminated Si (1 0 0) to tertiarybutylarsine at 650 °C. A trace amount of oxygen remained on the silicon surface after HF etching, but it desorbed after TBAs exposure at 650 °C. After this step, the surface becomes terminated with As dimers as indicated by the (2 × 1)/(1 × 2) LEED pattern of Fig. 1(b). The oxygen may have been removed from the surface as water by reaction with the hydrogen supplied from the TBA, or it could have desorbed as AsO, which has been observed on GaAs at 582 °C [24,26].

The mixed-phase LEED pattern indicates that the surface is covered with single-height steps. It is preferable to have a single domain (2 × 1) or (1 × 2), i.e. with all double-height steps, so as to prevent anti-phase domains from forming. This structure has been obtained by several groups on single-domain Si (1 0 0) starting surfaces [27–29]. However, obtaining a single-domain As-passivated structure on Si (1 0 0) surfaces that are not originally single domain is difficult. Bringans et al. [23], have shown that the interaction of As with vicinal Si surfaces is complicated by competition between kinetic and energetic effects, which result in the formation of both the (2 × 1) and (1 × 2) domains. The mixed phase (2 × 1)/(1 × 2) structure has been shown to be stable up to 900 °C [23–25]. The maximum safe operating temperature in the Veeco MOVPE reactor is 850 °C.

The deposition of a nucleation layer at reduced temperature followed by a thick layer deposited at elevated temperature is a well-known technique for growing III–V materials on Si [5,6,8–10,23,30,31]. The temperature at which a film nucleates determines the density and size of 3D nuclei. Lower temperatures ensure that many small GaAs islands coalesce, resulting in more efficient APD annihilation [30]. The subsequent growth at elevated temperature ensures that the material is highly crystalline. In this work, we find that the optimum nucleation temperature is 400 °C, as shown in Fig. 3. The high FWHM found below 400 °C is accompanied by polycrystalline reflections in the XRD spectrum. Non-uniform polycrystalline domains have been observed previously for growth below this temperature [32,33]. Above 400 °C, the entire epilayer is oriented in the [0 0 1] direction, exhibiting a single reflection in the XRD spectrum.

Takasugi and coworkers [31] have shown that nucleation at high temperature causes large GaAs nuclei to form that accommodate strain by forming "type II" dislocations, i.e. stacking faults, micro-twins, and threading dislocations inside the island. Conversely, low nucleation temperatures result in small islands forming on the terraces of the Si surface that relieve strain by introducing "type I" dislocations, i.e. edge or 90° misfit dislocations at steps where the edges of adjacent islands meet. Type I dislocations are more efficient in accommodating mismatch because their Burgers vectors are parallel to the growth plane, whereas the type II Burgers vectors propagate at an angle to the surface plane [5]. Therefore, more type II dislocations are required to accommodate a given mismatch than type I. We suspect that the observed peak broadening with increasing nucleation temperature above 400 °C may be due to increasing initial island size and preferential formation of type II dislocations.

Growth on patterned substrates led to a trapezoidal film shape with the base significantly wider than the top. The trapezoidal shape is expected for selective area growth of GaAs in trenches oriented along the [1 1 0] direction, which produces facets in the {1 1 1}B and {3 1 1}B planes near the mask edge [34]. This faceting is predicted for selective area deposition as a result of surface energy minimization during growth in a confined geometry [34–36]. The growth rate of GaAs on the (3 1 1) plane is nearly equal to that on the (1 0 0) plane, while that on the (1 1 1) plane is much less [36]. Because the (3 1 1) plane is inclined at an angle of 18.5° from the surface, growth on this plane results in more material in the lateral rather than vertical direction. Inspection of Figs. 6 and 7 reveals that the base of the GaAs strip is significantly wider than the pattern width, which indicates lateral overgrowth extending over the silicon nitride mask due to an enhanced growth rate at the mask edge. This phenomenon has been reported by numerous groups [37–39]. In our case, the ratio of lateral to vertical growth is approximately two. One would expect this ratio to be closer to unity based on the growth rates on the (1 0 0) and (3 1 1) planes. We presume that diffusing adatoms from the mask incorporate in the (3 1 1) plane before they reach the (1 0 0) plane, contributing to an increase in lateral growth rate.

A variation of the base width is observed with orientation, as shown in Fig. 7. This is an unexpected result, as surface diffusion on an amorphous silicon nitride mask should be isotropic. Sugiyama and coworkers have observed anisotropic lateral edge growth in their study of selective area epitaxy of InP [38]. A modified gas-phase diffusion model incorporating migration lengths of adatoms on the mask and film was employed to explain their results. It was found that anisotropic migration lengths on the film, and not on the mask, determine edge growth size [38]. Based on Sugiyama's model, we relate the larger strip widths in the [$\bar{1}$ 1 0] direction to the larger Ga

adatom migration length documented for the [$\bar{1}$ 1 0] direction [40].

The crystal structure of a 1.0 μm thick gallium arsenide film improves when deposited on patterned Si, as indicated by the drop of the (0 0 4) rocking curve FWHM from 890 to 775 arcsec. This improvement indicates larger grain sizes for the film deposited on the patterned substrate compared to the unpatterned substrate. This is consistent with the estimated density of defect structures observed in the SEM images presented in Fig. 9. The decrease in intensity observed on the patterned substrate is due to a reduction in sample area. The tenfold drop in intensity is consistent with the decrease in total GaAs material due to the patterning.

The PL measurements provide an alternative means to measure strain. The shift of the GaAs peak to a lower energy on Si substrates indicates the film is under tension [41]. Although band splitting may contribute to the shift, it is expected to be much less than that from strain. Approximating the shift in peak position as due solely to strain, we can estimate the normal stress and in-plane strain for the 1.0-μm-thick GaAs blanket layer to be 1.2 kbar and 1.0×10^{-3}, respectively [41,42]. For the patterned substrate, the redshift decreases from 24 to 15 meV, indicating a reduction of the normal stress and in-plane strain to 0.8 kbar and 6.5×10^{-4}, respectively.

The stress and in-plane strain for a 2.0 μm GaAs film grown on unpatterned Si increases to 1.4 kbar and 1.2×10^{-3}, respectively. The increase in strain is due to an increased film thickness. Conversely, increasing the GaAs thickness from 1.0 to 2.0 μm on the patterned Si actually decreases the stress and in plane strain to 0.7 amd 5.7×10^{-4}, respectively. We surmise this strain relief is accomplished in a manner similar to epitaxial lateral overgrowth (ELO), where laterally grown material is demonstrated to result in improved material qualities [43].

5. Conclusions

In summary, we have developed a procedure for growing crystalline gallium arsenide films on silicon substrates by metalorganic vapor-phase epitaxy. The properties of the films improve when deposited on substrates patterned with silicon nitride. Photoluminescence and X-ray diffraction data presented in this work are consistent with significant strain relieve being provided by the selective growth in trenches. The estimated in-plane strain for a 1.0-μm-thick GaAs film was reduced from 1.0×10^{-3} on unpatterned Si (1 0 0) to 6.5×10^{-4} on Si_3N_4-patterned Si (1 0 0). The in-plane strain for 2.0-μm-thick GaAs layers was reduced from 1.2×10^{-3} to 5.7×10^{-4} on unpatterned and Si_3N_4-patterned Si (1 0 0) substrates, respectively.

Acknowledgements

Funding for this research was provided by Intel Corporation and the UC-MICRO Program.

References

[1] J.F. Geisz, D.J. Friedman, Semicond. Sci. Technol. 176 (2002) 769.
[2] D.L. Mathine, IEEE J. Sel. Top. Quantum Electron. 3 (1997) 952.
[3] S.A. Ringle, J.A. Carlin, C.L. Andre, M.K. Hudait, M. Gonzalez, D.M. Wilt, E.B. Clark, P. Jenkins, D. Scheiman, A. Allerman, E.A. Fizgerald, C.W. Leitz, Prog. Photovoltaics 10 (2002) 417.
[4] H. Yonezu, Y. Furukawa, H. Abe, Y. Yoshikawa, S.Y. Moon, A. Utsunu, Y. Yoshizumi, A. Wakahara, M. Ohtani, Opt. Mater. 27 (2005) 799.
[5] S.F. Fang, K. Adomi, S. Iyer, H. Morkoc, H. Zabel, C. Choi, N. Otsuka, J. Appl. Phys. 68 (1990) R31.
[6] G. Vanamu, A.K. Datye, R. Dawson, S.H. Zaidi, Appl. Phys. Lett. 88 (2006) 251909.
[7] S. Datta, G. Dewey, J.M. Fastenau, M.K. Hudait, D. Loubychev, W.K. Liu, M. Radosavljevic, W. Rachmady, R. Chau, IEEE Electron. Device Lett. 28 (2007) 685.
[8] F.K. Legoues, B.S. Meyerson, J.F. Morar, P.D. Kirchner, J. Appl. Phys. 71 (1992) 4230.
[9] G. Radhakrishnan, O. McCullough, J. Cser, J. Katz, Appl. Phys. Lett. 52 (1988) 731.
[10] N. Chand, R. Fischer, A.M. Sergent, D.V. Lang, S.J. Pearton, A.Y. Cho, Appl. Phys. Lett. 51 (1987) 1013.
[11] N. Chand, J. Allam, J.M. Gibson, F. Capasso, F. Beltram, A.T. Macrander, A.L. Hutchinson, L.C. Hopkins, C.G. Bethea, B.F. Levine, Y. Cho, J. Vac. Sci. Technol. B 5 (1987) 822.
[12] N. Chand, R. People, F.A. Baiocchi, K.W. Wecht, A.Y. Cho, Appl. Phys. Lett. 49 (1986) 815.
[13] H.P. Lee, S. Wang, Y.H. Huang, P. Yu, Appl. Phys. Lett. 52 (1988) 215.
[14] H.P. Lee, X. Liu, S. Wang, Appl. Phys. Lett. 56 (1990) 1014.
[15] J.A. Carlin, S.A. Ringel, A. Fitzgerald, M. Bulsara, Sol. Energy Mater. Sol. Cells 66 (2001) 621.
[16] D.B. Noble, J.L. Hoyt, C.A. King, J.F. Gibbons, T.I. Kamins, M.P. Scott, Appl. Phys. Lett. 56 (1990) 51.
[17] R. Hull, J.C. Bean, G.S. Higashi, M.L. Green, L. Peticolas, D. Bahnck, D. Brasen, Appl. Phys. Lett. 60 (1992) 1468.
[18] E.A. Fitzgerald, G.P. Watson, R.E. Proano, D.G. Ast, P.D. Kirchner, G.D. Pettit, J.M. Woodall, J. Appl. Phys. 65 (1989) 2220.
[19] J. Lee, H. Kim, M. Bao, K.L. Wang, Thin Solid Films 508 (2006) 10.
[20] B. Korgel, R.F. Hicks, J. Crystal Growth 151 (1995) 204.
[21] K. Yamaguchi, K. Okamoto, Jpn. J. Appl. Phys. 29 (1990) 2351.
[22] C. Blaauw, A. Szaplonczay, K. Fox, B. Emmerstorfer, J. Crystal Growth 77 (1986) 326.
[23] R.B. Bringans, D.K. Biegelsen, L.E. Swartz, Phys. Rev. B 44 (1991) 3054.
[24] T. Hannappel, W.E. McMahon, J.M. Olson, J. Crystal Growth 272 (2004) 24.
[25] T. Bork, W.E. McMahon, J.M. Olson, T. Hannappel, J. Crystal Growth 298 (2007) 54.
[26] A.J. SpringThorpe, S.J. Ingrey, B. Emmerstorfer, P. Mandeville, W.T. Moore, Appl. Phys. Lett. 50 (1987) 77.
[27] M. Kawabe, T. Ueda, H. Takasugi, Jpn. J. Appl. Phys. 26 (1987) L114.
[28] R.S. Becker, T. Klitsner, J.S. Vickers, J. Microsc. 152 (1988) 157.
[29] J. Varrio, H. Asonen, J. Lammasniemi, K. Rakennus, M. Pessa, Appl. Phys. Lett. 55 (1989) 1987.
[30] A. Georgakilas, P. Panayotatos, J. Stoemenos, J.L. Mourrain, A. Christou, J. Appl. Phys. 71 (1992) 2679.
[31] H. Takasugi, M. Kawabe, Y. Bando, Jpn. J. Appl. Phys. 26 (1987) L584.
[32] W.C. Chen, C.S. Chang, W.K. Chen, Jpn. J. Appl. Phys. 36 (1997) 3649.
[33] R.M. Lum, J.K. Klingert, M.G. Lamont, Appl. Phys. Lett. 50 (1987) 284.
[34] H. Kuriyama, M. Ito, K. Suzuki, Y. Horikoshi, Jpn. J. Appl. Phys. 39 (2000) 2457.

[35] S.C. Lee, L.R. Dawson, S.R.J. Brueck, J. Crystal Growth 240 (2002) 333.
[36] M. Dilger, M. Hohenstein, F. Phillipp, K. Eberl, Semicond. Sci. Technol. 9 (1994) 2258.
[37] D.G. Coronell, K.F. Jensen, J. Crystal Growth 114 (1991) 581.
[38] M. Sugiyama, N. Waki, Y. Nobumori, H. Song, T. Nakano, T. Arakawa, Y. Nakano, Y. Shimogaki, J. Crystal Growth 287 (2006) 668.
[39] R. Bhat, J. Crystal Growth 120 (1992) 362.
[40] M. Hata, T. Isu, A. Watanabe, Y. Katayama, J. Vac. Sci. Technol. B 8 (1990) 692.
[41] S.C. Jain, M. Willander, H. Maes, Semicond. Sci. Technol. 11 (1996) 641.
[42] S. Zemon, S.K. Shastry, P. Norris, C. Jagannath, G. Lambert, Solid State Commun. 58 (1986) 457.
[43] R.P. Gale, R.W. McClelland, J.C.C. Fan, C.O. Bozler, Appl. Phys. Lett. 41 (1982) 545.