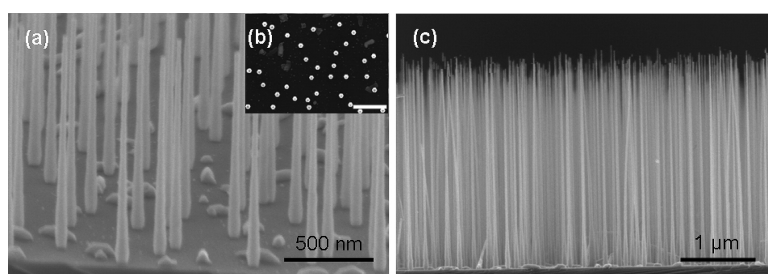


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Self-Catalyzed Epitaxial Growth of Vertical Indium Phosphide Nanowires on Silicon

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ABSTRACT

Vertical indium phosphide nanowires have been grown epitaxially on silicon (111) by metalorganic vapor-phase epitaxy. Liquid indium droplets were formed in situ and used to catalyze deposition. For growth at 350 °C, about 70% of the wires were vertical, while the remaining ones were distributed in the 3 other <111> directions. The vertical fraction, growth rate, and tapering of the wires increased with temperature and V/III ratio. At 370 °C and V/III equal to 200, 100% of the wires were vertical with a density of $\sim 1.0 \times 10^9 \text{ cm}^{-2}$ and average dimensions of 3.9 μm in length, 45 nm in base width, and 15 nm in tip width. X-ray diffraction and transmission electron microscopy revealed that the wires were single-crystal zinc blende, although they contained a high density of rotational twins perpendicular to the <111> growth direction. The room temperature photoluminescence spectrum exhibited one peak centered at $912 \pm 10 \text{ nm}$ with a FWHM of $\sim 60 \text{ nm}$.

Semiconductor nanowires have attracted considerable interest due to their intriguing physical properties and potential applications in nanoelectronics, optoelectronics, and sensors.^{1–29} The growth of III/V nanowires on silicon would be an important step forward in integrating high-speed compound semiconductors with mainstream silicon technology.^{13–23} Heteroepitaxy has been observed for several nanowire materials: ZnO on Al₂O₃(110),⁶ Ge on Si(100) and Si(111),^{10,12} InP on Si(100), Si(111) and Ge(111),^{14–19} GaAs on Si(111),²³ and GaN on Al₂O₃(0001).²⁹

Indium phosphide (InP) is a key building block in III/V heterojunction devices. The lattice parameter of InP is 8.1% larger than that of silicon, and in bulk epitaxial films this mismatch generates strain that is relieved through the formation of dislocations. Indium phosphide nanowires have been grown on silicon using gold as the catalyst.^{14–19} The wires are generated by the well-known vapor–liquid–solid (VLS) mechanism, in which the metalorganic precursors decompose on the gold and incorporate into the crystal at

the liquid–solid interface.³⁰ As already noted, InP wires will grow epitaxially on silicon, and in the case of (111) substrates, vertical growth has been observed.^{14–17} Recently, indium has been explored as a substitute catalyst for gold.^{20,21} Indium has the advantage that it is compatible with silicon integrated circuit fabrication. Also, the In droplets may be generated in situ immediately before InP crystal growth, thus eliminating separate catalyst preparation steps.

In this letter, we demonstrate that highly uniform, vertical, single-crystal indium phosphide nanowires can be grown epitaxially on Si(111) by metalorganic vapor phase epitaxy (MOVPE) using indium as the catalyst. The effects of the process conditions on the vertical fraction, growth rate, and extent of tapering have been determined. In addition, the zinc blende crystal structure of the InP nanowires has been examined by X-ray diffraction (XRD) and transmission electron microscopy (TEM).

The experiments were carried out in a Veeco D125 MOVPE reactor using trimethylindium (TMIn) and tertiarybutylphosphine (TBP) as the precursors. The Si(111) substrates were miscut 4° towards the <110>, and boron doped with a resistivity of 1932 to 2110 $\Omega\cdot\text{cm}$. The Si(100) substrates were miscut 6° towards the <110>, and arsenic doped with a resistivity less than 0.004 $\Omega\cdot\text{cm}$. Right before being loaded into the reactor, the Si wafers were cleaned by

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the following procedure: degreased in acetone, methanol, and then isopropanol; rinsed in deionized water three times; dipped in electronic-grade HCl/H₂O₂/H₂O (1:1:1) solution for 5 min; rinsed in deionized water; and oxide etched with 5 vol % HF in deionized H₂O for 5 min. Next, the samples were loaded into the MOVPE reactor and heated to the growth temperature, which ranged from 300 to 375 °C for Si(100) and 320 to 380 °C for Si(111). Note that the accuracy of the temperature measurement was estimated to be ± 25 °C.

Indium droplets were deposited onto the Si surfaces by feeding TMIIn into the reactor with a flow rate of 5.4 $\mu\text{mol}/\text{min}$ for 5 s. After that, a soak interval of 30 s was used to create a uniform distribution of droplets of about the same size (see Figure S1 in Supporting Information). Then both TMIIn and TBP were introduced into the reactor to grow the InP nanowires. The flow rate of TBP was varied from 0.27×10^{-3} to 1.08×10^{-3} mol/min at a constant TMIIn flow of 5.4 $\mu\text{mol}/\text{min}$. The corresponding V/III ratio ranged from 50 to 200. The total pressure in the reactor during growth was 60 Torr. The growth of InP nanowires was terminated by switching off the indium supply while maintaining the TBP supply until the samples had been cooled down to room temperature.

The InP nanowires on silicon were characterized by scanning electron microscopy (SEM), TEM, XRD, and photoluminescence spectroscopy (PL). The SEM measurements were made on a Hitachi S4700 field emission scanning electron microscope. Double-axis high-resolution XRD measurements were performed on a Bede D¹ diffractometer equipped with a Maxflux focusing graded X-ray mirror and a two bounce Si 220 channel-cut collimator crystal, using Cu K α_1 radiation from a sealed X-ray tube. For triple-axis measurements a dual channel two bounce Si 220 analyzer crystal (DCA) was moved into the diffracted beam.³¹ The PL measurements were made at room temperature using the 659 nm line of a diode laser. The TEM measurements were obtained on a FEI Titan 300 kV scanning transmission electron microscope. In some cases, the wires were exfoliated from the Si substrate and placed on a TEM grid. For images of the wire-substrate interface, the sample was prepared by a lift-off technique, slicing a thin vertical cross-section using a focused Ar⁺ ion beam in an FEI Nova 600 dual-beam focused ion beam (FIB)-SEM system.

A top-view SEM image of InP nanowires deposited on Si(100) is shown in Figure 1a. The process conditions were 370 °C and a V/III ratio of 200. The growth time was 25 min. In the image, the nanowires appear bright, while the darker grey contrast underneath them is due to a thin layer of interconnected InP islands. The density of the nanowires is about $2.0 \times 10^9 \text{ cm}^{-2}$. The nanowires are tapered with a tip diameter of 20 ± 3 nm and a base diameter of 30 ± 5 nm. The length of the nanowires is 850 ± 50 nm. There are four orientations of the wires with in-plane components at 90° from each other. These correspond to the four <111> directions that can be extracted from the (100) crystal plane. As shown in Figure 1c, the four orientations form a 35.3° angle with the surface and are at 90° angles from each other.

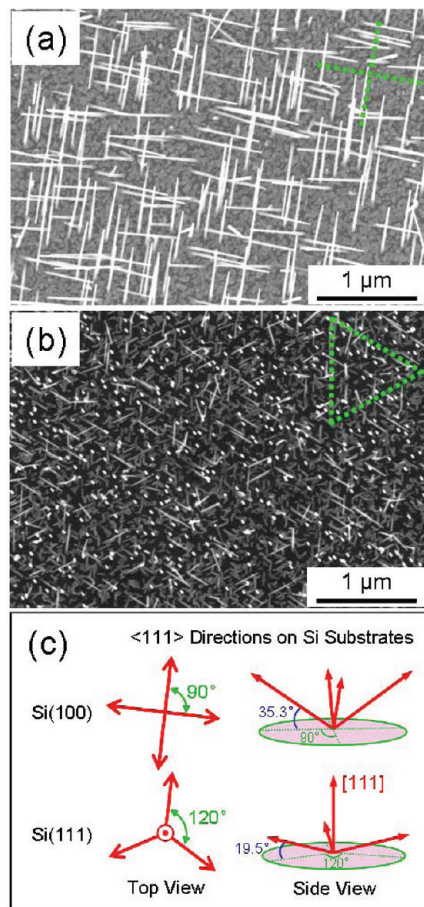


Figure 1. Top view scanning electron micrographs of InP nanowires on (a) Si(100) and (b) Si(111). (c) Schematic showing the <111> directions for the Si(100) and Si(111) substrates.

These results indicate that the InP nanowires grow along the <111> directions, which is in agreement with earlier work.^{14–19}

A top-view SEM image of InP nanowires deposited on Si(111) is presented in Figure 1b. The process conditions were 350 °C and a V/III ratio of 200. The growth time was 6 min. The nanowires appear as three white lines each rotated 120° from each other. Additional wires are orientated perpendicular to the surface and appear as small bright spots. The density of the nanowires is about $4.6 \times 10^9 \text{ cm}^{-2}$. The wires exhibit a uniform diameter of 45 ± 5 nm, and their length is 290 ± 100 nm. On the basis of Figure 1b, about 69% of the as-grown nanowires are vertical. The orientations seen in the image correspond to the four <111> directions that emerge from the (111) crystal plane; one is perpendicular to the surface, while the other three form a 19.5° angle with the surface and a 120° angle with respect to each other, as shown in Figure 1c.

The above results indicate that it is feasible to grow vertical InP nanowires on Si(111), but not on Si(100). We find that by increasing the temperature to 370 °C and maintaining the V/III ratio at 200, it is possible to grow 100% vertical nanowires on Si(111). An image of this material is presented in Figure 2. In the top view (inset b), the wires appear as bright white spots. The density of the nanowires is $1.0 \times 10^9 \text{ cm}^{-2}$. Note that there is about the same number of indium

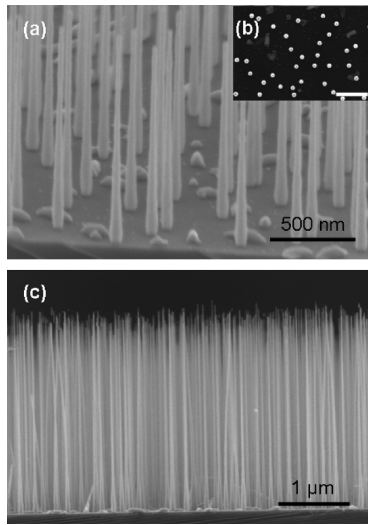


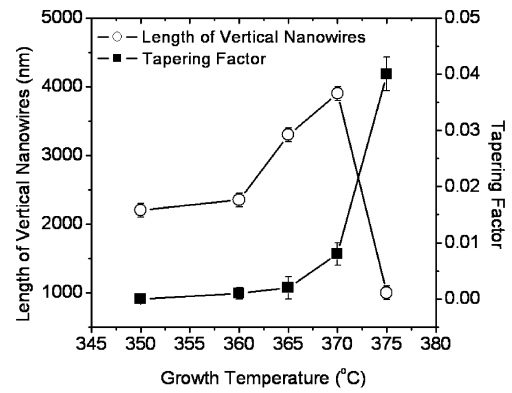
Figure 2. Scanning electron micrographs of vertical InP nanowires on Si(111): (a) tilted view, (b) top view, and (c) side view.

droplet nucleation sites on the silicon surface. A similar density of InP nanowires have been reported previously for gold catalysts on Si(111).^{14–18} Nevertheless, the length of the nanowires is $3.9 \pm 0.2 \mu\text{m}$, which is much longer than that has been seen before. The remainder of the paper will focus on the results obtained with Si(111).

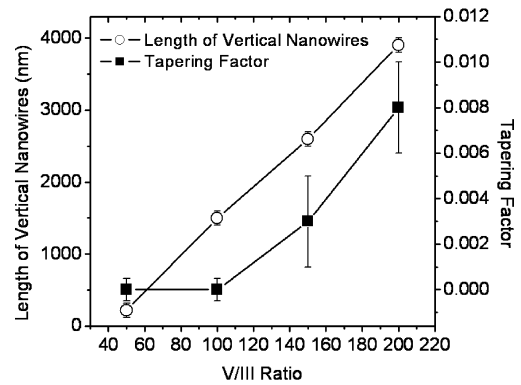
The temperature is the most important parameter for the growth of vertical nanowires. At 325 °C, the nanowires are randomly oriented. At 350 °C, the nanowires grow in the four $\langle 111 \rangle$ directions emanating from the Si substrate. As the temperature is raised further, the vertical fraction of the wires increases until at 370 °C when they are all vertical. The temperature also affects the growth rate and tapering factor. The tapering factor is defined as $(D_{\text{base}} - D_{\text{tip}})/L$, where D_{base} , D_{tip} , and L are the base diameter, tip diameter, and length of the nanowires. Shown in Figure 3a is the dependence of the nanowire length and tapering factor on temperature. In these experiments, the V/III ratio is 200 and the growth time is 25 min. Here, the data were taken from vertical nanowires. The nanowire length increases from 350 to 370 °C, then falls dramatically as the temperature rises to 375 °C. As for the tapering factor, it is 0.00 up to 365 °C, and then jumps up to 0.04 as the temperature is raised to 375 °C.

Figure 3b shows the dependence of the nanowire length and the tapering factor on V/III ratio. In these experiments, the temperature is 370 °C and the growth time is 25 min. The nanowire length increases from near zero to 3900 nm with increasing V/III ratio from 50 to 200. At the same time, the tapering factor rises slightly from 0.000 to 0.008. These results show that high V/III ratios are required to obtain vertical wires with preferred length-to-diameter ratios exceeding 50 and with minimal tapering.

Figure 4 shows the normalized room-temperature photoluminescence spectra of the nanowires. Results for several samples are presented where deposition was carried out at different temperatures and V/III ratios. For nanowires grown at 360 °C and V/III = 200, the PL peak position is 922 nm,



(a)



(b)

Figure 3. (a) Dependence of the nanowire length and the tapering factor on the temperature and (b) dependence of the nanowire length and the tapering factor on the V/III ratio.

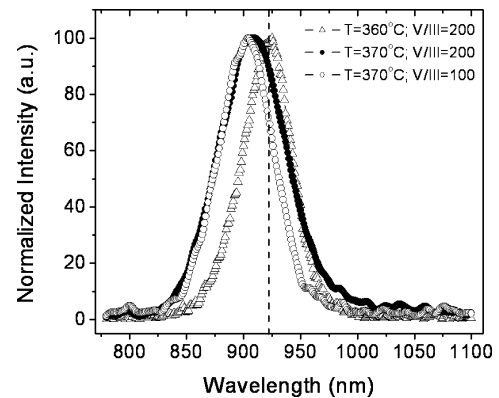


Figure 4. Normalized room temperature photoluminescence spectra of InP nanowires on Si(111) grown under different conditions. The dotted line represents the PL peak position for bulk InP.

identical to the value for bulk InP. In contrast, the PL peak shifts to shorter wavelengths for nanowires grown at 370 °C. Lower V/III ratios also result in a larger blue shift, 14 nm at 200 and 19 nm at 100. The blue shift can be caused by several effects, including quantum confinement,³² twins, and/or stacking faults,^{33,34} or wurtzite sections in the nanowires.^{35,36} As the Bohr radius in bulk InP is about 20 nm, quantum confinement is expected when the diameter of the nanowires is below this value. According to the SEM measurements, the tip and base diameters are $42 \pm 5 \text{ nm}$ and $45 \pm 5 \text{ nm}$ for $T = 360 \text{ °C}$ and V/III = 200, whereas

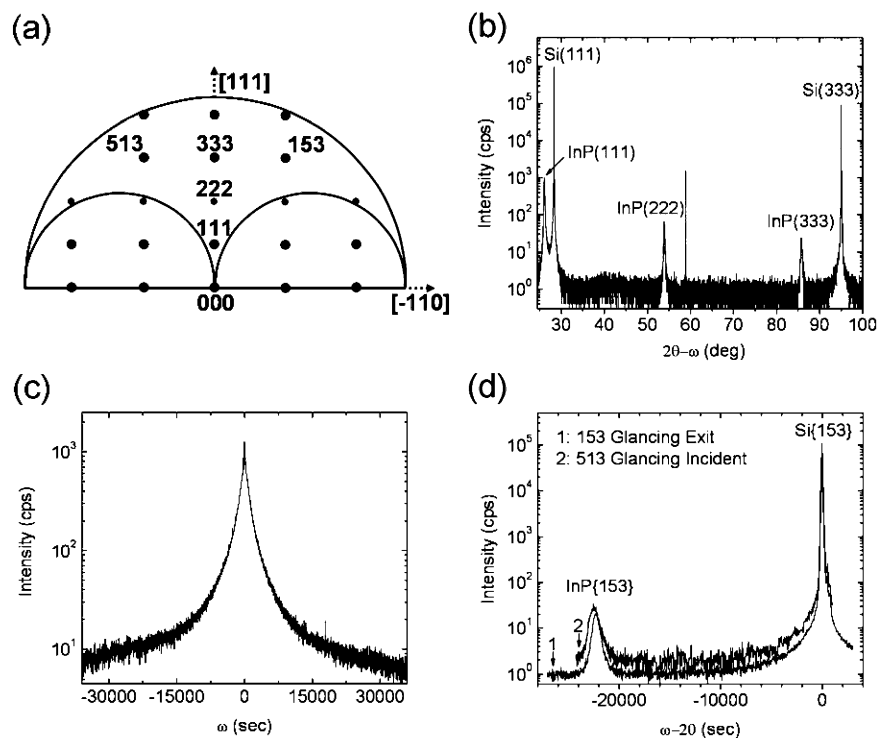


Figure 5. (a) Reciprocal space for (111) oriented zinc-blende and $[1\bar{1}2]$ zone axis. (b) An out-of-plane double-axis 2θ - ω scan. (c) Double-axis rocking curve of InP (111) nanowires. (d) Asymmetric $\{153\}$ 2θ - ω scans.

they are both 15 ± 2 nm for $T = 370$ °C and $V/III = 100$. The size effect seems to be the most likely explanation for the blue shift, since none of the wires exhibit wurtzite domains, while they all contain rotational twins.

X-ray diffraction measurements of the InP nanowires on Si(111) are shown in Figure 5. An illustration of reciprocal space for a zinc blende lattice with a (111) surface orientation and a $[1\bar{1}2]$ zone axis is shown in Figure 5a. The double-axis 2θ - ω scan shown in Figure 5b demonstrates that the only InP reflections observed are those that match the silicon substrate reflections. This confirms that the InP (111) planes are aligned along the Si (111) surface orientation. Furthermore, only zinc blende reflections are observed; there is no evidence of wurtzite InP. On the basis of other X-ray scattering measurements including triple axis measurements, there is no evidence of InP crystalline orientations other than those that indicate an epitaxial relationship between the InP and Si; we conclude that the InP wires are epitaxially deposited on the silicon substrate. The width of the InP (111) reflection (ω scan, Figure 5c) in double axis mode is $650''$, which is on the same order as reported for InP nanowires on Ge(111).²² Further X-ray scattering measurements are being conducted to better determine the origin of this peak breadth. Figure 5d includes a pair of asymmetric double-axis ω - 2θ scans of the Si and InP $\{153\}$ peaks under glancing incident (513) and glancing exit (153) geometries. The combination of the $\{153\}$ scans and the (111) ω - 2θ scan determines both the in-plane and out-of-plane lattice spacing and hence the strains along each direction. From this information, the interplanar distances are calculated for the out-of-plane (111) to be 3.394 Å and in-plane (110) to be 4.151 Å, which corresponds to a substantial 0.17% out-of-

plane strain and a smaller 0.029% in-plane strain compared to cubic InP. Increases in lattice parameter have also been reported for other nanowires³⁷ and for porous silicon,³⁸ although the present study is the first to independently determine the in-plane and out-of-plane strain values for epitaxial InP nanowires. The origin for the lattice expansion is not known; thermal expansion coefficients, slight non-stoichiometry, and the effect of adsorbed surface species may all play a role.

Figure 6a is a high resolution TEM image of two nanowires grown at 370 °C with a V/III of 200. In wire no. 1, the alternating darker and lighter grey contrast bands perpendicular to the wire axis are rotational twins separated by stacking faults. Note that we do not observe such contrast in wire no. 2. Figure 6b,c is the fast Fourier transforms (FFTs) taken of the wires within the boxes highlighted in the image. The FFT data indicate that both nanowires are zinc-blende in structure with no. 1 viewed along the $[011]$ axis, and no. 2 viewed along the $[\bar{1}12]$ axis. Since the rotational twins are aligned parallel to $[111]$, diffraction contrast due to them is absent when viewed along the $[\bar{1}12]$ zone axis. Rotational twins are often observed in III-V nanowires deposited epitaxially along the $\langle 111 \rangle$ directions.^{21,34,39,40} This is due to random stacking of the closest-packed planes during crystal growth. Finally, in Figure 6d we present a high resolution TEM image of the InP nanowire viewed along the $[\bar{1}12]$ axis. The crystal planes perpendicular to the wire axis are clearly resolved. The separation is 0.34 nm, matching the (111) lattice spacing of zinc blende indium phosphide. The nanowires grown at different conditions, included in Figures 3a and 3b, all have the $\langle 111 \rangle$ zinc blende structure with rotational twins.

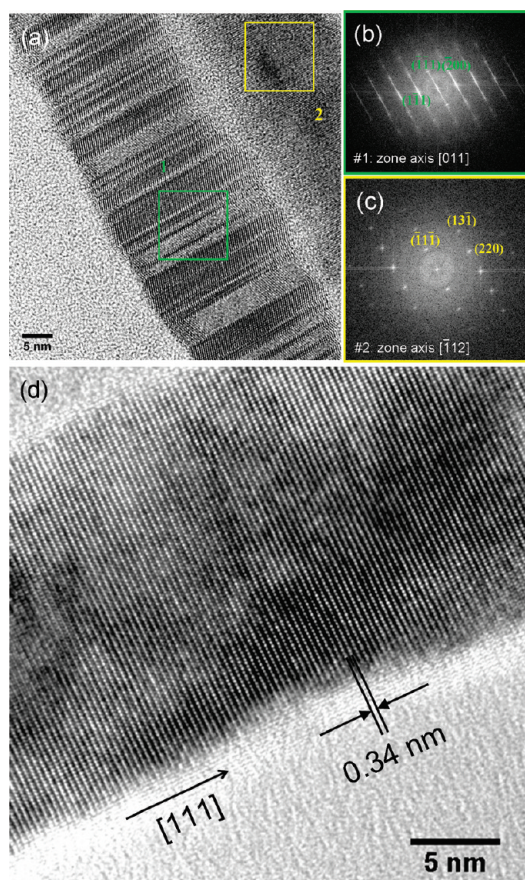


Figure 6. (a) High resolution transmission electron micrograph of two InP nanowires. (b) Fast Fourier transform of the selected area on wire no. 1, which is viewed along the $[1\bar{1}2]$ direction. (c) Fast Fourier transform of the selected area on wire no. 2, which is viewed along the $[011]$ direction. (d) High resolution transmission electron micrograph of an InP nanowire.

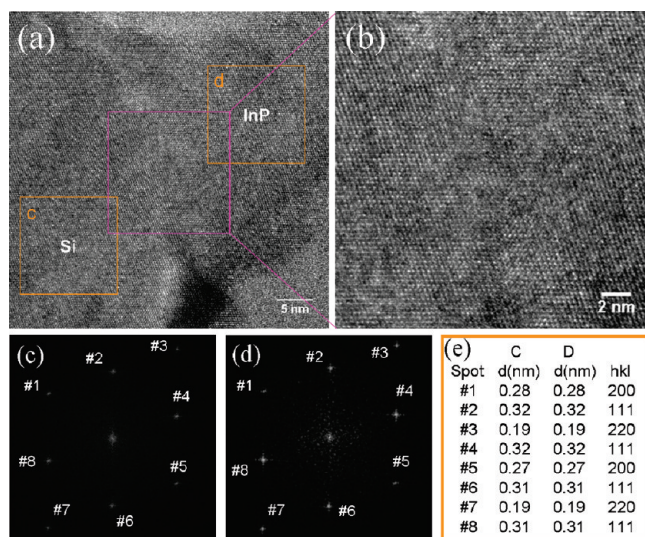


Figure 7. (a,b) High-resolution TEM images of the InP/Si interface, which are viewed along the $[011]$ direction. (c,d) Fast Fourier transforms of the selected areas on (c) the Si(111) substrate and (d) the InP nanowire. (e) Lattice constants calculated from FFT results.

Figure 7a,b is cross-sectional TEM images of the interface between the InP nanowires and the Si substrate. Evidently,

the crystal lattice progresses smoothly from the silicon substrate into the III–V semiconductor. Although the image quality is not perfect, close inspection (Figure 7b) does not uncover any dislocations at the interface. Additional images can be found in Supporting Information (Figures S2 and S3). Figure 7c,d is FFTs taken of the Si and InP, respectively. On the basis of the FFT results, in the vicinity of the InP/Si interface InP and Si have equivalent lattice constants, as shown in Figure 7e. This would suggest that the strain induced by the 8.1% lattice mismatch could be fully accommodated by elastic deformation. A similar observation has been reported by Bakkers et al.¹⁵ Nevertheless, further high resolution images are required in order to prove or disprove this hypothesis.

In summary, 100% vertical InP nanowires have been grown on Si(111) using indium droplets as the catalysts. The height-to-diameter ratio exceeds 50 with almost no tapering. Careful control over the MOVPE process temperature and V/III ratio is required in order to achieve these results.

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Supporting Information Available: This material is available free of charge via the Internet at <http://pubs.acs.org>.

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