

*Dr. Mehrnoosh Eshaghian-Wilner has developed a new computing architecture that will make nanoscale computing truly viable*

### **Interview with Mary Mehrnoosh Eshaghian-Wilner**

Questions by Sander Olson. Answers by Mary Mehrnoosh Eshaghian-Wilner

Dr. Mehrnoosh Eshaghian-Wilner is an electrical engineering professor at UCLA, with a background in Very Large Scale Integration (VLSI) chip design. She leads the Bio-Inspired and Nanoscale integrated Computing (BioNIC) research group, which is focused on biologically inspired nanocomputing architectures. Her team recently announced a major advance in computing architectures involving "spin-wave buses". This advance has myriad potential applications, and should result in wearable and even implantable nanocomputing devices.

**<Question>: Tell us about yourself. What is your background, and what is your current position?**

<Answer>: I am an electrical engineering adjunct professor at UCLA. My background is in the area of computer architecture and Very Large Scale Integration (VLSI) chip design. I have been doing research in that area for about twenty years. My expertise is in parallel processing, and I have spent much of my career examining different platforms for various applications. So, I have a broad background in parallel and distributed computing architectures and algorithms.

**<Question>: Describe the Bio-inspired and Nano-scale Integrated Computing research at UCLA.**

<Answer>: I lead the BioNIC research group at UCLA which is focused on biologically inspired computing architectures. This should have applications in biomedical fields. For example, our recent breakthrough in spin-wave buses could have many applications for implantable medical devices. We are also examining bioinformatics applications, such as rapid DNA sequence mapping.

**<Question>: The Semiconductor research corporation is funding the construction of a Functional Engineered Nano Architectonics Focus Center (FENA) at UCLA. What are the goals and objectives of this Center?**

<Answer>: I am not directly involved in FENA, the director is Dr. Kang Wang. One of the emphases of FENA is to design post-Complementary Metal Oxide Semiconductor (CMOS) nano architectures. FENA is funded by both the semiconductor research corporation and the Department of Defense. California Nano Systems Institute (CNSI) is another research unit at UCLA campus that focuses on nano architectures. I collaborate with members of both CNSI and FENA.

**<Question>: Your team at UCLA just made a breakthrough involving "spin-wave buses" nanoarchitectures. What is the significance of this breakthrough?**

<Answer>: In order to describe the significance of this advance I first need to mention a few aspects of VLSI architectures. VLSI technology now allows chip designers to design a network of processors on a single chip. That is important, because current VLSI technology uses copper wires as interconnects, and there are several issues with that technology. One problem is the tremendous amount of area required to connect numerous processing nodes to one another. There are also other technical issues that make this technology impractical for interconnecting large number of processors on a single chip. When I did my thesis I wondered if there was a way to have a fully connected computing network without wires. I first examined the possibility of optical interconnects, but found that there were myriad technical difficulties with that approach as well. I recently through my collaboration with Dr. Alex Khitun and Dr. Kang Wang found that “spin-wave” technology could offer a real solution. Spin-wave technology has a number of advantages as an interconnect – it is actually possible to build a fully interconnected network of processors on a single chip. The processor nodes communicate through spin-waves, and don’t require any physical wires. Although spin waves are relatively slower than optical waves, it has a potential for terahertz switching. At the moment, we are already able to achieve gigahertz switching, which makes it compatible with the current state of chip technology. From a computing point of view, this new spin-wave model effectively solves the intractable problems that plague other interconnect approaches. This nanoscale architecture increases computational speeds, is power-efficient, reduces the space requirements for interconnects, and allows for fundamentally new computing paradigms. The potential applications of this technology are enormous, since this is a nanoscale architecture that can work at room temperature. This method of computing could almost be considered biologically inspired, and has a number of potential applications. Biomedical imaging is just one of many applications that this technology could substantially improve. This architecture will make nanoscale computing viable.

**<Question>: How integratable is this technology with standard CMOS? Could a microprocessor be manufactured with spin wave buses?**

<Answer>: A microprocessor employing spin-wave buses could be designed and built. You could do this by integrating nanoscale modules within a multiprocessor chip. This could result in a powerful hierarchical architecture. Such a chip should be manufacturable, since my collaborator, Dr. Khitun has already built a basic semi-prototype on silicon substrate here at UCLA which does notably operate in room temperature.

**<Question>: Do you see nanoscale computing devices supplanting conventional CMOS?**

<Answer>: I see nanoscale computing devices being integrated into conventional CMOS integrated circuits. This technology, at least at the beginning, should complement and enhance, rather than replace, existing silicon technology. It is possible to design a system that uses only nanoscale components and spin-wave buses, but that would require redesigning the entire system to take advantage of these nanoscale phenomena.

**<Question>: Have you done any research into using spin-wave technology for logic applications?**

<Answer>: We have done research into this area, and we are continuing to examine this field. My collaborator, Dr. Alex Khitun has simulated logic functions such as AND, NOT as well as OR gates using spin-wave technology. So this technology could potentially be used for computer logic as well as for interconnect technology.

**<Question>: When do you see the first commercial applications emerging from this research?**

<Answer>: It is possible that we could see the first commercial applications emerging within the next several years. With sufficient funding, spin-wave technology could begin to transform fields very soon.

**<Question>: What outside organizations besides the SIA are funding your research?**

<Answer>: At the moment, we are not being funded by any outside organizations for this particular project involving the three architectures. We have submitted a proposal to the National Science Foundation (NSF) and we are waiting to hear from them. So we are seeking outside sources of funding.

**<Question>: Are there any startup corporations that have been founded to commercialize this research?**

<Answer>: Right now, the UCLA intellectual property office is just beginning to send out announcements regarding commercialization of this technology. This push to commercialization began as soon as we published. These three nanoarchitectures have been provisionally patented, and are available for licensing through UCLA. But this process has just begun. I don't believe that it will be long before it is licensed by some major corporations, and or before the first startup companies emerge to take advantage of this technology.

**<Question>: How do you see this technology evolving during the next decade?**

<Answer>: I predict that within a decade, huge applications for spin-wave technologies will emerge. This technology has a plethora of potential applications. This nanotechnology should result in wearable and even implantable computing devices. Computing could even be sprayed on surfaces. I don't know if we will see desktop PCs from this technology, but spin-wave technology could be used in a plethora of embedded applications. One of my goals is to eventually see these nanocomputing devices embedded in humans.