Motivation:

- EE213A: link between digital signal processing and ASIC implementation
- is a vertical refinement

  - Specification: MATLAB, SPW, Cossap
  - Floating point
  - Fixed point
  - Algorithm transformations
  - Architecture mapping:
    - Bit parallel - bit serial
  - Link to floorplanning, power optimization, etc.
Motivation:

- EE298-2: exploration of implementation platforms
- is a horizontal exploration

<table>
<thead>
<tr>
<th>ASIC</th>
<th>Application Specific</th>
<th>Domain Specific</th>
<th>General DSP</th>
<th>General Purpose</th>
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Performance / Power:

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<th>high</th>
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<th>low</th>
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Programmability:

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<tr>
<th></th>
<th>none</th>
<th>parameters</th>
<th></th>
<th>very high</th>
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Motivation:

- This class: one application over different implementation platforms
- horizontal and vertical exploration

- Specification: MATLAB, SPW, Cossap, C/C++
- Floating point
- Fixed point
- Algorithm transformations

Architecture alternatives:

- ASIC
  - Bit parallel
  - Bit serial
  - Special Purpose (DSP Canvas, Art Designer)
- Retargetable coprocessor (Target compiler technologies, Easics)
- DSP processors (TI TMS320C54x)
- DSP extensions to RISC (Tensilica)
Motivation:

- Back-end: Verilog/VHDL, synthesis, place & route

- ASIC
  - Bit parallel
  - Bit serial (DSP Canvas)

- Special Purpose
  - (Art Designer)

- Retargetable coprocessor
  - (Target compiler technologies, Easics)

- DSP processors
  - (TI TMS320C54x)

- RISC with DSP extensions
  - (Tensilica)

- Hardware
  - Synopsys synthesis
  - Cadence Place & Route

- Software
  - C-compilation
  - Assembly optimization

System-on-a-chip

Embedded systems = “systems-on-a-chip.”
Applications:

- This class (spring 2000): FIR filter over these implementation platforms
- (next class: Viterbi algorithm or network processor)

\[
\begin{align*}
\text{FIR design in Matlab} \\
\text{C, C++ conversion, gradual refinement} \\
\text{Optimizations:} \\
\quad & \text{algorithm transformations} \\
\quad & \text{fixed point optimization} \\
\quad & \text{coefficient optimization} \\
\text{Architecture design and optimization} \\
\quad & \text{(several alternatives)} \\
\text{Comparison based on:} \\
\quad & \text{throughput} \\
\quad & \text{area} \\
\quad & \text{power} \\
\quad & \text{design time} \\
\quad & \text{design reuse (flexibility)}
\end{align*}
\]

Throughput driven computations

- Real-time systems: sample rate, frame rate, symbol rate, etc.
  \textit{Worst case} operation determined by \textit{external} events

- Different from “average” running time
  \(=\) measure on programmable processors
  E.g. average time to display powerpoint file

\[
\begin{align*}
\text{Sample frequency} \quad \frac{\text{Clock frequency}}{=\text{number of clock cycles available for the job}}
\end{align*}
\]