Digital Signal Processors for Mobile Phone Terminals

Katsuhiko Ueda

Matsushita Electric Ind. Co., Ltd.
Abstract

- A DSP is one of the key components in a digital cellular phone terminal.
- This talk will discuss the role of the DSP in the terminal and how to achieve high performance with low power consumption.
- Mobile phone system is moving rapidly into mobile multimedia era. A DSP architecture suitable for this new era will be also discussed.
1. The role of DSP in cellular phone terminal.

2. How to achieve high performance with low power consumption.

3. Issues for DSP in next generation mobile phone systems.

4. Mobile multimedia DSP.

5. Summary.
Role of DSP
- Speech CODEC
- Channel CODEC
- Equalizer
- Mod/Demodulator
K. Ueda, '99 VLSI Circuits Short Course

1 TDMA Frame (40ms)

125us (8KHz) -> 2,560bits/40ms -> 64kbps (8bits * 8KHz)
Speech: 138bits/40ms -> 3.45kbps
FEC: 86bits/40ms -> 2.15kbps
Total: 5.6kbps

User 6 User 1 User 2 User 3 User 4 User 5 User 6 User 1
42kbps

1 slot (~6.7ms, 7kbps)

K. Ueda, '99 VLSI Circuits Short Course
Speech CODEC

Digitized Input Speech Signal -> Spectrum Analysis

Gain

Code Book -> Synthesis Filter

Minimizing the difference between input speech signal and synthesized speech signal

Parameter

<table>
<thead>
<tr>
<th>Bit rate [kbps]</th>
<th>PSI-CELP</th>
<th>13kbps VSELP</th>
<th>11.2kbps VSELP</th>
<th>RPE-LTP</th>
</tr>
</thead>
<tbody>
<tr>
<td>MOPS</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>[MOPS]</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

K. Ueda, '99 VLSI Circuits Short Course
K. Ueda, '99 VLSI Circuits Short Course

Dedicated DSP for Portable Phone

- Increase Performance by adding accelerators
- Reduce Power consumption

\[ P_c \propto f^2 c v^2 \]

- Frequency, c: capacitance, v: voltage

K. Ueda, '99 VLSI Circuits Short Course
A DSP Architecture for Portable Phone Terminal

Special memory scheme to realize double speed MAC

Dedicated MAC unit
Double speed MAC scheme
Redundant binary number system

K. Ueda, '99 VLSI Circuits Short Course
Double Speed MAC Scheme

Output of MX

- 1 cycle

<table>
<thead>
<tr>
<th>D(2x)</th>
<th>D(2x+2)</th>
<th>D(2x+3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D(2x+1)</td>
<td>D(2x+3)</td>
<td>D(2x+5)</td>
</tr>
</tbody>
</table>

TEMP REG

<table>
<thead>
<tr>
<th>D(2x)</th>
<th>D(2x+2)</th>
<th>D(2x+3)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D(2x+1)</td>
<td>D(2x+3)</td>
<td>D(2x+5)</td>
</tr>
</tbody>
</table>

A-BUS

<table>
<thead>
<tr>
<th>D(2x)</th>
<th>D(2x+1)</th>
<th>D(2x+2)</th>
<th>D(2x+3)</th>
<th>D(2x+4)</th>
<th>D(2x+5)</th>
</tr>
</thead>
</table>

B-BUS

<table>
<thead>
<tr>
<th>D(2y)</th>
<th>D(2y+1)</th>
<th>D(2y+2)</th>
<th>D(2y+3)</th>
<th>D(2y+4)</th>
<th>D(2y+5)</th>
</tr>
</thead>
</table>

MULTIPLIER

<table>
<thead>
<tr>
<th>D(2x)</th>
<th>D(2x+1)</th>
<th>D(2x+2)</th>
<th>D(2x+3)</th>
<th>D(2x+4)</th>
<th>D(2x+5)</th>
</tr>
</thead>
<tbody>
<tr>
<td>D(2y)</td>
<td>D(2y+1)</td>
<td>D(2y+2)</td>
<td>D(2y+3)</td>
<td>D(2y+4)</td>
<td>D(2y+5)</td>
</tr>
</tbody>
</table>

MAC UNIT

BARREL SHIFTER

ADDER

PIPELINE REG

MULTIPLIER

K. Ueda, '99 VLSI Circuits Short Course
Accelerator for Viterbi Decoding

PM0(t-1) → PM0(t)
PM1(t-1) → PM0(t)

PM0(t) = \min[(PM0(t-1) + BMa(t)), (PM1(t-1) + BMb(t))]

Two Adds, one Compare and one Select -> ACS operation

- Normal operation: The ALU is used as a 16-bit processing unit.
- ACS operation: The ALU is used as two 8-bit adders.

K. Ueda, '99 VLSI Circuits Short Course
Comparison of the number of clock cycles needed to realize an 11.2kbps VSELP CODEC.

Effect of Accelerators

- **DSP w/o MAC & Viterbi Accelerators**
  - Misc: - 11.4%
  - Block Floating Error Correction: - 9.0%
  - MAC: - 8%
  - ALU: - 4.7%
  - Total: - 33.1%

- **DSP w/ MAC & Viterbi Accelerators**
FIR Filtering: tow outputs in parallel with delay register

\[
\begin{align*}
y(0) &= c(0)x(0) + c(1)x(-1) + c(2)x(-2) + c(3)x(-3) + \\
y(1) &= c(0)x(1) + c(1)x(0) + c(2)x(-1) + c(3)x(-2) + \\
y(2) &= c(0)x(2) + c(1)x(1) + c(2)x(0) + c(3)x(-1) + \\
y(3) &= c(0)x(3) + c(1)x(2) + c(2)x(1) + c(3)x(0)
\end{align*}
\]

<table>
<thead>
<tr>
<th></th>
<th>Single MAC</th>
<th>Dual MAC</th>
<th>Dual MAC with REG</th>
</tr>
</thead>
<tbody>
<tr>
<td># of MAC operations</td>
<td>N</td>
<td>N</td>
<td>N</td>
</tr>
<tr>
<td># of Memory reads</td>
<td>2N</td>
<td>2N</td>
<td>N</td>
</tr>
</tbody>
</table>

Low power consumption

K. Ueda, '99 VLSI Circuits Short Course
MAC Unit using Redundant Binary Number

RBMU : Redundant Binary Multiply Unit
RBAU : Redundant Binary Accumulation Unit
RTBC : Redundant Binary Digit to Binary Digit Conversion Unit

RB->B CNV 0.5 cycle
ACC 0.5 cycle
MUL 0.5 cycle

Power Consumption Ratio normalized to a BW-MAC

K. Ueda, '99 VLSI Circuits Short Course
A System LSI realizing Base Band Processing & Control

Features of the LSI

<table>
<thead>
<tr>
<th>Feature</th>
<th>Details</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Tech.</td>
<td>0.35 um CMOS</td>
</tr>
<tr>
<td># of Transistors</td>
<td>2.5 Million</td>
</tr>
<tr>
<td>Die Size</td>
<td>9.26x10.0mm</td>
</tr>
<tr>
<td>Package</td>
<td>11x11mm CSP</td>
</tr>
<tr>
<td>Integrated IP</td>
<td>16b MCU MN102L (3MIPS)</td>
</tr>
<tr>
<td></td>
<td>16b DSP MN1930 (40MIPS)</td>
</tr>
<tr>
<td></td>
<td>Demodulator, TDMA Controller, VCO, etc.</td>
</tr>
</tbody>
</table>

K. Ueda, '99 VLSI Circuits Short Course
Goal of the next generation Mobile Phone System

Current System
(PDC)

5.6 / 11.2 kbps

Next Generation
System
(W-CDMA)

8 kbps ~ 2 Mbps

System Requirements

High Bit Rate Data Transfer
- MORE cycles for error correction
- MORE data input/output to/from DSP

Video CODEC Capability

Of course, LOW POWER

K. Ueda, '99 VLSI Circuits Short Course
Increasing Capability of Access Systems

FDMA (Frequency Division Multiple Access)

CDMA (Code Division Multiple Access)

TDMA (Time Division Multiple Access)

Increase
- Channel Capacity
- Data Speed

-> System Complexity (DSP Performance)

Digital System
ex. IS-95, W-CDMA

Digital System
ex. PDC, GSM, IS-54, PHS

Analog System

K. Ueda, '99 VLSI Circuits Short Course
Next Generation Mobile Phone Terminal and Issues to LSIs

- Receiver
- Transmitter
- Duplexer (DUP)
- RF unit
- A/D
- De-spread
- Rake
- Base band Signal Processing unit
- Spread
- Channel CODEC
- Speech/Video CODEC
- Control unit
- Low-power Video/Audio CODEC LSI
- High speed LSI
- Low-power A/D
- Low-power & High speed correlator
- High speed Viterbi/Turbo decoder

K. Ueda, '99 VLSI Circuits Short Course
DSP Architecture for the Next Generation System

- RF
- ADC, DAC
- Spreading/Despreading

Wide bandwidth to/from DSP

High Performance Processing Unit for Viterbi Decoding

CKU: Clock control Unit
DPP: Direct Parallel Port
DPU: Data Processing Unit
ICU: Interrupt Control Unit
IOU: data I/O Unit
PCU: Program flow Control Unit
PU: Pointer Unit

K. Ueda, '99 VLSI Circuits Short Course
Dual ACS Operation

2 path metrics are updated in 1 cycle

K. Ueda, '99 VLSI Circuits Short Course
DSP for Wireless Video Phone

Features

<table>
<thead>
<tr>
<th>Feature</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Clock frequency</td>
<td>67.5MHz(14.8nsec)</td>
</tr>
<tr>
<td>Technology</td>
<td>0.25um-CMOS(4-Metal)</td>
</tr>
<tr>
<td>Number of devices</td>
<td>7,670KTr.</td>
</tr>
<tr>
<td>Die size</td>
<td>9.41 x 9.22(=86.76)mm^2</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>1.8V(Internal), 3.3V(IO)</td>
</tr>
<tr>
<td>Performance</td>
<td>4GOPS 15frames/sec(CIF CODEC)</td>
</tr>
</tbody>
</table>

K. Ueda, '99 VLSI Circuits Short Course
1. DSP is one of key components in portable phone terminal and high performance with low power consumption is essential factor.

2. In the mobile multimedia era, new DSPs with higher performance and increased functionality will be necessary.

3. DSP for portable phone must keep on achieving MORE MIPS and LESS power consumption.
[References]


Mobile Phone for Internet & Data Communication

Ex. i Mode system provided by NTT DoCoMo

Applications
- E-mail
- Web Browsing
- Banking
- Locating combining car navigation system
  etc.

Panasonic P502i