Towards High Speed and
Bandwidth Efficient CMOS Wireless Transceivers

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ABSTRACT
We describe an approach to constructing an all-CMOS wireless transceiver capable of
transmission speeds of up to 30 Mb/s in the 2.4 GHz ISM band. To achieve robust high
bandwidth efficiency communications, the design includes such features as a four element
antenna array, adaptive equalization, multi-level QAM transmission, variable baud rates,
frequency hopping, and adjustable transmission power. We further describe how these adaptive
features can be exploited in high efficiency multiple access schemes.
I. Introduction
The variability of wireless channels presents both challenges and opportunities in designing multiple access communications systems. To maximize throughput for a given power budget, the link must adapt to the actual channel conditions, changing the transmitter power level, antenna beam pattern, equalizer settings, and possibly the symbol rate and constellation size. On the other hand, the attenuation and directionality of signals makes possible re-use of the time/frequency resources in space, permitting a large number of users to access the shared medium. In this paper we describe a high speed radio transceiver with the wide range of adaptive features needed to support such high spectral efficiency access techniques, as well as a suite of adaptive methods which could be supported on the radio platform. We consider the particular application of an indoor LAN, where laptop computers require highspeed wireless access, for either pico cellular or peer-to-peer networks. In such applications, we require not only high bandwidth efficiency but also low cost and compact implementations. There are challenges in many technology areas in producing such a system, among them:

• development of adaptive algorithms to manage in a distributed fashion both links and multiple access for high spectral efficiency
• testing of algorithms in representative environments on hardware platforms
• development of low power, highly integrated digital baseband circuits for management of the adaptive functions
• development of low power and low-cost integrated analog front ends with high linearity and suppression of out of band interference
• creation of antenna systems which take into account constraints of the platform and the requirements for low cost manufacturability.

Substantial progress has been made towards the demonstration of a highly spectrally efficient all-CMOS transceiver operating in the 2.4 GHz ISM band. To exploit the many possibilities for interference avoidance and averaging in an environment notorious for its unmanaged interference, the transceiver will support frequency hopped M-ary QAM, with the capability of variable bit and power assignment on individual hops. The digital and analog circuits under development support transmit and receive antenna arrays, and the receiver includes an adaptive decision feedback equalizer (DFE). Novel antenna elements have been developed, and new but
simple distributed algorithms have been devised to manage the interactions between so many adaptive components. A prototype QAM radio supports transmission at up to 30 Mb/s; future versions will include the highly integrated digital and analog circuits that have been developed. Throughout, the emphasis has been on pushing the envelope in each domain while living within the practical constraints of other components of the system.

Given the very broad set of systems and technology issues involved in such a design, we will not be able to provide complete detail on each subsystem. Rather, in the remainder of the paper we will present the major results of the research and its present status, in a “top = down” fashion moving from systems issues to components. In section II we describe how the adaptive features of the radio can be exploited in a multiple access setting, presenting a suite of interconnected adaptive algorithms that mitigate interference. In section III we describe measurement results for a prototype radio. In section IV, V, and VI we describe our research in how to reduce the size and power consumption to a form suitable for laptop computers, presenting designs for the digital, analog, and antenna systems respectively. In section VII, we present our conclusions.

II. Adaptive Algorithms for Bandwidth Efficient Multiple Access

A fundamental limit on the capacity of a multiple access wireless system is imposed by the inability of the various users to perfectly estimate and predict the time-varying channel and interference. In the limit of large complexity and power levels, all other impairments can in principle be overcome if the channel dynamics (including interference) are slow enough. In this section, we describe practical techniques for ameliorating the impairments, through channel probing, dynamic power and bit allocation, and adaptive antenna arrays and equalizers. Our research has focussed on distributed rather than centralized algorithms for management of multiple access. Such algorithms are desirable, in that they require minimal revision of existing network software and can apply to both cellular and peer-to-peer network topologies, with greatly reduced complexity as compared to centralized solutions.

In support of the algorithmic development reported here, considerable simulation effort has been involved. For the work that includes antenna arrays, the correlated multipath channel was constructed using ray-tracing techniques, which included up to quadruple bounces in a large room [1]. Otherwise, statistical models assuming Rayleigh fading and log-normal shadowing with fourth power distance loss were used. The specific models are relatively unimportant to the
conclusions, as we were mainly interested in devising algorithms that would be robust with respect to channel variability while living within the hardware constraints. They can be fine-tuned for any particular application scenario, following testing on hardware.

II.1. Dynamic Channel, Power, and Bit Allocation

Dynamic channel assignment (DCA) algorithms are interference avoidance strategies which slot users to keep the SIR above a desired value, changing assignments as needed. Systems employing DCA are interference-limited; thus techniques that reduce the Eb/No required for reliable operation directly improve the overall capacity. Distributed forms of DCA [e.g. 2,3] achieve performance similar to centralized omniscient algorithms, with only imperfect local measurements of the channel conditions, and no cooperation among base stations. This comes at the expense of additional convergence time, and relies upon the local nature of the interference coupling among users.

Capacity can be further improved using distributed dynamic power and channel assignment (DPCA) algorithms [4-8]. The only information transfer required is for the communication partners to exchange their measurements of the interference power and the propagation loss for their link. If the SIR is below the target, the receiver signals the transmitter to increase the power by a small fixed amount in dB; if above the target, it signals for a decrease. This amounts to a gradient search on SIR, and has a geometric convergence rate. In addition to the interference avoidance properties of DCA, power control reduces the total amount of interference generated since only as much power is transmitted as is needed to maintain a reliable link. Therefore a further network capacity benefit accrues. In practice, there are dynamic power range limitations on the radio. These can be accommodated through voluntary termination of channel admission attempts when the resistance of other users is apparent from rapidly increasing interference levels [9,10].

Channel probing is one means to speed up distributed forms of DPCA. For noise-limited dispersive channels, probing consists of learning the noise level and the channel impulse response. From these measurements, the best achievable SNR can be computed, and the appropriate combination of symbol rate, power level, and constellation size can be chosen. However, in interference-coupled systems, an increase in the power level of a new user will
cause a reaction of increased power by the other users sharing the channel. Probing therefore aims to predict the SIR that the power control algorithm will converge to.

We have established that a very small number of measurements suffice to predict the final power level. Having measured the propagation gain on the desired link, a few power control steps establish the starting interference level and the change in interference as a result of increasing the power [10]. To probe the channel, let $q_i(0)$ be the measured received interference value before transmission begins. Let $q_i(1)$ be the measured interference value and $s_i(1)$ the measured received signal power value after a fixed power level has been transmitted, and the other users have adjusted their power in response. Then the maximum feasible SIR is estimated as

$$\hat{\lambda}_{\text{max}} = \frac{s_i(1)}{q_i - q_i(0)}$$

(1)

As there will be measurement errors, several iterations are needed in practice to form reasonable estimates of the final SIR, but probing is orders of magnitude faster than going through the complete adaptation.

In a frequency-hopped system, there are additional degrees of freedom beyond choosing power levels and channel assignments. If hopping patterns are aligned across cells and we assign the same power to every slot, then the DPCA problem is the same as for a simple TDMA system, except that hopping affords the possibility of coding over slots to provide diversity protection. We may alternatively randomize the hopping patterns over cells [11], in which case coding also provides some diversity protection with respect to the varying interference levels. Since in this case the choice of channel is less critical, time spent probing can be reduced. The former approach leads to a greater possibility of interference avoidance, but is less robust in with respect to channel and traffic dynamics than the latter.

Furthermore, it is not necessary to transmit the same number of bits in every hop, or indeed to use every hop. Suppose hopping patterns have been randomized among cells, and the digital constellation size is fixed, but we can choose in which $M$ out of $N$ slots in a hopping pattern to transmit bits. Coding is performed across the hops so that we are most concerned with the
average power, although with a fixed constellation size minimum SIR requirements remain unless large redundancy is contemplated. Then the allocation of slots can be accomplished by using channel probing and choosing the M slots leading to the lowest power consumption. This choice causes users to arrange themselves for near-minimum mutual interference; i.e. it promotes interference avoidance [12]. Lower M permits more interference avoidance, but increases the bandwidth requirements for each user. The optimal ratio of M/N can be determined by simulations.

Larger capacity is obtained if we can allocate a variable number of bits to the slots. The optimal allocation of bits and power when dealing with signal-independent impairments is the well-known waterfilling distribution with respect to the noise floor. However, in multiple access systems the variable power allocation also changes the interference. We have found that the most successful heuristics are those which aim to achieve maximum interference avoidance, rather than a minimization of average transmitted power. That is, users tend to occupy as small a number of slots as possible consistent with the maximum constellation size permitted, with some smaller number using medium size constellations, and many with no bit allocation at all [13]. Two algorithms which give good performance are reverse waterfilling based on maximum estimated SIR, and minimization of the total number of slots in the hopping pattern that are occupied, subject to having an acceptable SIR. In both cases, similar error rates are found in all hops for which bits are allocated, through the joint adjustment of constellation size and power level, resulting in a 50% capacity increase compared to DPCA alone, assuming a maximum constellation size of 64 QAM (limited by the analog front end linearity). Here accurate channel probing is essential, although channel coding over slots can permit reliable communications even if there remains some variability in uncoded error rates due to small errors in the SIR prediction.

II.2. Interaction of Adaptive Antenna Arrays, Equalizers, and Power Control

We now consider how the antenna arrays, equalizers, and adjustable transmit power levels are coupled, and how to beneficially adapt the ensemble. Adjustment of either the power or the transmit beam pattern changes the interference seen by everyone else, and also modifies the impulse response seen by the intended receiver through selective weighting of multipath components. Adjustment of the receiver beam pattern changes the interference levels and the impulse response, and thus the power level required for reliable operation and the residual
channel seen by the equalizer. Therefore, the algorithms are coupled at two levels: internally, with respect to the desired link, and externally, via the interference coupling to other users. This renders analysis difficult, and we have largely resorted to simulations.

Closed form solutions can be derived for the optimal weights of the receiver array given any particular transmitter pattern, but the joint optimization is already difficult for our situation of adaptive transmitter and receiver arrays. The problem is even more difficult when the interferers also have adaptive arrays, since for strongly coupled links (large gains) an action by one produces a large reaction in the others. Our approach [1,14] was to adapt the receiver using the LMS algorithm, with receiver weights re-used for transmission. The heuristic behind this choice is that in a time division duplex system the nulls placed in the direction of interferers during reception will also reduce interference transmitted towards the other users who caused most of the interference. Thus, receiver adaptation will also serve to reduce the interference generated. Additionally, gain in the direction of the communications partner is preserved, so that SIR is improved for the link. These two effects also serve to decouple interactions, promoting more rapid convergence. More complicated choices for the adaptive algorithm with potentially faster convergence are in fact possible [15], but the requirements for implementation at high symbol rates made variants on the LMS algorithm the only practical option.

Fortunately, in our simulations where users in the same cell were prohibited from using the same channel, convergence was always obtained with this "ping-pong" adaptation of the arrays of the communicating partners. This channel access restriction insures that the desired link rather than any one interferer dominates the adaptation dynamics. When this restriction is released, there were many occasions in which adaptation failed. This is unsurprising, since there is no prior expectation that the error surface should be quadratic. Further simulations using the same scenario as in [1,14] revealed that one can also ensure stability by using an approach similar to that used in distributed power control algorithms, namely, voluntary drop-out when little progress is being made in SIR levels. This mechanism also decouples the system, leading to stable convergence by the remaining users. The result for the peer-to-peer system simulated was only a 10% reduction in capacity relative to the explicit frequency re-use restrictions, which might be an acceptable price for a fully distributed solution. The cost (or benefit!) will of course
in practice depend on the particular network topology, number of antennas, and channel dynamics.

Adding equalizers to the system greatly expands the number of configurations possible. In multichannel combiners (MC) there are linear equalizers for each antenna branch, and then after combining, either MLSE or a DFE. Alternatively, all equalization can follow adaptive antenna combining. The MC deals with the distinct impulse responses seen in each antenna branch, and (in slowly changing channels) has better performance than structures where the equalizer follows simple combining. However, the hardware complexity is much higher and it is difficult to produce appropriate beam patterns for the transmitter array. For the indoor environment simulated in [14], there was little performance loss from using a simple combiner followed by equalization, so that the receiver antenna weights could be re-used for transmission. At the same time, the simple use of adaptive transmitters so enabled lead to a large link gain improvement compared to omnidirectional transmission and an MC receiver.

Power control produces further interactions. A change in the beam pattern even with constant radiated power affects the power measured at all receivers. An interesting result is that if the antenna weights are renormalized to maintain constant gain in the direction of the desired users, then including small power control steps actually improves convergence of the distributed beamforming algorithm [1]. The intuition is that power control directly determines the minimum gain required for the desired link, quickly reducing unnecessary interference, and thus the coupling in adaptation among cells. This combination of methods results in both improved capacity and reduced average transmitted power compared to either technique alone.

Probing to estimate the maximum SIR is made much more difficult by the presence of adaptive transmitter and receiver antenna arrays. When probing at low power levels, receivers can easily slightly shift their beam patterns to almost completely remove the effect of the new interference. Later, at some higher power level, shifting the beam pattern is insufficient and the transmitted power levels increase. Nevertheless, a simple model, which assumes that most interference is due to one interference path, predicts the final SIR with remarkable accuracy [16]. Thus, variable bit allocation may also be combined with power control and adaptive antenna arrays.
II.3. Summary

In this section we have presented a suite of distributed iterative algorithms which promise orders of magnitude capacity improvement compared to fixed solutions, with modest implementation complexity. These techniques exploit variations in the radio channel with angle, frequency, and location. Our research indicates that distributed algorithms based on gradient descent techniques suffice to produce stable and rapid convergence in many circumstances. This success is fortunate in that hardware realizations are possible even at high symbol rates, but somewhat surprising given the complicated interference interactions. The explanation is however fairly straightforward in retrospect. Gradient search techniques are known to work extremely well for individual links for which there is no interference coupling. The LMS algorithm in particular is robust against small nonlinearities and modeling errors. However, for universal success explicit re-use restrictions, interference averaging, or dynamic methods (e.g. probing and adaptive dropout provisions) must exclude users that produce strong interference coupling. The proper mix among these methods will depend on the application scenario.

III. First Generation Testbed

While simulations are constantly increasing in sophistication, completely accurate modeling of transceivers in wireless environments is still a difficult, if not impossible, task. In order to investigate the actual performance of these systems and the effects of advanced algorithms, a series of versatile wireless QAM testbeds are being developed. The first-generation testbed depicted in Figure 1 is based on a 5 MBaud QAM transmitter-receiver pair, and it allows researchers to use data rates of 10, 20, and 30 megabits-per-second (Mbps) with a decision-feedback equalizer of up to 16 coefficients [17].

The transmitter section of the testbed starts with a serial bitstream produced by a bit-error-rate tester (BERT) transmitter, which provides pseudo-random data for the baseband QAM modulator. The modulator can produce 4-, 16-, or 64-QAM constellations at 5 MBaud, and its output is an analog bandpass signal at an intermediate frequency (IF) of 43.75 MHz. This is followed by a linear upconverter, which amplifies and converts the signal up to a carrier frequency of 2.44 GHz at a power level of 10 mW (+10 dBm). For the tests discussed here, the
antennas used are “sleeve monopoles” with near-uniform gain in the azimuth plane, approximating an omnidirectional antenna.

After the receive antenna, the first stage is the downconverter, which bandpass filters, linearly amplifies, and shifts the received signal back to the IF at 43.75 MHz. It also allows manual control of the downconverter gain over a 48-dB range. This IF signal is sent to the QAM receiver, which first converts the signal to baseband and digitizes it. The receiver digitally demodulates the signal with matched filtering, then performs real-time adaptive decision-feedback equalization with a 16-tap, T-spaced (eight feedforward and eight feedback taps) equalizer using the least-mean squares (LMS) algorithm. It also provides timing and carrier recovery as well as automatic-gain control, finally resulting in an output bitstream that is sent to a BERT receiver. The demodulator has a personal computer (PC) interface that allows users to monitor the operation and control the functions of the digital baseband receiver, allowing display of variables including the slicer SNR and equalizer tap values.

To explore the feasibility of wideband wireless QAM transmission in the indoor office or laboratory environment, extensive measurements were made at two different locations: the Crawford Hill building of Bell Laboratories [18] and the Wireless Systems Research Laboratory at UCLA, depicted in Figure 2. The Crawford Hill experiments involved 2664 data points, using the receiver at a fixed location in room R202. In rooms R206, R219, and R225, the transmitter antenna was placed in a total of 576 locations by placing a cart in 63 locations and moving the antenna through a three-by-three grid of points separated by a single wavelength (l ~ 12 cm) at each cart location. The UCLA trials resulted in 3600 data points, obtained by using a fixed transmitter (at location TX1 or TX2 in Figure 2) in Room 1 and a receiver at a location within Room 1, Room 2, or the adjacent hallway. An array of seven antenna positions separated by l was used for these tests. In both sets of tests, the data rates were varied between 10, 20, and 30 Mbps (corresponding to constellation sizes of 4-, 16-, and 64-QAM), and the receiver was operated with both full adaptive equalization (all 16 taps) and unequalized configurations. In the unequalized state, the DFE maintap was allowed to vary to control the equalizer gain.

The data collected was converted into cumulative distribution functions (CDF) of the slicer SNR, with the objective of gathering data measuring the impact of real-time adaptive
equalization on the SNR and outage performance of high data-rate QAM transmission. Figure 3 shows the results of transmitting between two different rooms (R219 and R202) at Crawford Hill. For both 4- and 16-QAM (10 and 20 Mbps) constellations, the plot shows curves both with and without equalization, but in 64-QAM mode (30 Mbps) links could not be reliably established without the DFE operating. Figure 4 shows similar data taken at UCLA, displaying the CDF for tests within Room 1, between Rooms 1 and 2, and between Room 1 and the hallway, but only for 16-QAM (20 Mbps) mode.

Figure 3 indicates that the median SNR of the equalized receiver is at least 13 dB better than the unequalized receiver for 10 and 20 Mbps transmission, and the 30 Mbps links require equalization to operate over this particular channel (between two rooms separated by approximately 11 meters). Between rooms R202 and R206, the median SNR gain was found to be 10-11 dB, and between rooms R202 and R225, communications were only possible in any of the modes when equalization was used.

Similarly, Figure 4 shows median SNR gains of 11-13 dB for the 16-QAM case (20 Mbps) at the UCLA site. For 16-QAM, the theoretical additive white Gaussian noise (AWGN) bit-error-rate (BER) at 20 dB SNR is about 10-6. With a DFE running at this SNR, Figure 4 shows approximately 3% outage for links within the same room and roughly 10% outage between rooms. For an unequalized system, these figures increase to almost 70% and 85%, respectively. Results using the low-rate (10 Mbps, 4-QAM) and high-rate (30 Mbps, 64-QAM) links generally paralleled these figures.

These two experiments seem to validate the theory that equalization is a powerful technique for enabling high-speed digital QAM communications in indoor environments. In particular, the outage probabilities at reasonable uncoded bit-error-rates can be improved from barely usable to practical by using decision-feedback equalization.

The first-generation testbed is primarily useful for exploring the role of equalization, but further refinements of the wireless testbed are currently being tested and planned. The second-generation design includes an eight-antenna receiver beamcombiner using a custom UCLA integrated circuit [19] and it allows variable equalizer lengths. Later versions will incorporate additional custom UCLA integrated circuits as described in the following sections, to allow
fully-variable bitrates, four-antenna beamcombining at both transmitter and receiver, and other features in extremely compact receivers. These testbeds all provide opportunities to bridge the gap between theoretical and simulation studies and physically realizable systems that provide real-world communications.

IV. Digital Design

Realization of a low-cost, broadband wireless modem with spatial diversity depends on the development of multi-channel integrated RF front-ends and digital baseband modems. One of the fundamental design decisions in the development of a multi-antenna modem is placement of the antenna beamformer and combiner. In this design, the antenna beamformer in the transmitter and the antenna combiner in the receiver are both implemented digitally. While this results in duplication of RF hardware, the all-digital approach enables repeatable performance and a clean analog/digital interface. Other desirable features in the baseband modem include support for variable signal bandwidths and flexible digital IF. The digital receiver should incorporate techniques to compensate for impairments such as adjacent-channel interference (ACI) and multipath. The challenge in the digital modem design is to incorporate all of the necessary signal processing into a small, clean solution while minimizing constraints on the analog front-end.

Using a 0.6µm, triple-metal CMOS process, the core diversity QAM modem has been integrated into a 2-chip solution operating at 3.3V. The flexible chip set supports 4, 16, 32, 64, 128, and 256-QAM formats, 1 to 4 channel antenna beamforming, and continuously variable symbol rates from 0.5-8 MBaud. All of the necessary signal processing, including limited channel-select filtering, matched filtering, decision-feedback equalization, synchronization, and Gray/quadrant encoding are included. Both chips can communicate with an HC11 microcontroller for convenient control and monitoring. With four real IF signals, the digital modulator and receiver can interface to any RF front-end with suitable IF, including the prototype dual-conversion system described in section III and the proposed CMOS front-end presented in Section V. Future generations of this digital modem could drive integration of the modulator, receiver, data converters, and error correction into a single chip using a more modern 0.35µm or 0.25µm CMOS process [20].
IV.1. Modulator

The digital variable-rate QAM modulator architecture is shown in Figure 5. This unique architecture allows the off-chip digital-to-analog converters to operate at a fixed sampling clock rate, with all necessary rate conversion accomplished through digital interpolation. In general, the input and output rates may be incommensurate. The modulator accepts external parallel and serial inputs or can generate training data using a programmable linear feedback shift register. The input stream is then optionally Gray and differential quadrant encoded before being mapped to the desired QAM constellation. After square-root Nyquist filtering at two samples/symbol, the signal is polynomial interpolated up to the output sampling rate [21,22]. The single complex signal is then broadcast to four complex coefficient multipliers implementing the antenna beamforming. The beamformer coefficients are obtained from the receiver chip through the microcontroller interface. Four mixers and a direct-digital frequency synthesizer (DDFS) upconvert the complex baseband beamformer outputs to a user-programmable IF up to 70 MHz. The four real signals are then optionally filtered to compensate for sync distortion and delivered to four, off-chip digital-to-analog converters. The modulator chip is currently in fabrication.

IV.2. Receiver

The receiver architecture including an external IF analog front-end is illustrated in Figure 6. The 4-channel analog front-end downconverts the QAM signal to a fixed low IF of F_{sample}/4. The analog bandpass filter selects an 8 MHz channel, and the resulting low-IF signals are then digitized by four, analog-to-digital (A/D) converters. Both the downconversion oscillator and A/D sampling clock operate open loop. Carrier and timing offsets are compensated using all-digital techniques.

Each of the four receiver inputs pass through identical variable-rate demodulators. A quadrature mixer downconverts the real IF inputs to complex baseband signals. The choice of IF results in the trivial down-conversion tone \( \exp(j\pi n/2) = \{1,0,-1,0\} + j\{0,1,0,-1\} \), reducing the mixer to a simple negater and multiplexer. In this case, the hardware savings associated with eliminating four true I/Q mixers operating at the sampling rate outweighs the reduced flexibility of a fixed IF. Following the trivial mixer, the signal passes through a programmable channel-
select filter with 1 to 4 octaves of rejection. At the maximum symbol rate, the external analog filter performs the primary channel selection and this digital filter simply eliminates the mixing image. Due to the difficulty in designing a sharp, variable-bandwidth analog filter, the digital receiver must provide additional filtering at the lower symbol rates to eliminate adjacent channel interference passed by the analog filter. Obviously, this digital channel-selection technique cannot eliminate arbitrarily-large adjacent channels due to internal dynamic range constraints. The internal precision allows an input signal-to-ACI ratio of -20 dB with a corresponding decision slicer SNR of 30 dB. After eliminating the mixing image and ACI, the four complex signals are resampled from the input sampling rate down to twice the symbol rate under control of the timing recovery loop. Like the modulator, the receiver employs a polynomial interpolator.

The timing-recovered complex baseband signals output from the 4-channel demodulator are subsequently weighted and summed by the adaptive antenna combiner to produce a single complex output. The combiner is logically partitioned into four, self-contained adaptive taps each containing a complex multiplier and a sign-LMS update section. Each tap updates its locally-stored complex coefficient using an error signal generated at the decision slicer. This parallel-tap design allows simple scalability - inclusion/exclusion of channels without altering the timing. Because interference and multipath characteristics are different for each frequency slot, the coefficients may be stored for later use when the modem returns to the same frequency. Shadow registers allow off-line loading and saving of the coefficients, which minimizes reconfiguration time. The antenna combiner location was selected to minimize hardware duplication while preserving performance of the adaptive algorithm. Simulations demonstrate degraded performance in the presence of ACI motivating placement of the antenna combiner after the channel-select filter. In addition, the LMS algorithm requires 1-to-1 correlation between the input samples and errors, requiring the combiner to be located after the interpolator.

Adaptation of the antenna combiner coefficients simply attempts to minimize an error metric at the decision slicer. This minimization is in general independent of the antenna placement. For the special case where the antennas are placed in a regular array, the combiner can be treated as a beamformer which electronically directs the antenna pattern towards the desired signal and away from interfering sources or dominant multipaths. Regular placement corresponds to uniform spatial sampling which enables tractable analysis. Figure 7 illustrates measured performance for
a linear antenna array with I/2 spacing. The desired 4 MBaud source has a direction of arrival (DOA) of 0° measured perpendicular to the plane of the array. A 6 MHz co-channel interferer (CCI) arrives at a DOA of 30° and an SIR of 12 dB. With the antenna combiner disabled, the single-channel receiver is helpless against the interferer and accepts a 12 dB slicer SNR. With the 4-channel combiner enabled, the receiver achieves a 30 dB slicer SNR. The antenna pattern computed from the combiner coefficients demonstrates a 20 dB notch at a 30° direction of arrival.

After matched filtering the combiner output, the decision-feedback equalizer removes intersymbol interference caused by multipath propagation. Even in benign indoor environments with delay spreads of 25 ns, 8 MBaud signals experience significant multipath dispersion mandating an adaptive equalizer. The equalizer consists of two transpose-form adaptive FIR filters, carrier phase derotator, decision slicer supporting 4, 16, 32, 64, 128, and 256-QAM formats, error formatter, and constant modulus block. The feedforward filter supports both T and T/2-spaced operation with programmable gain tap location and filter length from 1 to 8 taps. With up to 16 feedback taps, the feedback filter spans 2 μs at 8 MBaud and contains sufficient guard bits to compensate a +3 dB postcursor. Like the antenna combiner, the equalizer contains shadow coefficient registers for rapid reconfiguration. Following the feedforward filter, the derotator compensates carrier phase and frequency offsets under control of the carrier recovery loop. This placement of the derotator results in a 1-delay loop, which allows maximum loop gain without sacrificing stability. Wide loop bandwidths enable the receiver to compensate for phase noise introduced by analog oscillators in the RF conversion. In addition to derotating the complex received signal, this block also derotates the complex half-baud sample used in the timing recovery loop and re-rotates the complex errors for adapting the feedforward filter and antenna combiner.

Following the derotator, the decision slicer determines the hard decisions and errors for square QAM constellations using a simple multiplexer [23]. For 32 and 128-QAM cross constellations, the hard decisions are multiples of 1/6 and 1/12 respectively. These values are also easily sliced on the 64 and 256-QAM grids by scaling the signal by 3/4 to obtain multiples of 1/8 and 1/16. This scaling is performed at the equalizer input rather than at the slicer to maintain a fixed gain tap reference across all QAM modes. Finally, the error format and constant
modulus blocks compute the appropriate error signals for the adaptive antenna combiner and equalizer. Allowing simultaneous carrier acquisition and combiner/equalizer adaptation, the constant modulus error is given by \( \mu * \text{soft} * (|\text{soft}|^2 - R^2) \), where \( R \) is a constellation dependent constant. After carrier recovery, the receiver switches to decision-directed mode.

The synchronization section performs automatic gain control (AGC), carrier recovery, and timing recovery. In the AGC loop, the gain detector selects the maximum absolute value of the four inputs and computes the square of the result. This maximum selection approach prevents clipping, which is more detrimental to the received bit error rate than the softer degradation associated with under loading the A/D. The power estimate is then compared to a programmable threshold and averaged prior to digital-to-analog conversion. The carrier recovery loop employs a decision-directed phase/frequency detector \([24]\) and a proportional-plus-integral loop filter. The loop filter output drives a ROM-based quadrature DDFS, producing the complex tone \( \exp(j\omega n) \). The all-digital timing loop generates a timing phase estimate using the half-baud samples and hard decisions. After passing through a proportional-plus-integral loop filter, the timing estimate drives a numerically-controlled oscillator which generates the recovered clock and sampling phase offset for the interpolator.

In addition to the fundamental QAM receiver datapath and synchronization, the chip depicted in Figure 8 includes numerous peripheral functions. A data format block performs Gray and differential quadrant decoding of the hard decisions prior to delivering the data off-chip in parallel or serial format. A windowed accumulator provides an estimate of the SNR by averaging the decision error power. Training sequences may be generated using a linear feedback shift register with programmable generator polynomial and initial state. Finally, a general purpose DDFS with programmable frequency control word can generate a digital output tone with frequency from 0 to 40 MHz. When used with an off-chip D/A and lowpass filter, this DDFS can provide the necessary tones for IF downconversion.

V. Analog Design

We now describe the analog portions of the proposed transceiver. Submicron CMOS processes provide transistors with high \( f_T \) which are suitable for RF applications. The memory industry has the highest volume of production and uses CMOS process, which makes CMOS the least
expensive among all technologies. If the circuit performance of CMOS can be made comparable with bipolar and GaAs which traditionally have been used for RF applications, CMOS would be preferred over other technologies for lower cost. One of our goals is to demonstrate the ability of CMOS for 2.4 GHz RF circuits.

The 2.4 GHz ISM band was chosen for our system. One of the major obstacles in this band is the strong interference from microwave ovens at the middle of the band, which can degrade the receiver sensitivity due to the limited blocking dynamic range. Beamforming requires duplicated transceivers for each antenna on the same die, which limits the power consumption and the chip area for each transceiver. Any off-chip component requirement would be multiplied by the number of antennas, which is unacceptable. This dictates a fully on-chip image rejection in the receiver to prevent bulky and expensive off-chip IF filters.

Assuming the main application of the system is internet access, the channel is highly asymmetric. The mobile unit sends a web site path and it downloads a large pack of data. The transmit activity would be less than 10%. In this case, the power consumption of the transceiver would be dominantly defined by the receiver. The power consumption of the receiver should be minimized, while the transmitter can be designed with a less stringent power consumption specification. All the transceivers on the same die share the one synthesizer of which the effective power consumption will be divided by number of transceivers. The synthesizer power consumption is not as significant as the receiver.

V.1. Receiver Design

For on-chip image rejection, double quadrature image rejection mixers with polyphase filters are used with a stringent image rejection of 60 dB as the goal. The mixers and the resistors and capacitors in the polyphase filter need to be 0.1% matched for 60 dB image rejection. At high frequencies, mismatches in the NMOS transistors introduce gain and phase mismatch in the mixers. At low frequencies, the LO signal driving the mixers can be a square wave, which overcomes the effect of DC offset voltage due to transistor mismatches. Thus, the high frequency mixer at 2 GHz cannot provide the required image rejection. The first IF was chosen at 270 MHz to achieve 40 dB image rejection from the preselecting BPF following the antenna. In this way, only 20 dB image rejection is required from the first image rejection mixer. This corresponds to
10% matching, which is easily achievable. Another mixer down-converts the signal from 270 MHz (first IF) to the 2nd IF. The 2nd IF is at 10 MHz, so that the desired channel is higher than the flicker noise corner frequency. The mixer and the following polyphase require 0.1% matching, which has been achieved with a very careful circuit and layout design. Since the polyphase filters are lossy, they have been interleaved with amplifiers to maximize the total dynamic range and the sensitivity of the receiver.

In the final IF (10 MHz), the system encompasses a programmable gain amplifier (PGA), the active filter, and the continuously variable gain amplifier (VGA) preceding the A/D. The PGA is used to overcome the input noise of the filter and the last variable gain amplifier is used to amplify the signal at the output of the filter to occupy the input full range of the A/D, which minimizes the required number of bits in the A/D. The bandpass filter (BPF) has a fixed center frequency and variable bandwidth. To realize such a bandwidth-adaptive filter, a lowpass filter (LPF) and a highpass filter (HPF) with independently controllable edge frequency are used. In the 10 MHz case, this approach reduces the total noise of the resulting BPF by 40%, compared to a common approach to implement the BPF (applying bilinear transformation on the equivalent LPF) with the same filter characteristics. The direct approach to HPF, which is very sensitive to parasitic capacitances of the circuits, is impractical at high frequencies. To overcome this problem, the HPF is realized by a LPF in the feedback path of a gain amplifier. At low frequencies, the circuit has a unity gain feedback path. At high frequencies, the LPF in the feedback path breaks the feedback path and allow the gain amplifier to have its maximum gain. This combination forms a HPF.

A unique feature of this receiver is its power consumption adaptivity. For each block in the receiver there is a fundamental relationship between the power consumption and the dynamic range. Every 10 dB improvement in dynamic range requires 10 times the power consumption. The on-chip IF active filter usually has several stages in cascade, which results in accumulated noise and nonlinearity. Thus, the active filter is usually the dominant limiting factor of the dynamic range for the whole receiver. The required instant dynamic range of the receiver is set by the scenario. If the desired signal and the interferers are both weak, enough gain can precede the filter to overcome its noise. If the desired signal is large, it can overcome the noise of the filter and the desired S/N can be achieved. In both cases, a low noise filter with high linearity
(high instant dynamic range) is not needed. The worst case is when strong interferers accompany a weak desired signal. Strong interferences demand highly linear filter and prevent large enough gain before the filter, while the weak desired signal requires a low noise filter. This worst case can be detected by comparing the signal power at the input and the output of the filter. In the first two cases, the regular 20 mW low dynamic range filter is used to minimize the power consumption. When the worst case is detected, the normal filter will be substituted with a 200 mW high dynamic range filter to increase the worst case dynamic range. Since the worst case is infrequent, the average power consumption will be mainly set by the lower power filter.

The complex constellation of 64-QAM has very close signal points. Even a small jump in the gain of the RF receiver increases the BER. For 64-QAM and low BER, 9 bits of gain control is needed for a step PGA, which requires large area. The alternative method is to use a continuously varying gain amplifier (VGA), which does not have any jump in the gain. However, with the same input noise, linearity, and gain range, a VGA typically consumes 2 to 3 times more power vs. a PGA. By using the channel model and the indoor delay spread, the path loss variation in the channel for the maximum frame length is less than 20 dB for 98% of situations. This led to the optimized combination of the PGA and VGA. During the training sequence at the beginning of each frame, the PGA with 70 dB gain range and 3 dB gain steps sets the required coarse gain, while the VGA with a gain range of 0 to 20 dB is set in the middle and is used for fine tuning of the gain. During the data section of frame, PGA gain will be constant and the channel pathloss variation will be compensated by the VGA to prevent any gain jump.

V.2. Transmitter Design

In the transmitter path, the signal is large enough so that the flicker noise and DC offset do not significantly degrade the signal quality. To reduce the speed and the power consumption of the transmitter DAC, a direct up-conversion was chosen for the transmitter. In this case, the image of the signal has the same power as the main signal. For 40 dB final transmitted S/N, a 45 dB image reject in the quadrature up conversion mixers is adequate, which can easily be achieved in practice.
The critical block of the transmitter is the power amplifier. With a maximum average power of 20 mW, -50 dBc off-channel leakage, and 5.7 dB peak/average power ratio, it is very difficult to have efficiency higher than 2%, unless complicated linearization methods are used.

Fortunately, for the scenario of interest the transmitter has less than 10% activity and the mean average transmitted power is 2 mW. Thus, even with 1% power efficiency in the power amplifier, it has only a 20 mW contribution in the total power consumption of the transmitter, which is acceptable. A simple class A power amplifier with large backoff is used. The 30 dB required power control in the power amp can be easily achieved with switchable binary weighted stages.

V.3. Frequency Synthesizer Design

The synthesizer generates 3 sets of frequencies. A fixed 2161 MHz quadrature LO for the first mixer of the receiver and a hopping quadrature LO of 241 MHz to 321 MHz for the receiver second mixer and 2402 to 2482 MHz hopping quadrature LO for the transmitter up-conversion mixers. To generate a fast hopping LO, a direct digital frequency synthesizer (DDFS) is used with a high speed DAC to generate an agile baseband tone. The DAC’s output is up-converted with a single-sideband double quadrature up-conversion mixer to reject the image. To satisfy 60 dB unwanted signal rejection in the receiver, a 10-bit DAC is needed and the mixers and DAC buffer should be 60 dB linear with 60 dB unwanted sideband suppression in the up-conversion. These very stringent requirements call for a very careful circuit design.

To prevent problems with multi-VCO on the same die and the VCO pulling in the direct conversion transmitter, an offset-VCO at 2161 MHz was used. Its differential output is converted to two quadrature differential output by the polyphase. By dividing 2161 MHz by 8, the quadrature LO required to up-convert the DAC’s output is generated. In this way the 241 to 321 MHz hopping LO is achieved. Up-converting this frequency with the output of the VCO, the transmitter hopping LO is generated.

The DC offset at the output the DAC creates LO leakage. This problem is solved by a local DC loop which removes the DC offset. To achieve the 0.1% quadrature accuracy for the quadrature up-conversion at the output the DAC required for 60 dB sideband suppression, a
phase detector detects the phase error and feeds it back to modify the delay through quadrature paths.

V.4. Analog Design Status

The operation of the individual components of the receiver and transmitter have all been tested with satisfactory results. A fully integrated receiver has been fabricated in a 0.6 micron process and is now undergoing testing. It therefore seems clear that the original design goal of devising an all-CMOS analog front end for a challenging application such as multiple baud rate and multi-level QAM transmission is indeed feasible.

VI. Antenna and Antenna Array Design

This section describes the antenna array design, beginning with a brief review to the principal specification that drove the development of the array. This is followed by a discussion of the alternative antenna elements that were investigated. Finally, the development of a new antenna element [25] is described and some measured results are presented for the element in isolation and in a 4-element array configuration.

The project requirements that determined the antenna array design included element pattern characteristics, impedance bandwidth constraints and issues associated with manufacturability and package integration. The elements comprising the array ideally had to provide omnidirectional patterns in the horizontal or azimuth plane to enable a single array to achieve optimum adaptability. As an alternative, pairs of arrays with hemispherical azimuthal coverage could be used with the associated increase in cost and complexity of having two arrays. Some directivity or narrowing of the beam in the vertical or elevation plane was considered desirable. The bandwidth of the array had to cover the specified ISM band from 2.4 to 2.48 GHz. Ideally, a much broader band antenna was sought that would avoid the need for element tuning. In addition the goal was to focus on antenna elements which had a 50 ohm input impedance and provided a good match (<2:1 VSWR) over the entire range of operation. Finally, the array had to be capable of integration with selected mobile platforms such as laptop computers, and the array should be manufacturable using conventional, low cost printed circuit board manufacturing
techniques. A conceptual integration of a printed circuit antenna array with a laptop display panel that meets these goals is depicted in Figure 9.

A number of antenna elements were considered as candidates for developing the array, including standard monopole and helix antennas, \( \frac{1}{4} \lambda \) and \( \frac{1}{2} \lambda \) patch antennas, and the planar inverted F antenna. The standard monopole is probably the most widely used antenna on existing mobile telecommunication applications, with the axial mode helix coming in a close second. These two antenna types are simple to manufacture, but they are not particularly easy to integrate into handset or mobile terminal cases and they have relatively narrow operational bandwidths. Planar antennas, particularly printed circuit antennas, are therefore of considerable interest for modern applications. While \( \frac{1}{4} \lambda \) and \( \frac{1}{2} \lambda \) patch antennas [26] have been used in a wide variety of systems, their size relative to the mobile terminal and handsets often makes these antennas undesirable for modern mobile applications. Attempts to produce antennas that are more compact than these standard patch designs have produced antennas such as the planar inverted-F (PIFA) antenna [27, 28]. While smaller than the traditional patch antennas, these antennas generally offer no more bandwidth than monopoles and can be difficult to manufacture in production. The investigation of potential antenna elements for the array ultimately led to the development of an entirely new antenna, the Tab Monopole, which features very broadband operation and can be readily manufactured in a printed circuit configuration.

The Tab Monopole consists of a sub-wavelength tapered radiating element fed by a suitable transmission line feeding structure and situated above a planar ground plane. A diagram of a printed circuit version of a prototype tab monopole is provided in Figure 10c. The name “tab monopole” was chosen to distinguish this new antenna from existing printed monopole designs. The tab monopole evolved from attempts to reduce the size and increase the bandwidth provided by existing printed monopole designs.

The development and operation of the tab monopole can best be understood by considering the conceptual evolution from a printed monopole, as illustrated in Figure 10. The standard printed monopole is approximately \( \frac{1}{4} \lambda \) in length. By broadening the width of the monopole into a tab shape the length can be reduced while preserving the input match. Finally, by tapering the tab and further shortening the length, the tab monopole is realized.
The size of the tab monopole element is approximately 0.12 \( \lambda \) high and 0.22 \( \lambda \) wide with a 20-40 degree taper, where \( \lambda \) is the free space wavelength and the design center frequency is 2.6 GHz. The prototype element is fed by a grounded coplanar waveguide line. While other feeding configurations are possible, including microstrip, stripline and coax, coplanar waveguide simplifies the integration of the tab monopole into standard PCB configurations. Vias connecting the front and back ground planes were used in the prototype tab monopole are required to suppress spurious parallel plate modes which are known to occur in the grounded coplanar waveguide [25]. The tab monopole element was fabricated by standard double sided etching of a double-clad printed circuit board, and can be easily located on the edge of a board used for transceiver hardware.

The tab monopole provides a wide operational bandwidth and a broad, nearly omnidirectional azimuth pattern. Figure 11 shows the measured magnitude S11 for the 2.6 GHz prototype tab monopole of Figure 10. The measured S11 magnitude of a \( \frac{1}{4} \lambda \) wire monopole is also provided in Figure 11 for comparison purposes. As can be seen, the input match of the tab monopole is better than -10 dB over approximately 1.5 GHz. This results in an operational bandwidth of better than 50%. Existing monopoles, on the other hand, typically have 10-15% bandwidths. The ultimate match of the tab monopole is also very good, achieving better than -25 dB. The S11 measurements present in Figure 11 were made utilizing an HP 8510B network analyzer with the tab monopole mounted in an anechoic chamber to minimize errors in the measured values.

Measured tab monopole gain patterns for the 2.6 GHz prototype were obtained [25] and it was observed that the vertical polarization pattern in this cut was nearly omnidirectional with a nominal gain of 0 dB, while the horizontal polarization pattern exhibited four distinct lobes.

A photograph of the array incorporating the tab monopole is shown Figure 12. The antenna array is 27.94 cm (11”) long and has four tab monopole elements spaced approximately \( \frac{1}{2} \lambda \) at 2.48 GHz. The measured azimuth patterns for the array at 2.4, 2.44 and 2.48 GHz are shown in Figure 13 and the array input impedances are plotted in Figure 14 as magnitude S11. The patterns are for an equal-amplitude, in-phase feed configuration and the S11 plots are the non-active configuration (i.e. unused elements are terminated in 50 ohms).
In summary, the Tab Monopole is a relatively broad bandwidth antenna that is readily manufactured in large volume production using standard printed circuit board manufacturing methods. It is suitable for linear array applications and can be readily integrated into packages requiring planar element designs such as a display panel of a notebook computer. The tab monopole element provides nearly omnidirectional coverage enabling the adaptive array to take full advantage of its adaptation range. We are presently experimenting with the four-element array in our radio testbed.

VII. Conclusions

We have described the design of a radio transceiver with an unprecedented range of adaptive features. The high level of integration in the circuits we have so far fabricated indicate that it will be possible to build such a radio with reasonable form factor and power consumption, using standard CMOS technology. This may ultimately lead to low-cost implementations. The potential benefits of the adaptive elements in terms of robustness to interference and high spectral efficiency have been discussed, with tests on a prototype platform establishing the usefulness of adaptive equalization for indoor QAM systems.

Our motivation in producing the probing, resource allocation, and adaptive algorithms was to provide a set of compatible techniques for low-complexity implementation. However, the interference interactions in and of themselves are very interesting. There appears to be room for a more rigorous mathematical analysis from the point of view of coupled dynamical systems, the results of which may suggest new algorithmic approaches to stable and rapid convergence. Additionally, for bursty traffic techniques which rely upon receiver/transmitter cooperation are less effective due to the large overhead relative to message size, and the rapid interference dynamics. Devising effective algorithms for this more challenging traffic mix is the subject of ongoing research.

Acknowledgements

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References


Figures

Figure 1: First-generation wireless QAM testbed.

Figure 2: Test locations and local antenna placement patterns.
Figure 3: CDF of slicer SNR, transmitter in R219 (Crawford Hill).

Figure 4: CDF of slicer SNR, 16-QAM constellation (UCLA).
Figure 5: Beamforming QAM modulator architecture.

Figure 6: Diversity QAM receiver architecture.
Figure 7: Measured 16-QAM performance with CCI (SIR = -12 dB, interference DOA = 30°). (a) without antenna combiner and (b) with antenna combiner.

Figure 8: Diversity QAM receiver chip photomicrograph.
**Figure 9:** Four-element Tab Monopole Array integrated with a notebook computer display panel.

**Figure 10:** Evolution of the Tab Monopole from the $\frac{1}{4} \lambda$ Classical Printed Monopole. (a) Classical $\frac{1}{4} \lambda$ Printed Monopole. (b) Top Loaded Printed Monopole. (c) Tab Monopole with both front and side views shown.
Figure 11: Measured magnitude S11 for the prototype 2.6 GHz Tab Monopole and a wire monopole above a ground plane.

Figure 12: Photograph of a printed four-element Tab Monopole array.
Figure 13: Measured azimuth pattern for a four-element printed Tab Monopole array.

Figure 14: Measured S11 magnitude for four Tab Monopole elements arranged in four element linear array with a frequency span of 1 – 8 GHz and a vertical resolution of 5 dB per division.