Analog Integrated Circuit Design

Instructor: Behzad Razavi
56-147D, Eng. IV
(310) 206-1633,

Email: For On-Campus Students: ee215fall2014@gmail.com
       MSOL Students: ee215online@gmail.com

Office Hours: Tue., Thur., 10:30 am - noon
Handouts posted at: http://www.seas.ucla.edu/brweb/teaching.html

Time: TR 2:00-3:50 pm

Place: Boelter Penthouse

Prerequisites: Undergraduate electronics courses, e.g., EE 115B

Credit: 4 Units

Grading: Midterm 30%
           Final 30%
           Homeworks 20% (Late HW Policy: 25% deduction per day)
           (Keep a copy. We are not responsible for lost homeworks.)
           Final Project 20%

Use of laptops is not allowed during class.

Course Textbook:

Recommended Books:

Important Dates:

<table>
<thead>
<tr>
<th>Date</th>
<th>Event</th>
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<tbody>
<tr>
<td>Thur., Oct. 9</td>
<td>HW#1 Due</td>
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<tr>
<td>Tue., Oct. 21</td>
<td>HW#2 Due</td>
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<tr>
<td>Thur., Oct. 30</td>
<td>HW#3 Due</td>
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<td>Thur., Nov. 6</td>
<td>HW#4 Due</td>
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<td>Thur., Nov. 13</td>
<td>Midterm Exam</td>
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<td>Fri. Dec. 12</td>
<td>Final Project Due</td>
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<td>Wed. Dec. 17, 3:00-6:00 pm</td>
<td>Final Exam</td>
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Course Outline

- MOS Device Structure and Circuit Models
- Single-Stage and Differential Amplifiers
- Passive and Active Current Mirrors
- Frequency Response of Amplifiers
- Noise
- Feedback
- Op Amp Design
- Stability and Frequency Compensation
- Bandgap References
- Introduction to Switched-Capacitor Circuits

**Simulation Platform:** HSPICE or Cadence. The device models for 0.18-um technology are posted at [http://www.seas.ucla.edu/brweb/teaching.html](http://www.seas.ucla.edu/brweb/teaching.html) and called 215a.sp (for HSPICE) and 215a.scs (for Cadence). The minimum device width is 0.6 um. The source/drain area is given by W x 0.6 um, and the perimeter by 2W + 1.2 um.

For Cadence tutorials, visit


and log in as:

username: "ee215a 01" (there is a space between a and 0)
password: "open215a"

You need 8-10 hours to learn the basics of Cadence; so be patient!