Single-Stage Amplifiers

Many aspects of the performance of amplifiers are critical. We summarize the trade-offs as shown below.

The amplifiers to be studied here include: CS and CG stages, source followers, and cascades. For each stage, we wish to study both the large-signal and small-signal properties.

**Amplifier Categories**

<table>
<thead>
<tr>
<th>Common-Source Stage</th>
<th>Source Follower</th>
<th>Common-Gate Stage</th>
<th>Cascode</th>
</tr>
</thead>
<tbody>
<tr>
<td>With Resistive Load</td>
<td>With Resistive Bias</td>
<td>With Resistive Load</td>
<td>Telescopic Folded</td>
</tr>
<tr>
<td>With Diode-Connected Load</td>
<td>With Current-Source Bias</td>
<td>With Current-Source Load</td>
<td></td>
</tr>
<tr>
<td>With Current-Source Load</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>With Active Load</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>With Source Degeneration</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Common Source Stage**

- Large-Signal Behavior
What is the small-signal gain in this region?

At point A:  \[ V_{in1} - V_{TH} = V_{DD} - R_D \mu_n C_{ox} \frac{W}{L} (V_{in1} - V_{TH})^2. \]

How do we maximize the gain?

- Small-Signal Analysis

We assume that the bias currents and voltages are chosen such that \( M_1 \) is in saturation and \( Q_i \) in forward active region.

Voltage Gain:

Sometimes we don’t want to use a resistive load. So we try other tricks:

This device can operate as a resistor. How about this:

**Common Source with “Diode” Load**
How do we maximize the voltage gain here?

Large Signal Behavior:

![Graph showing voltage gain](image1)

**Example:** Common Source with PMOS Diode Load

Both versions suffer from serious headroom limitations at low supply voltages.

**CS Stage with Current Source Load**

![Circuit diagram](image2)

What happens to the gain as $I_D$ decreases?

**CS Stage with Active Load**

![Circuit diagram](image3)
CS Stage with Source Degeneration

It is useful to find the Gm of the stage:

Also, the output impedance:

Now let’s compute the gain by noting that:

If $\lambda=0$ and $g_{mb}=0$, then:
**Example**

Source Followers

- **Large-Signal Behavior**

![Diagram of large-signal behavior](image)

Sketch the gain vs. input.

- **Small-Signal Behavior**

![Diagram of small-signal behavior](image)

\[ A_V = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S} \]

- Often use a current source in place \( R_S \) to have a better definition of the bias current.
How good a buffer is a source follower? Input impedance =

**Output Impedance:**

Another method of finding the gain:

- Can eliminate body effect in PMOS version:

- Source followers are used only occasionally. They introduce noise and consume voltage headroom. For example:
Common-Gate Stage

- Large-Signal Behavior

- Small-Signal Behavior

\[
\frac{V_{out}}{V_{in}} = \frac{(g_m + g_{mb})r_O + 1}{r_O + (g_m + g_{mb})r_O R_S + R_S + R_D}
\]

- Input Impedance

\[
R_D I_X + r_O [I_X - (g_m + g_{mb})V_X] = V_X
\]

\[
\frac{V_X}{I_X} = \frac{R_D + r_O}{1 + (g_m + g_{mb})r_O}
\]

\[
\approx \frac{R_D}{(g_m + g_{mb})r_O} + \frac{1}{g_m + g_{mb}}
\]
Example

- Output Impedance

![Diagram of a cascode stage]

Cascode Stage

How do we choose the bias conditions?

![Diagram of a cascode stage with bias conditions]
What is the maximum output voltage swing?

Gain Calculation:

\[ V_{out} = g_{m1}V_1 \]

Output Impedance:

Cascode Stage with Current Source Load

Bias currents and voltages are chosen such that all MOSFETs are in saturation.

Voltage Gain:

\[ I_{out} = g_{m1}V_{in} \frac{r_{O1}}{r_{O1} + \frac{1}{g_{m2} + g_{mb2}}} \]

\[ G_m = \frac{g_{m1}r_{O1}[r_{O2}(g_{m2} + g_{mb2}) + 1]}{r_{O1}r_{O2}(g_{m2} + g_{mb2}) + r_{O1} + r_{O2}} \]

\[ |A_v| = G_mR_{out} \]

How do we maximize the voltage gain?
Actual realization:

Gain calculation:

\[ R_{\text{out}} = \left\{ [(1 + (g_{m2} + g_{m3})r_{O2})r_{O1}]r_{O2} \right\} \left\{ [(1 + (g_{m3} + g_{m4})r_{O3})r_{O4}]r_{O3} \right\} \]

\[ A_v \approx g_{m1} \left( \left( g_{m2}r_{O2}r_{O1} \right) \left( g_{m3}r_{O3}r_{O4} \right) \right) \]

Folded Cascode

The input and cascode devices need not be of the same type.

Large-Signal Behavior

Let the input decrease from \( V_{DD} \) to zero.

\[ V_{in1} = V_{DD} - \sqrt{\frac{2I_1}{\mu_p C_{ox}(W/L)}} - |V_{TH1}| \]
- Small-Signal Behavior
  Similar to that of simple cascode.

**Example**

![Cascoded MOSFETs Diagram]

**Other Applications of Cascodes**

1. Reduction of Miller Effect

2. Shielding

3. Stability

4. Reduction of Device Stress