Single-Stage Amplifiers

Many aspects of the performance of amplifiers are critical. We summarize the trade-offs as shown below.

The amplifiers to be studied here include: CS and CG stages, source followers, and cascades. For each stage, we wish to study both the large-signal and small-signal properties.

Amplifier Categories

<table>
<thead>
<tr>
<th>Common-Source Stage</th>
<th>Source Follower</th>
<th>Common-Gate Stage</th>
<th>Cascade</th>
</tr>
</thead>
<tbody>
<tr>
<td>With Resistive Load</td>
<td>With Resistive Bias</td>
<td>With Resistive Load</td>
<td>Telescopic</td>
</tr>
<tr>
<td>With Diode-Connected Load</td>
<td>With Current-Source Bias</td>
<td>With Current-Source Load</td>
<td>Folded</td>
</tr>
<tr>
<td>With Current-Source Load</td>
<td>With Source Degeneration</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Common Source Stage

- Large-Signal Behavior

What is the small-signal gain in this region?

At point A: \[ V_{in} - V_{TH} = V_{DD} - R_D \frac{1}{2} \mu_C C_{ox} \frac{W}{L} (V_{in} - V_{TH})^2 \]

How do we maximize the gain?

- Small-Signal Analysis

We assume that the bias currents and voltages are chosen such that \( M_1 \) is in saturation and \( Q_i \) in forward active region.

Voltage Gain:

Sometimes we don't want to use a resistive load. So we try other tricks:

This device can operate as a resistor. How about this:

Common Source with “Diode” Load
How do we maximize the voltage gain here?

Large Signal Behavior:

![Diagram of voltage gain curve]

**Example**: Common Source with PMOS Diode Load

Both versions suffer from serious headroom limitations at low supply voltages.

**CS Stage with Current Source Load**

What happens to the gain as $I_D$ decreases?

**CS Stage with Active Load**

It is useful to find the $G_m$ of the stage:

![Diagram of CS stage with source degeneration]

Also, the output impedance:

$$R_{out} = [1 + (g_m + g_{mb}) R_s] r_O + R_s$$

$$= [1 + (g_m + g_{mb}) r_O] R_s + r_O.$$ 

Now let's compute the gain by noting that:

$$\frac{V_{out}}{V_{in}} = \frac{-g_m R_D}{R_D + R_s + r_O + (g_m + g_{mb}) R_s r_O}$$

If $\lambda=0$ and $g_{mb}=0$, then:
Example

Source Followers

- Large-Signal Behavior

Sketch the gain vs. input.

- Small-Signal Behavior

\[ A_v = \frac{g_m R_S}{1 + (g_m + g_{mb}) R_S} \]

- Often use a current source in place of \( R_S \) to have a better definition of the bias current.

How good a buffer is a source follower? Input impedance =

Output Impedance:

Another method of finding the gain:

- Can eliminate body effect in PMOS version:

- Source followers are used only occasionally. They introduce noise and consume voltage headroom. For example:
Common-Gate Stage

- Large-Signal Behavior

\[ V_{out} = \frac{V_{DD}}{r_o + (g_m + g_{mb})r_o R_S + R_S + R_D} \]

- Small-Signal Behavior

Input Impedance

\[ V_X = \frac{R_D I_X - (g_m + g_{mb})V_X}{R_D + r_o} \]

\[ \approx \frac{R_D}{(g_m + g_{mb})r_o} + \frac{1}{g_m + g_{mb}} \]

Example

Output Impedance

Cascode Stage

How do we choose the bias conditions?
What is the maximum output voltage swing?

Gain Calculation:

Output Impedance:

Cascode Stage with Current Source Load

Bias currents and voltages are chosen such that all MOSFETs are in saturation.

Voltage Gain:

How do we maximize the voltage gain?

Actual realization:

Gain calculation:

\[ R_{\text{out}} = \frac{1}{\left(1 + (g_{m2} + g_{m3})r_{02}\right)ro1 + r_{02}} \]

\[ A_0 \approx g_{m1}\left[\left(g_{m2}r_{02}ro1\right)\left|\left(g_{m3}r_{03}ro4\right)\right.\right] \]

Folded Cascode

The input and cascode devices need not be of the same type.

- Large-Signal Behavior
Let the input decrease from \( V_{\text{DD}} \) to zero.

\[ V_{\text{in}} = V_{\text{DD}} - \sqrt{\frac{2I_{\text{D1}}}{\mu pC_{\text{ox}}(W/L)_2}} - |V_{\text{TH1}}| \]
- Small-Signal Behavior
  Similar to that of simple cascode.

Example

Other Applications of Cascodes

1. Reduction of Miller Effect

2. Shielding

3. Stability

4. Reduction of Device Stress