A 32-Gb/s 9.3-mW CMOS Equalizer with 0.73-V Supply

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Abstract

A CTLE/DFE cascade incorporates inductor nesting to reduce chip area and latch feedforward to improve the loop speed. Realized in 45-nm CMOS technology, a 32-Gb/s prototype compensates for a channel loss of 18 dB at Nyquist while providing an eye opening of 0.44 UI at BER $< 10^{-12}$.

I. Introduction

The push for higher data rates in copper media continues unabated. The use of fewer lanes to carry faster data is attractive, especially if the power dissipation per lane can be maintained relatively constant. In the limit, most of the transceiver power is dissipated in the unscalable termination resistors at the transmitter output and the receiver input. It is therefore desirable to minimize the power drawn by all of the building blocks.

This paper describes the design of a full-rate equalizer operating at 32 Gb/s with a 0.73-V supply. Employing a continuous-time linear equalizer (CTLE) and a one-tap decision feedback equalizer (DFE), the circuit draws upon two ideas, namely, nested inductors and latches with inductive feedforward, to achieve a power consumption of 9.3 mW in 45-nm CMOS technology.

Section II provides the background for this work and Section III introduces the equalizer architecture. Section IV deals with the design of the building blocks and Section V presents the experimental results.

II. Background

At 32 Gb/s, the unit interval (UI) of 31.25 ps poses critical challenges in the design of the DFE loop. As explained in [1], the timing constraint is roughly the same for direct DFE, half-rate DFE, and unrolled DFE. The unrolled topology replaces the settling time at the summing junction with the propagation delay through the multiplexer, but it requires that the *data* perform the multiplexing operation and hence have sufficiently large voltage swings. This issue makes unrolled DFEs less attractive at low supply voltages.

In order to process a data rate of 32 Gb/s in 45-nm technology, the stages in the signal path must incorporate inductive peaking, potentially occupying a large area. Moreover, this approach does not adequately reduce the feedback delay, still producing a relatively narrow eye at the summing junction. Fig. 1 shows the simulated eye diagram for a simple DFE loop using CML stages with inductive peaking (including layout parasitics), suggesting that new measures are necessary to ensure a more robust operation. The circuit techniques presented in this paper address these issues.

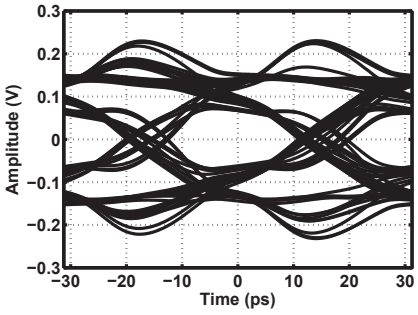

Fig. 1. Eye diagram at the summing junction of DFE loop using CML stages with inductive peaking.

III. Equalizer Architecture

Fig. 2 shows the proposed equalizer architecture. In order to save chip area, the design "nests" the load inductors used in the CTLE and the DFE summer, thus creating mutual coupling between the two stages. As explained in Section IV, this effect can be exploited to further reduce the area.

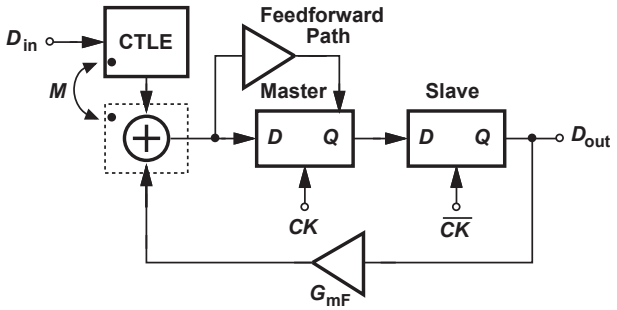

Fig. 2. Proposed equalizer architecture.

The architecture of Fig. 2 also incorporates a feedforward path around the master latch so as to reduce the loop delay. Feedforward is particularly effective here as this latch senses quite smaller voltage swings than those it applies to the slave latch.

The equalizer power dissipation can be reduced through the use of "linear scaling" [1]; i.e., the width and bias current of

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all tansistors can be scaled down by a factor of α and the load resistors scaled up by the same factor. The scaling, however, eventually faces two issues because the inductors must also scale up by a factor of α: (1) the area penalty becomes significant, and (2) the large inductor parasitics degrade the speed. The design reported here makes a compromise between the power dissipation and these two drawbacks.

IV. Design of Building Blocks

This section presents the circuit-level implementation of the equalizer building blocks in 45-nm CMOS technology. The inductors used in this work have been designed and simulated in Ansoft's HFSS and ported into Cadence as S-parameter-based models that are extracted for a frequency range of near dc to 60 GHz.

A. CTLE and DFE Input Stage

In a full-rate equalizer, the CTLE and the input stage of the DFE can be designed as one entity so as to improve the performance. In the prototype reported here, these two blocks consume about 44% of the total power, warranting careful optimization of their performance.

Fig. 3(a) shows the realization of the two stages. In addition to the CTLE, the DFE input also includes a zero so as to raise the high frequency boost [2]. Located at 4 GHz and 4.7 GHz, respectively, these zeros provide a maximum boost of about 10 dB at 20 GHz [gray plot in Fig. 3(b)]. The first DFE tap is a differential pair whose current can be programmed from 0 to 1.5 mA in steps of 100 μA.

While essential to operation at 32 Gb/s, the two differential load inductors in Fig. 3(a) can occupy a large area. The two structures can be stacked, but the large capacitance between the two spirals would severely limit the bandwidth. Instead, we nest L_1 and L_2 as shown in Fig. 3(c), facing two issues. First, since $L_1 \approx L_2$, one inductor must be designed with a larger number of turns so as to fit in a smaller diameter. Second, the coupling factor (≈ 0.3) between L_1 and L_2 alters the behavior of both stages by both feedforward and feedback. This phenomenon can be studied with the aid of the simplified model depicted in Fig. 4. We wish to determine the transfer function from V_{in} to V_{out2}. We have

$$\begin{aligned} V_{out1} &= G_{m1}V_{in}(2R_1 + j\omega L_1) + j\omega M G_{m2} V_{out1} \\ V_{out2} &= G_{m2}V_{out1}(2R_2 + j\omega L_1) + j\omega M G_{m1} V_{in}. \end{aligned} \quad (1)$$

Further manipulating these equations and assuming $\omega^2 M^2 g_{m2}^2 \ll 1$, $2R_1 \gg \omega^2 L_1 M g_{m2}$ for $\omega \leq 16$ GHz, we obtain,

$$\begin{aligned} \frac{V_{out2}}{V_{in}}(j\omega) \quad &\approx \quad 4G_{m1}G_{m2}R_1R_2 + \\ & \qquad j\omega G_{m1}G_{m2}(2R_1L_{eff,2} + 2R_2L_{eff,1}), \end{aligned} \quad (2)$$

where $L_{eff,1} = L_1 + 2MG_{m2}R_1$, $L_{eff,2} = L_2 + M/2G_{m2}R_1$.

Thus, in the presence of mutual coupling, the zero caused by inductive peaking moves to a lower frequency and the magnitude of the boost increases. Simulation of the actual circuit with various capacitances confirms this result [black plot in Fig. 3(b)]. The apparent increase in the value of inductors further reduces the area.

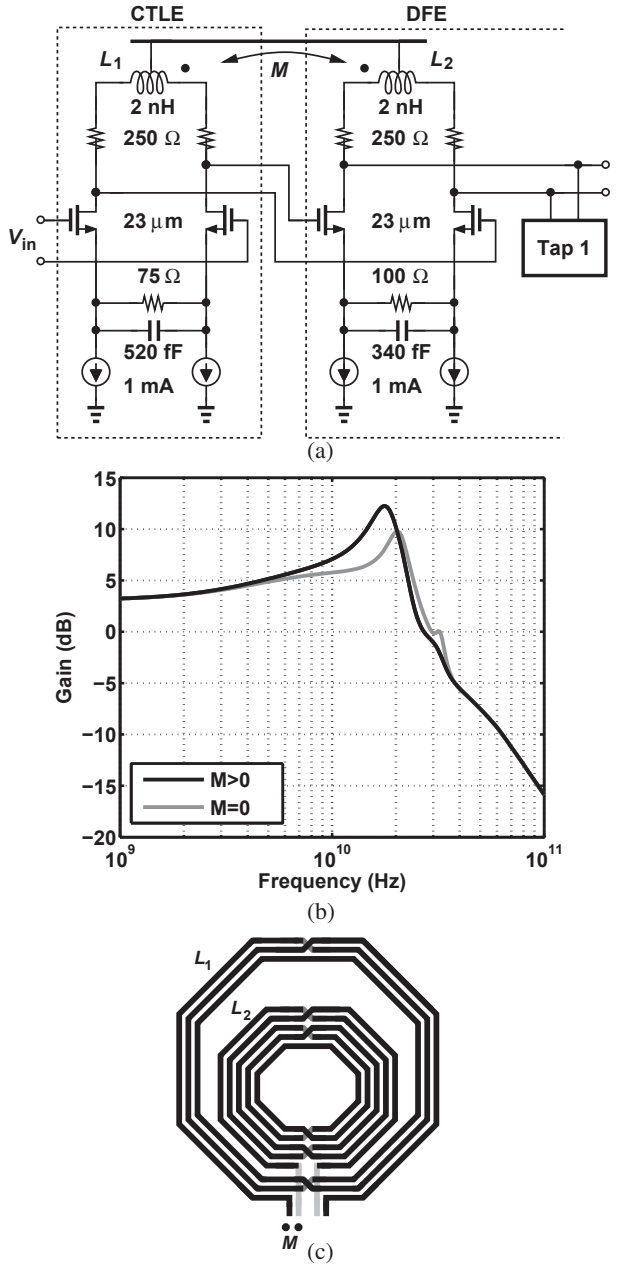


Fig. 3. CTLE and input stage of the DFE: (a) circuit diagram (L=40 nm for all transistors) , (b) frequency response with and without mutual coupling, and (c) nesting of L_1 and L_2.

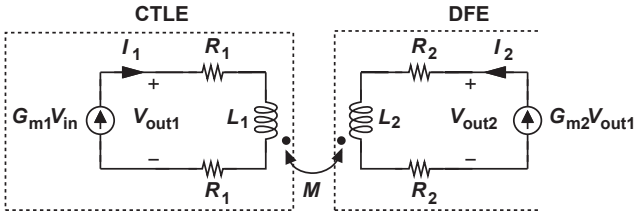
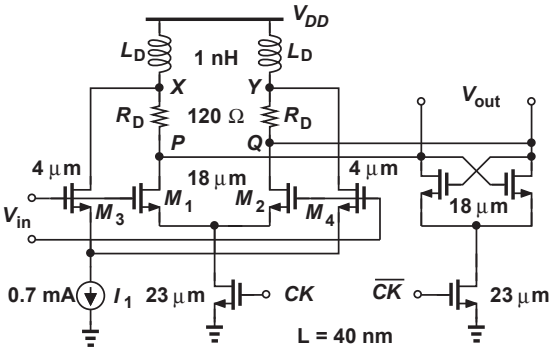


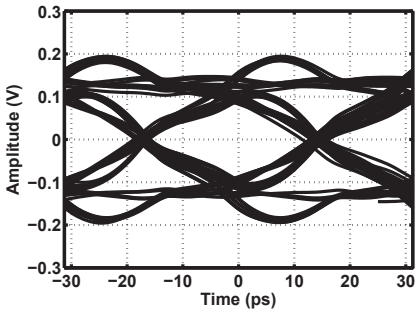
Fig. 4. Simplified model to study nested inductors.

B. Latch with Feedforward

It is possible to improve the speed of latches by means of feedforward [3]. Particularly suited to low-voltage implementations is feedforward to the load inductors as it entails no headroom penalty. Shown in Fig. 5(a), the master latch employs the unclocked differential pair, M_3-M_4, as the feedforward path, allowing the data to propagate towards the output before the main pair, M_1-M_2, is clocked. The injection of this "early" signal to X and Y (rather than to P and Q) avoids additional IR drops, but it also creates a high-pass response. Fortunately, this effect is desirable in a DFE environment for the components that must be fed forward indeed lie at high frequencies.



(a)



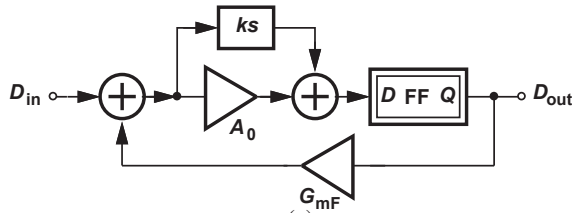
(b)

Fig. 5. (a) Master latch with feedforward, and (b) simulated eye diagram at the summing junction of DFE loop using feedforward.

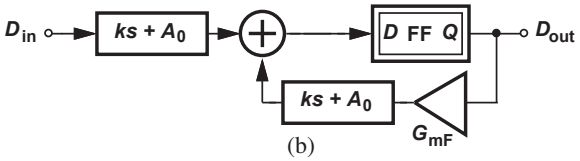
The high-pass behavior of the above feedforward path also affects the nature of the data processed by the master latch. This attribute can be analyzed by modeling the high-pass transfer function as ks and constructing the equivalent circuit shown in Fig. 6(a), where $A_0 \approx g_{m1,2}R_D$. Factoring out the composite transfer function, we arrive at the system shown in Fig. 6(b), recognizing that latch feedforward is equivalent to some boost in both the data path and the feedback path. This is an interesting departure as conventional DFEs assume a flat frequency response for the feedback G_m.

The relative strengths of the feedforward and main paths must be chosen carefully. If excessive, the former produces heavy ringing and hence intersymbol interference. Also, since the feedforward path remains on even during the regeneration phase, it can corrupt the stored bit by the new input bit. In this design, the ratio is about 1 to 5.

Fig. 5(b) repeats the simulations leading to Fig. 1 but with the above feedforward method applied. We observe considerable reduction in the jitter.



(a)



(b)

Fig. 6. (a) Equivalent circuit for analyzing feedforward, and (b) modified equivalent circuit.

The nesting of inductors can also be considered for those in the master and slave latches. However, since the two latches operate on successive bits, the coupling between the inductors would result in ISI. Hence, the two latches' inductors are realized as four independent, single-ended metal-5 to metal-9 stacked structures, each occupying an area of 25 μm × 25 μm.

V. Experimental Results

The equalizer has been fabricated in TSMC's 45-nm CMOS technology. Shown in Fig. 7, the active area of the die measures about 200 μm × 340 μm. The prototype has been mounted directly on a printed-circuit board and the high-speed signals are carried through probes. The circuit operates robustly from 1 Gb/s to 32 Gb/s with a supply voltage ranging from 1.2 V to 0.73 V, at which the results reported below have been measured. The CTLE draws 1.46 mW, the summer 2.59 mW, and the two latches 5.27 mW.

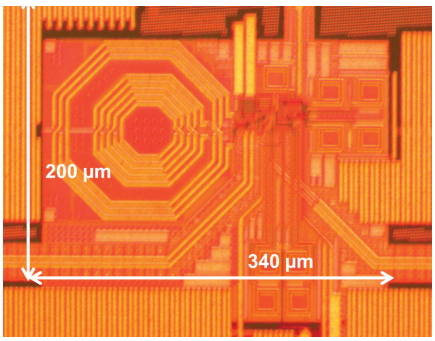


Fig. 7. Equalizer die photograph.

Fig. 8 plots the measured loss profile of the channel used in the equalizer characterization. The channel exhibits a loss of 18 dB at 16 GHz and a deep notch at 10 GHz. Fig. 9 shows the eye diagrams at the output of the channel and at the output of the equalizer. Note that the PRBS generator itself has a peak-to-peak jitter of about 7 ps.

Fig. 10 shows the bathtub curve for 32 Gb/s, measured by

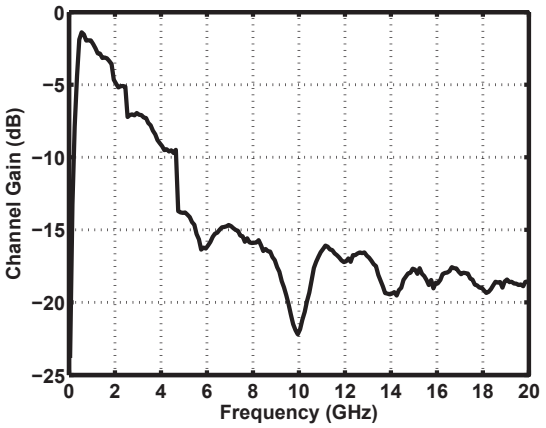
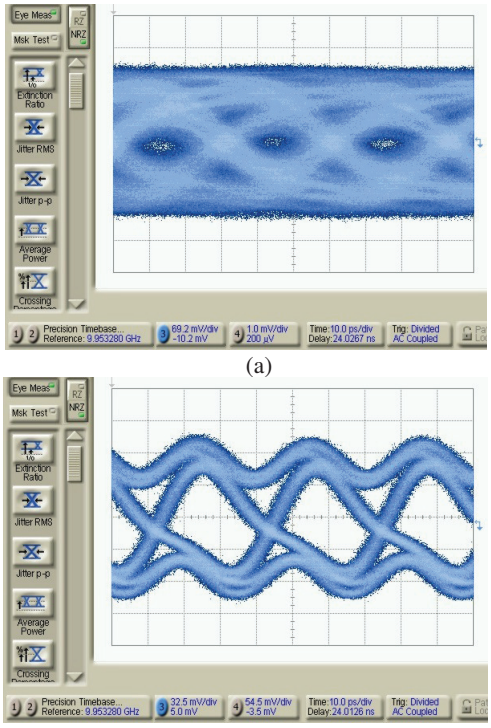


Fig. 8. Measured frequency response of lossy channel.



(a)

(b)

Fig. 9. Eye diagrams at (a) channel output (10 ps/div., 69.2 mV/div.), (b) equalizer output (10 ps/div., 32.5 mV/div.).

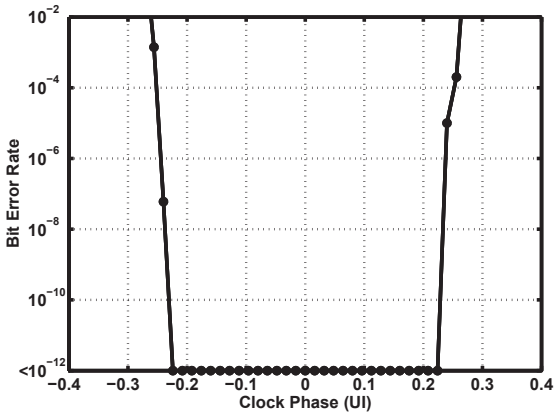


Fig. 10. Measured bathtub curve.

varying the generator's clock phase. We observe a horizontal eye opening of 0.44 UI. If the generator's jitter (≈ 0.22 UI) is discounted, the actual opening is larger.

Table 1 summarizes the performance of our prototype and recent state of the art. This work demonstrates the feasibility of high-speed full-rate DFEs with low power consumption.

Table 1. Performance summary and comparison to prior art

Reference	[4]	[2]	[5]	[6]	[7]	This Work
Data Rate (Gb/s)	40	28	32	27	25	32
Channel Loss @ Nyquist	15 dB	35 dB	36 dB	>10 dB	24 dB	18 dB
BER/ Eye Opening	$<10^{-11}$/ NA	$<10^{-9}$/ 35.6% UI	$<10^{-12}$/ 19% UI	$<10^{-9}$/ 11% UI	$<10^{-12}$/ 44% UI	$<10^{-12}$/ 44% UI
Supply (V)	1.2	1.05	1.15	1.1	1.0	0.73
Power (mW)	45	80*	97.6	11.1	5.8	9.3
Power Efficiency (pJ/bit)	1.125	2.857	3.05	0.411	0.232	0.29
Area (mm^2)	0.05	0.81**	0.018	0.015	0.01	0.068
Technology	65−nm CMOS	32−nm SOI CMOS	32−nm SOI CMOS	40−nm CMOS	45−nm CMOS	45−nm CMOS

* Only for odd and even DFEs. Excludes CTLE, etc.
** Includes TX+RX+PLL.

VI. Conclusion

This paper presents a full-rate equalizer employing inductor nesting to save area and latch feedforward to improve the speed. It is shown that the inductor coupling due to nesting can be exploited to further shrink the area. Also, it is recognized that latch feedforward is equivalent to a high-frequency boost in the feedback tap. Such techniques afford operation at 32 Gb/s with 9.3 mW from a 0.73-V supply, producing an eye opening of 0.44 UI.

Acknowledgments

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