A Low-Power 60-GHz CMOS Transceiver for WiGig Applications

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Abstract—A direct-conversion transceiver including baseband amplifiers and filters employs a 60-GHz quadrature VCO and a feedforward divider with no buffers to achieve a low power consumption. Designed in 40-nm LP CMOS, the radio presents a noise figure of 4.8 to 8.2 dB in the receive mode and an output power of +10 dBm in the transmit mode while drawing 56 mW and 124 mW, respectively.

Recent work on 60-GHz radios has demonstrated high levels of integration in CMOS technology [1, 2, 3]. For such radios to find their way into mobile devices, their power consumption must also be reduced while maintaining both a high receive (RX) sensitivity and a high transmit (TX) output power. This paper describes a low-power 60-GHz transceiver for WiGig applications operating with QPSK modulation. Four principles are presented that improve the performance: (1) a "minimalist" mentality advocating that less hardware translates to less power; (2) use of passive mixers to broaden the bandwidth of the low-noise amplifier (LNA); (3) a method of boosting the gain of active mixers; (4) two methods of increasing the speed of frequency dividers.

The minimalist principle points to "true" direct conversion as the architecture of choice, culminating in the following design techniques: (1) a 60-GHz quadrature local oscillator (LO) directly drives the RX, TX, and synthesizer paths with no frequency multipliers, splitters, couplers, or even buffers; (2) the 60-GHz LO waveform is synthesized directly with no need for injection locking, mixing, etc.; (3) the RX LNA employs only one stage and the TX power amplifier (PA), only two. These techniques collectively stand in contract to those employed in [1-3]. For example, [1] and [2] incorporate four-stage LNAs, and [1] a four-stage PA.

Architecture Fig. 1(a) shows the radio architecture. The receiver consists of an LNA, quadrature mixers, and baseband gain and filter stages. Capacitive coupling between the stages avoids offset accumulation with a programmable cut-off frequency. The linearity of the RF front end allows the RX gain control to be realized only in the baseband, simplifying the design of the LNA and the mixers. The transmitter consists of baseband gain and filter stages, quadrature mixers, a PA, and carrier feedthrough cancellation DACs. The RX gain can be programmed from 66 dB to 12 dB in 1-dB steps, and the TX gain from 15 dB to 7 dB in 1-dB steps. A departure from the minimalist approach is the use of dedicated RX and TX synthesizers, imposing a 4% area penalty but providing enormous gains in terms of the routing of the quadrature LO phases to the mixers.

RX Design Fig. 1(b) shows the LNA and downconversion mixers. The cascode LNA exploits the inevitable mutual coupling between the gate and source inductors to improve the input matching. The choice of passive mixers relates to the required bandwidth: with an average input resistance of about 100 Ω, the four switching paths absorb most of the RF current produced by the LNA, thus minimizing the effect of L_D on the bandwidth. Note that this property evidently has not been recognized in [3].

The downconversion mixers must connect to the LNA at their RF port and the quadrature oscillator at their LO port. The minimum spacing between the LNA and oscillator inductors is determined by the desensitization of the former as a result of the coupling from the latter, inevitably requiring long RF and/or LO connections to the mixers. In order to minimize the LO load uncertainties, the mixers are placed next to the LO transistors and their RF port travels about 100 μm to reach the LNA output. Modeled by L_M in Fig. 1(b), the inductance associated with this wire in fact provides some series peaking and hence does not degrade the performance.

TX Design The minimalist approach also proves useful in the TX design. Fewer RF stages can improve the efficiency and linearity as well as allow a greater fractional bandwidth. The design of the TX path is governed by the LO drive capability as it constrains the size of the upconversion mixer devices, thus placing a lower bound on the input impedance of the PA. The PA must therefore deliver a high output level with relatively small input transistors, in turn demanding a high gain of the upconverter. Shown in Fig. 1(c), the RF section of the transmitter employs active mixers and a two-stage PA. Since the gain of the mixers is limited by the linearity and voltage headroom of their baseband input transistors, a cross-coupled pair, M_1-M_2, is added to boost the gain by about 6 dB. The higher gain allows smaller baseband voltage swings and hence greater overall linearity.

The PA consists of two differential grounded-source stages with an on-chip balun so as to accommodate a single-ended (patch) antenna. Resistor R_1 suppresses common-mode instability without degrading the differential Q.

Frequency Divider With the exception of [4], most 60-GHz CMOS radios have avoided direct LO synthesis, perhaps due to the difficulties in the design of a robust, wideband frequency divider whose input transistors are small enough to be driven by the LO and whose output swing and drive are large enough to drive the next divider. This paper presents a divider that employs two techniques to achieve these properties. As shown in Fig. 2, each latch in the master-slave configuration incorporates a feedforward path [5], impressing the input on the output inductors before the main path is enabled. The feedforward action raises the upper end of the toggle rate at the cost of some increase in the lower end. The second technique involves utilizing both the I and Q phases of the LO to drive each latch, equivalently raising the injection level by about 40%. This ar-

rangement also equalizes the loads seen by the two cores of the quadrature oscillator, avoiding systematic I/Q mismatches.

Experimental Results The transceiver has been fabricated in digital 40-nm LP CMOS technology, occupying an active area of 1.75 mm x 0.84 mm. Figure 3 shows the die photograph.

Figure 4 plots the measured RX NF for a baseband frequency range of 100 MHz to 800 MHz, where most of the WiGig signal energy lies. Also shown in this figure is the measured TX saturated output power and the measured TX output constellation for the WiGig MCS9 data format (QPSK at a raw rate of 2.86 Gb/s). The EVM is −15 dB, meeting the WiGig specification. The TX output P_{1dB} is about +8.8 dBm.

The synthesizer locks to all four channels and exhibits a phase noise of −90 dBc/Hz at 1-MHz offset. The loop bandwidth is about 4 MHz and the measured rms jitter 5.3 ps, well below the tolerable value for the 2.86-Gb/s QPSK signal.

Table I compares the measured performance of this work with that of other single-element transceivers that achieve an output power in the range of 10-12 dBm and are designed in 65- and 40-nm CMOS technologies.

References

[1] Okada et al, IEEE JSSC, pp. 2988-3004, Dec. 2011.
[2] Siligaris et al, IEEE JSSC, pp. 3005-3017, Dec. 2011.
[3] Vidojkovic et al, ISSCC Dig., pp. 268-269, Feb. 2012.
[4] M. Tabesh et al, IEEE JSSC, pp. 3018-3032, Dec. 2011.
[5] B. Razavi, IEEE TCAS I, pp. 1786-1793, Aug. 2009.

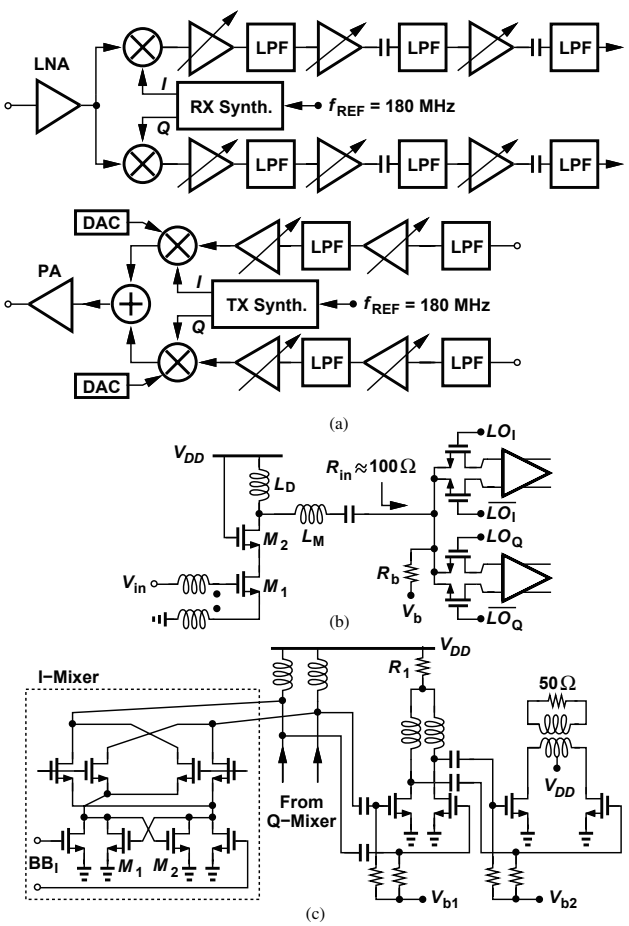


Fig. 1. (a) Radio architecture, (b) RX design, (c) TX design.

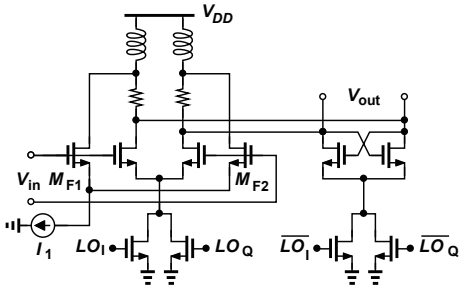


Fig. 2. Latch with feedforward and I/Q inputs.

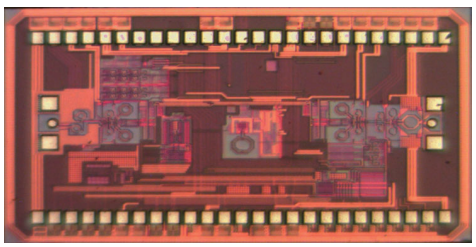
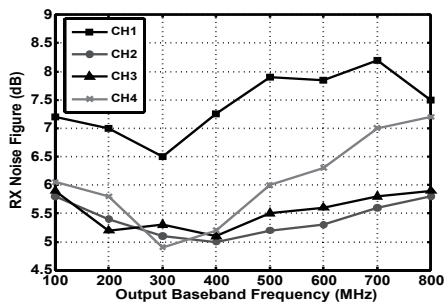


Fig. 3. Transceiver die photograph.



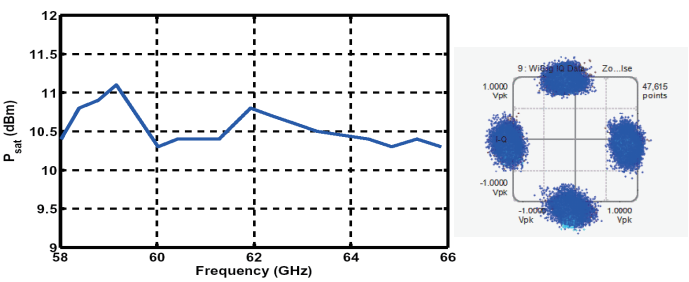


Fig. 4. Measured RX NF and TX P_{sat} and constellation.

	[1]	[2]	[3]	This Work
RX				
NF (dB)	6.8	8–11	5.5	4.8–8.2
Gain (dB)	17.3	32–41	30	12–66
P_{1dB} (dBm)	NA	NA	−31	−25 @ Gain = 12 dB −60 @ Gain = 66 dB
RX+Synth. Power (mW) (Excluding BB)	172	154	147 **	38
BB Power Diss. (mW)	NA	300	NA	18
TX				
P_{sat} (dBm)	10.9	12 *	11	10
Gain (dB)	21	11–18	22	7–15 dB
TX+Synth. Power (mW) (Excluding BB)	292	287 *	202 **	114
BB Power Diss. (mW)	NA	70	NA	11
Modulation and EVM (dB)	BPSK (−18) QPSK (−18) 8PSK (−17) 16QAM (−17)	16QAM (−19)	QPSK (−19) 16QAM (−18)	QPSK (−15)
Synthesizer				
Phase Noise (dBc/Hz)	−95	−99	−96 ***	−90
Ref. Spur (dB)	−58 (@ 20 GHz)	NA	NA	−52
Power Diss. (mW)	81	80	80	30 (RX), 34 (TX)

* Excluding external PA ** Including 20−GHz PLL *** With external 20−GHz reference

Table 1. Performance summary and comparison.