A 10-bit 1-GS/s CMOS ADC with FOM = 70 fJ/Conversion

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Abstract **A pipelined ADC incorporates a precharged resistor-ladder DAC in a multi-bit front-end, achieving fast settling and allowing calibration of both dynamic and static gain errors. Using simple differential pairs with a gain of 5 as op amps and realized in 65-nm CMOS technology, the 10-bit ADC consumes 36 mW at a sampling rate of 1 GHz and exhibits an SNDR of 52.7 dB at an input frequency of 490 MHz.**

I. Introduction

The figure of merit (FOM) of ADCs tends to degrade as higher speeds and/or resolutions are sought. For example, the FOM rises from 6.3 fJ/conversion for an 8-bit, 1.1-MHz ADC [1] to about 500 fJ/conversion for a 12-bit 3-GHz design [2]. It is therefore desirable to develop low-power gigahertz ADCs in the resolution range of 10 to 12 bits.

This paper proposes a pipelined ADC architecture employing a precharged resistor-ladder digital-to-analog converter (DAC) and a multi-bit front end with a low-gain op amp. Avoiding the need for op amp nonlinearity calibration, the ADC only computes the gain error at high speeds and corrects it in the digital domain.

Section II describes our design approach and the resulting ADC architecture. Section III deals with the design of building blocks and Section IV presents the experimental results obtained from the prototype.

II. Proposed ADC Architecture

A. General Considerations

The performance of pipelined ADCs is determined by primarily that of the op amps used in their first few stages. Among the imperfections afflicting these op amps, the finite gain and the nonlinearity have been the target of numerous calibration techniques. However, the nonlinearity poses difficult challenges: foreground calibration may not adequately hold as the temperature varies, and background calibration restricts the input signal bandwidth or dynamic range, does not correct for capacitor mismatch, or requires a slow but accurate auxiliary ADC [3]-[5]. These issues are summarized in [6].

It is desirable to architect the ADC such that the stages *inherently* avoid nonlinearity. To this end, the ADC can resolve several bits in the front end, thus allowing the first multiplying DAC (MDAC) to operate with small output swings. Such swings also improve the settling speed of the MDAC. What remains to be corrected is the gain error arising from the finite gain of the op amp and capacitor mismatches. If possible, the gain error due to the MDAC's incomplete settling should also be calibrated.

While attractive, multi-bit front ends entail another issue: if the multi-bit DAC in the first stage incorporates capacitors, then the mismatch between *each* of these capacitors and the MDAC feedback capacitor must be computed and corrected. We may instead consider a resistor-ladder DAC (RDAC), given that such DACs can achieve linearities exceeding 11 bits ([6]). However, it is generally believed that resistor-ladder DACs are slow, a true statement for stand-alone designs. Nonetheless, our key observation here is that, in a pipelined ADC environment, the DAC output node can be *precharged* to the analog input level, thereby considerably relaxing the settling speed.

B. ADC Architecture

Fig. 1(a) shows the first stage of the ADC architecture followed by the back end. A 4-bit sub-ADC in the first stage along with an MDAC gain of 2 greatly simplifies the design of the op amp. Moreover, a precharged resistor-ladder DAC rapidly establishes the analog equivalent of the sub-ADC output at node X. One bit of redundancy accommodates various errors, including the offsets of the comparators in the sub-ADC and the timing mismatch between the sub-ADC and the MDAC.

The operation of the front end and the timing budgets thereof are explained with the aid of the waveforms shown in Fig. 1(b). For 25% of the clock period (250 ps), bootstrapped switches sample the analog signal on the RDAC output [node X in Fig. 1(a)], the input capacitor of the MDAC, and the input capacitors of the sub-ADC comparators. Next, the sub-ADC is clocked while V_X is held, The coarse digital estimate arrives after 250 ps, turning on one switch in the RDAC and driving V_X to the corresponding value. The last 500 ps of the clock period is allocated to the settling of V_X and the MDAC output, V_{res1}.

The back end of the ADC consists of eight 1.5-bit stages, the first four of which are scaled down by a factor of two.

III. Building Blocks

A. Front-End Stage

To save power, the front end employs a single high-speed resistor ladder to provide three sets of quantities: (1) reference taps for the first sub-ADC, (2) first stage RDAC voltages, and

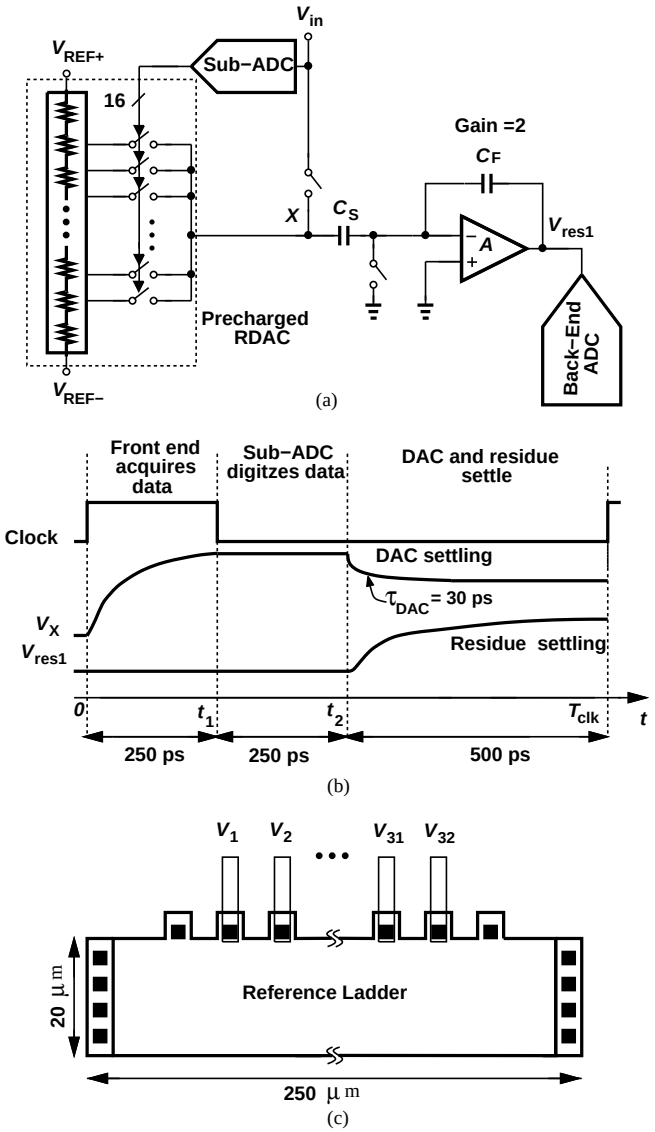

Fig. 1. (a) Front-end stage employs a precharged RDAC and a gain of 2 to improve linearity and speed, (b) conceptual DAC and residue waveforms, and (c) reference ladder structure.

(3) high-precision voltages for foreground calibration of the ADC. As such, the design of the ladder and its associated circuitry plays a critical role in the overall performance. It is important to note that the fast settling of the ladder also allows performing calibration at a high sampling rate and hence correcting for incomplete settling of the MDAC.

The reference ladder [Fig. 1(c)] is realized as a continuous rectangular geometry made of silicided polysilicon, with its taps positioned on the edge to minimally disturb the current flow [6]. This ladder has a total resistance of 150 Ω, which translates to a worst-case Thevenin equivalent of 37.5 Ω, negligibly affecting the RDAC settling and making the resistance of the DAC switches dominant. According to simulations, the worst-case time constant at node X is equal to 30 ps.

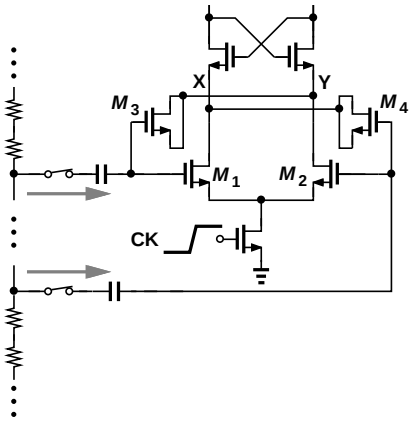

Fig. 2. Effect of sub-ADC kickback noise on the reference ladder.

B. Sub-ADC Kickback Noise

A critical issue in sharing a single ladder between the sub-ADC and the DAC is that the kickback noise of the former may substantially disturb the tap voltages utilized by the latter. It is therefore essential that the disturbance decays rapidly. This design employs a StrongArm comparator for low power consumption, but must deal with its large kickback noise. Fig. 2 illustrates the kickback noise mechanism. When CK goes high, V_X and V_Y are at V_{DD}, and one falls toward ground, coupling through the gate-drain capacitance of M_1 or M_2 and drawing a current from the ladder. Since for most of the 15 comparators in the sub-ADC, the change in V_X is much larger than in V_Y (or vice versa), the kickback noise contains a high differential component.

To remedy this effect, transistors M_3 and M_4 are added so that the large change in V_X or V_Y is coupled to both inputs. In other words, most of the differential error is converted to a common-mode error. Simulations indicate that the kickback noise due to the sub-ADC creates a peak jump of 2.5 mV on the *differential* voltages produced by the ladder and decays in about 30 ps. That is, by $t = t_2$ in Fig. 1(b), the ladder voltages safely settle to their static values.

The multi-bit operation results in a peak single-ended swing of only 75 mV at the output of the MDAC. The MDAC op amp is therefore implemented as a simple differential pair with resistor loads and an open-loop gain of 5. A tail current of 3 mA affords fast settling.

C. High-Speed Calibration

Foreground calibration is performed by applying to the ADC five differential dc voltages provided by the ladder: zero, $\pm V_{REF}/32$, and $\pm 2\,V_{REF}/32$. In a manner similar to that described in [6], calibration begins from stage 6 and proceeds backwards. Note that dynamic gain errors are calibrated even though the input in each case is constant because the MDAC outputs must start from zero and settle anew each time.

IV. Measurement Results

The prototype ADC has been fabricated in 65-nm digital CMOS technology. Shown in Fig. 3 is the die active area, which measures 250 μm $\times$700 μm. The ADC reference voltages are provided externally and the calibration is performed off-chip. Careful simulations including bond wire inductance reveal that V_{REF+} and V_{REF-} in Fig. 1(a) must have *no* bypass capacitors so that they can quickly recover from the switching action of the DAC.

The maximum differential nonlinearity (DNL) and integral nonlinearity (INL) reach 2 LSB and 6 LSB, respectively, before gain error calibration. Fig. 4 plots the calibrated DNL and INL for a sampling rate of 1 GHz. To demonstrate the efficacy of calibration at high clock rates, two cases are investigated: the calibration itself is performed at 100 MHz [Fig. 4 (a)], or at 700 MHz [Fig. 4 (b)]. We observe that the maximum DNL and INL respectively fall from 1.4 LSB and -3 LSB to 0.74 LSB and 1.4 LSB when calibration is performed at 700 MHz. These results suggest that the MDAC in the first stage (and possibly second stage) exhibits incomplete settling and greatly benefits from calibration at a high clock frequency. Note that only the gain error of each stage is calibrated.

Fig. 5 plots the measured output spectrum for input frequencies of 1.7 MHz and 490 MHz at a sampling rate of 1 GS/s. The third-order harmonic at -63.5 dB in the former case confirms the high linearity provided by the resistor ladder. The signal-to-(noise+distortion) ratio (SNDR) is possibly limited by ringing on the reference lines.

The dynamic performance of the ADC is shown in Fig. 6 for a sampling rate of 1 GS/s and analog input frequencies up to 490 MHz. The SNDR varies from 57 dB to 52.7 dB. The spurious-free dynamic range (SFDR) is also measured and observed to vary from 63.5 dB to 60 dB in this frequency range.

The ADC draws 36 mW from a 1.2-V supply, of which 2.5 mW is consumed by the reference ladder, 14.4 mW by the op amps, and 18 mW by the clock tree and the pipeline alignment latches. Computed as 36 mW/(2$\times$460 MHz$\times 2^{ENOB}$), the figure of merit is 70 fJ/conversion. A less conservative clock tree design could improve the FOM considerably.

Table I summarizes the measured performance of the ADC and Fig. 7 expands the FOM plot in [7] to include our work. Note that the design reported in [7] is realized in 40-nm technology and, due to time-interleaving, may suffer from a large input capacitance. Moreover, the design relies on the raw device matching of the technology and does not calibrate the gain error.

V. Conclusion

Pipelined ADCs can greatly benefit from the use of multi-bit front ends that incorporate precharged resistor-ladder DACs. With the settling speed afforded by the low-resistance ladder, the ADC can be calibrated at high sampling rates, thus correcting for the incomplete settling of the MDACs. In addition, RDACs simplify the calibration logic by reducing the required correction to only that of the gain error. Utilizing these concepts, a 10-bit 1-GS/s ADC has been demonstrated that improves the FOM by a factor of 2.6 with respect to the state of the art.

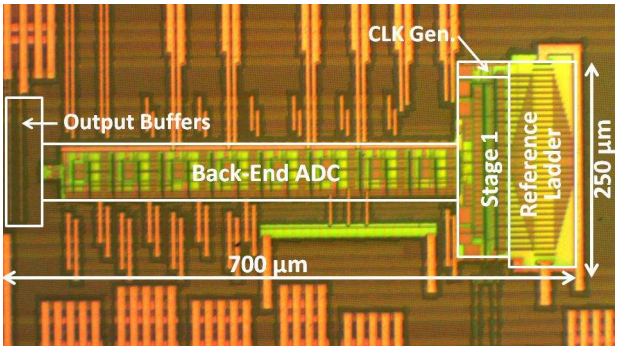

Fig. 3. ADC die photograph.

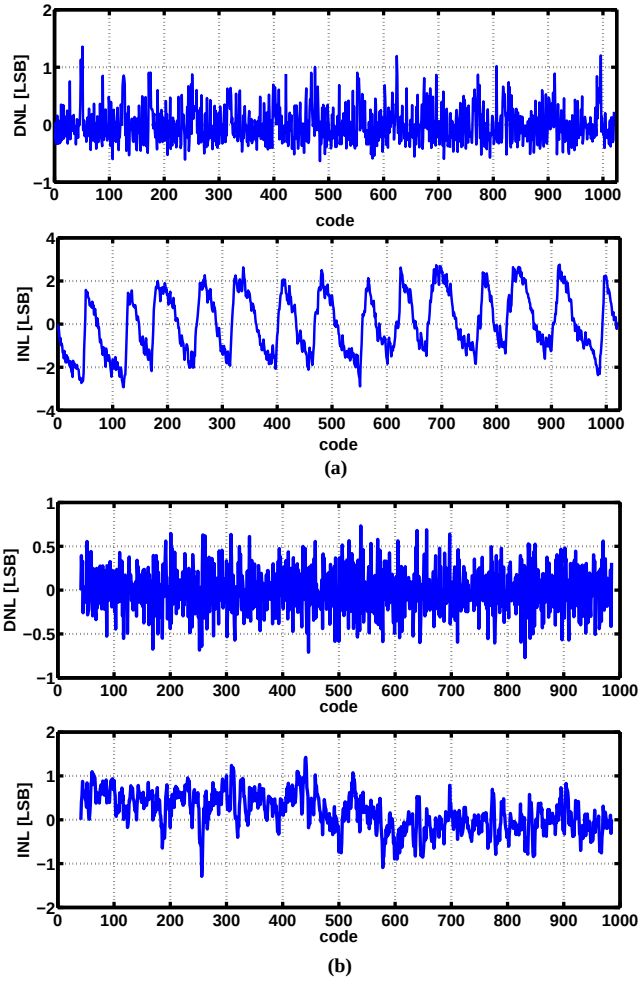

Fig. 4. Measured DNL and INL at f_{sample}=1 GS/s with gain error calibration run at (a) 100 MHz and (b) 700 MHz.

Acknowledgment

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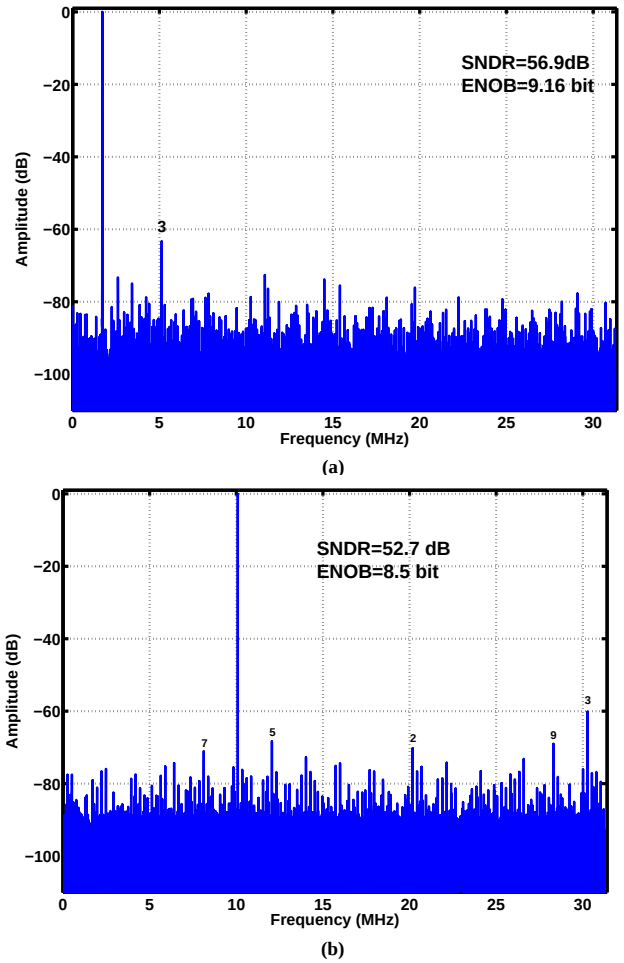

Fig. 5. Measured spectrum at f_{sample}=1 GS/s with (a) f_{in}=1.7 MHz and (b) f_{in}=490 MHz (down-sampled by a factor of 16).

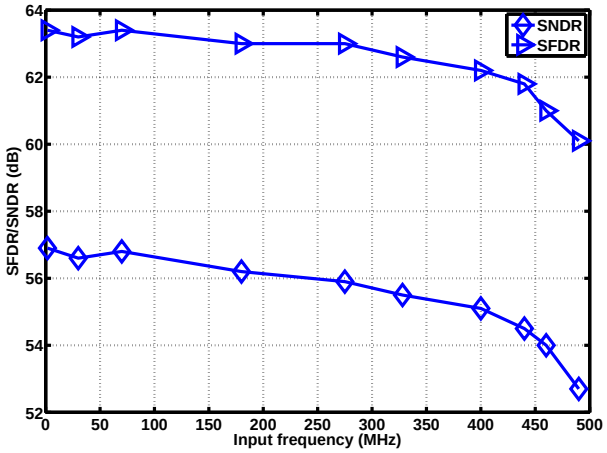

Fig. 6. Measured SNDR/SFDR as a function of input frequency at f_{sample}=1 GS/s.

TABLE I
ADC Performance Summary

Resolution	**10 Bits**
Sampling Rate)	**1 GHz**
Input Capacitance	**0.7 pF**
Input Range	**1.2 $V_{pp-diff}$**
Power Consumption **Ref. Ladder Power** **Analog Power** **Digital Power**	**36 mW** **2.5 mW** **14.4 mW** **18 mW**
SNDR	**57 dB**
Supply Voltage	**1.2 V**
Technology	**65 nm**
FOM	**70 fJ/Conv.**
Active Area	**0.175 (mm^2)**

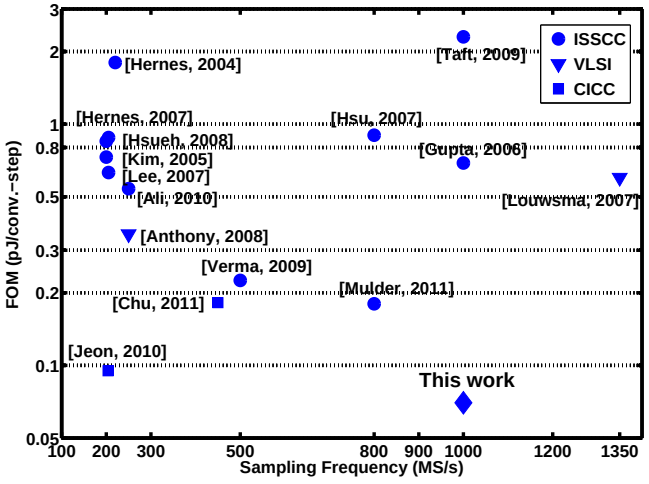

Fig. 7. FOM comparison with prior art.