8.8 A 20Gb/s 40mW Equalizer in 90nm CMOS Technology

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In order to reduce the pin count of chips and the complexity of the routing on printed-circuit boards and backplanes, it is desirable to replace a large number of parallel channels with a few serial links. Such a transformation can also potentially save significant power because it lowers the number of output drivers while maintaining the I/O voltage swings and termination impedances relatively constant. It is therefore plausible that data rates approaching 20 Gb/s will become common in the near future. At these speeds, the loss of FR4 boards poses a great challenge, requiring heavy equalization. From circuit design point of view, it is simpler to employ linear equalization (in the transmitter and the receiver), but from system design point of view, two serious issues make this approach unattractive: the amplification of crosstalk and the lack of ability to equalize for impedance discontinuities (sharp notches in the channel frequency response). In an optimum, yet practical system, one would place 4 to 5 dB of linear equalization in the transmitter and a similar amount in the receiver, and perform the remaining equalization by means of a decision-feedback equalizer (DFE), thus alleviating both issues.

A few CMOS solutions for rates near 20 Gb/s have been reported, *e.g.*, [1] employs duobinary signaling to equalize for 14 dB of loss at 10 GHz, [2] exhibits a high bit error rate (BER) (10^{-8}) for a loss of 11 dB at 10 GHz, and [3] exploits about 20 dB of linear equalization for a loss of 21 dB at 10.5 GHz. The need therefore exists for an NRZ DFE solution that compensates most of the loss.

This paper introduces a half-rate speculative DFE architecture that substantially improves the speed of the first tap, affording operation at 20 Gb/s in 90-nm CMOS technology with low power consumption. Figure 8.8.1 shows the receiver architecture in single-ended form. A linear equalizer is followed by a one-tap DFE and a demultiplexer. (Additional taps face less serious speed requirements and can be added with minimal power overhead.) The DFE consists of two branches that are multiplexed by MUX_1 as in a speculative topology and followed by two latches, L_1 and L_2, as in a half-rate architecture. In contrast to the DFE in [4], which operates two independent speculative equalizers at half rate, the proposed architecture merges the two paths, reducing the number of analog summers by a factor of two. As a result, the power consumption is lowered. The area savings are also significant if inductive peaking must be used to increase the bandwidth. The built-in offset necessary for each speculation is set by h_1.

The merging of the two paths necessitates the use of another multiplexer, MUX_2. In the positive half cycle of the clock, MUX_2 selects the odd channel output as the previous bit, applying the result to MUX_1 for speculation. In the negative half cycle, the even channel output plays the same role. The critical path now consists of MUX_1, L_1 (or L_2), and MUX_2. Note that the output of MUX_1 carries full-rate data while L_1 and L_2 are clocked at 10 GHz.

The DFE architecture of Fig. 8.8.1 employs three techniques to improve the speed of the critical path. First, since the delay of the speculation paths is not critical (for the first tap), amplifiers A_1 and A_2 have been inserted to increase the swings applied to MUX_1, thereby allowing faster steering of the current in the critical path. Second, the feedback memory element necessary for half-rate operation is reduced from a flipflop to a latch (L_1 and L_2). This is possible because MUX_2 itself is driven by the clock, and, by virtue of the clock phase choice, acts as a slave for each latch. The lack of regeneration within MUX_2 proves unimportant because, when, say, L_1 is in the sense mode, MUX_2 selects the output of L_2. The third technique is to merge MUX_1 and MUX_2 into a stacked structure, saving the delay associated with one MUX. This point is explained below.

Figure 8.8.2 shows the details of the linear equalizer. For testing simplicity, all of the linear equalization (9 dB) is placed on the receive side; in practice, as much as 9 dB can be accommodated on the transmit side with acceptable voltage swings (200 mV) [3]. The circuit consists of a high-pass path and an all-pass path whose outputs are summed with weights determined by the adaptation control [5]. In order to achieve a compact, low-power design that can provide a maximum of 13 dB of boost at 10 GHz (only 9 dB of boost is used here), the equalizer incorporates a passive boost of 6 dB and only three differential pairs. The linear equalizer draws 5 mW from a 1-V supply.

Figure 8.8.3 depicts partial circuit realization of the DFE. The speed of the critical path is improved through the use of inductive peaking in the gain stages and the latches. A critical trade-off here is that between the power consumption and the size of inductors. The load resistors, transistor widths, and bias currents of the entire DFE can be scaled almost arbitrarily to maintain constant voltage swings while reducing the supply current (so long as the drive for a subsequent circuit, *e.g.*, a DMUX is adequate); however, the inductor values must rise proportionally, leading to longer interconnects between the stages and hence larger parasitic capacitances. This issue is resolved with the aid of stacked inductors consisting of metal-3, metal-6, and metal-9 spirals. For an inductance value of 1 nH, the outer dimension is 35μm.

The class-AB clocking in Fig. 8.8.3 (with no tail current source and the bias current defined by mirrors [6]) both increases the speed and relaxes the voltage headroom constraint. This is particularly important for the stacked multiplexer. To ensure that the lower differential pairs in the MUX do not enter the triode region (and can steer their tail current with reasonable input voltage swings), resistor R_1 shifts down the output common-mode level of L_1 by 150 mV. The DFE draws 35 mW from a 1-V supply.

The receiver has been fabricated in digital 90-nm CMOS technology and tested with a 1-V supply. The 20-Gb/s PRBS data is applied to an 18-in differential trace on an FR4 board and then to the receiver. The demultiplexed outputs are monitored on an oscilloscope and sensed by a bit error rate tester (BERT). The board and cables produce a loss of 24 dB at 10 GHz and more than 40 dB at 20 GHz.

Figure 8.8.4 shows the measured demultiplexed output at 10 Gb/s. Note that the external clock driving the DFE and the DMUX exhibits a peak-to-peak jitter of 7 ps. The output buffer's limited bandwidth also contributes to the eye closure.

Figure 8.8.5 plots the BER as a function of the clock phase. Despite a peak-to-peak jitter of 10 ps in the input PRBS data and 7 ps in the clock, the bathtub curve indicates a horizontal eye opening of about 0.36 UI for the internal signal, suggesting robust sampling and slicing by the DFE and the DMUX. To our knowledge, this is the first 20-Gb/s DFE to compensate a loss of 15 dB with acceptable phase margin and BER.

Figure 8.8.6 shows a comparison of the performance of our equalizer to that of prior art. A figure of merit (FOM) capturing the speed, channel loss, and power consumption can be defined as power/(data rate)/loss (dB). We note that (a) our FOM is the lowest even though our technology is not the fastest and (b) a half-rate CDR designed for our DFE would consume less power than a full-rate CDR necessary for the DFE in [3]. Figure 8.8.7 shows a photo of the die, which has an active area of 300×300μm^2.

Acknowledgements:
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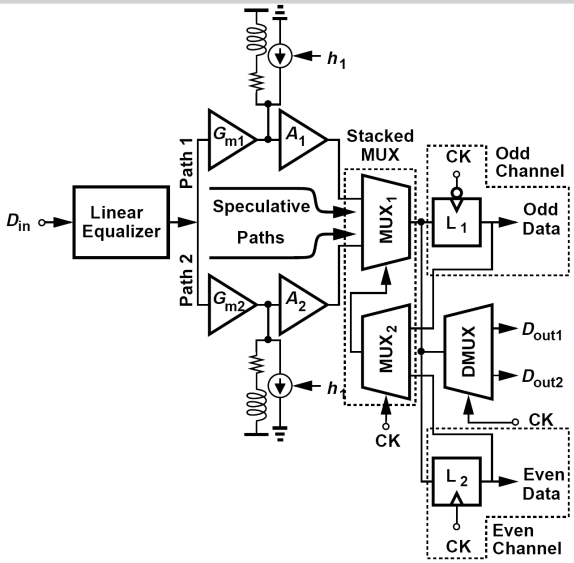

Figure 8.8.1: Proposed equalizer architecture.

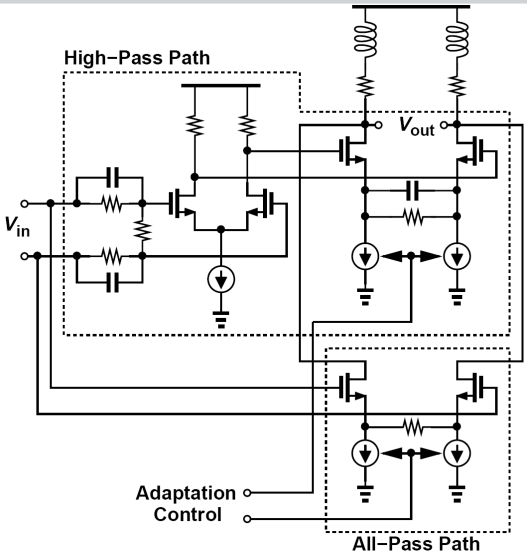

Figure 8.8.2: Linear equalizer circuit.

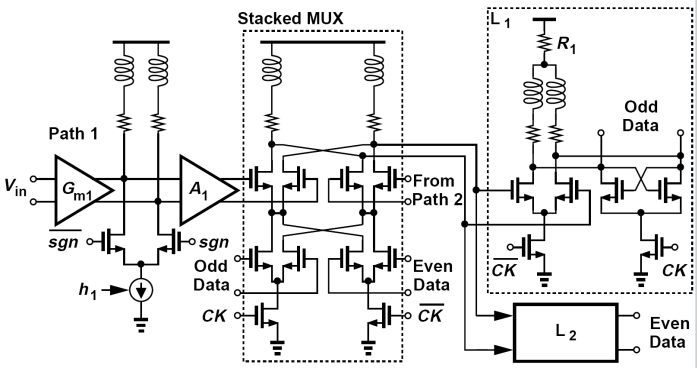

Figure 8.8.3: Partial circuit realization of the DFE.

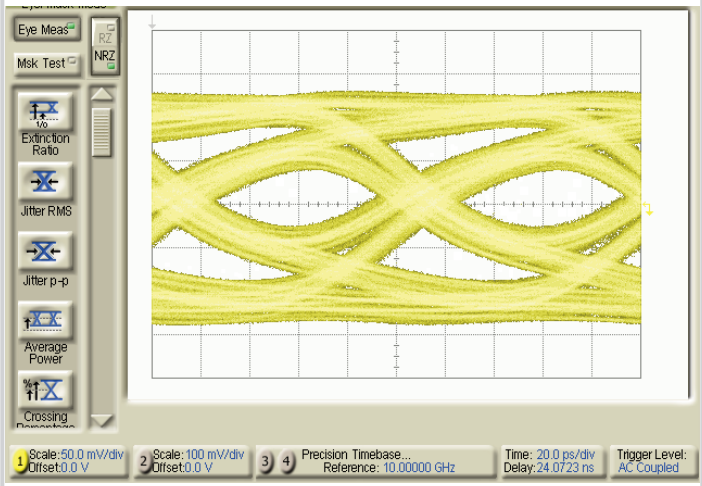

Figure 8.8.4: 10-Gb/s DMUX output (horizontal scale: 20 ps/div, vertical scale: 50 mV/div).

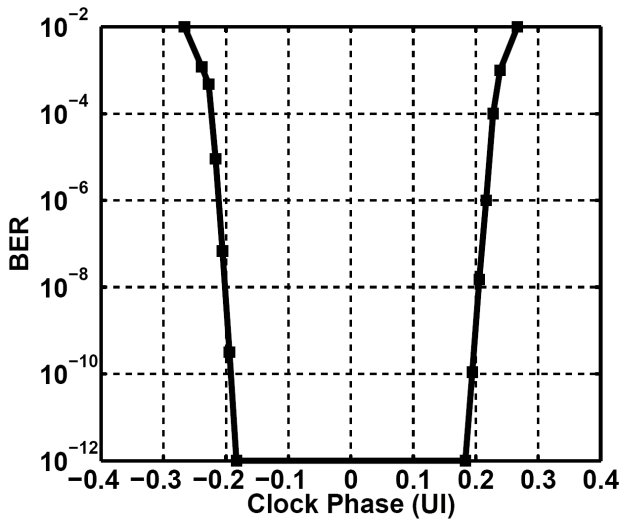

Figure 8.8.5: Bathtub curve for 18-inch FR4 trace at 20 Gb/s with 2^7-1 PRBS data pattern.

Reference	[1]	[2]	[3]	This Work
Data Rate	18 Gb/s	19 Gb/s	21 Gb/s	20 Gb/s
Architecture	4-Tap DFE 1st tap assisted by CDR	1-Tap speculative DFE	Linear equalizer + 1-Tap DFE	Linear equalizer + 1-Tap speculative DFE
Signaling	Duobinary	NRZ	NRZ	NRZ
DFE Clocking	Quarter Rate	Half Rate	Full Rate	Half Rate
Channel Loss @ Nyquist	14 dB	11 dB	11.7 dB*	24 dB
BER / horizontal eye opening	$< 10^{-12}$ / 12% UI	10^{-8} / 9% UI**	$< 10^{-12}$ / N/A	$< 10^{-12}$ / 36% UI
Supply (V)	1.2	1	1.2	1
Power (mW)	100.2***	38	42	40
Area (mm^2)	0.2***	0.02	0.04	0.09
Figure of Merit (pJ/bit/dB)	0.398***	0.182	0.171	0.083
Technology	90-nm CMOS	90-nm CMOS	65-nm CMOS	90-nm CMOS

* Since the TX in [3] includes 9.5 dB of equalization, the channel loss (21.2 dB) is discounted by this amount to allow fair comparison to our receiver.
** 10^{-13} at the center of the eye.
*** CDR included.

Figure 8.8.6: Performance summary and comparison with prior art.

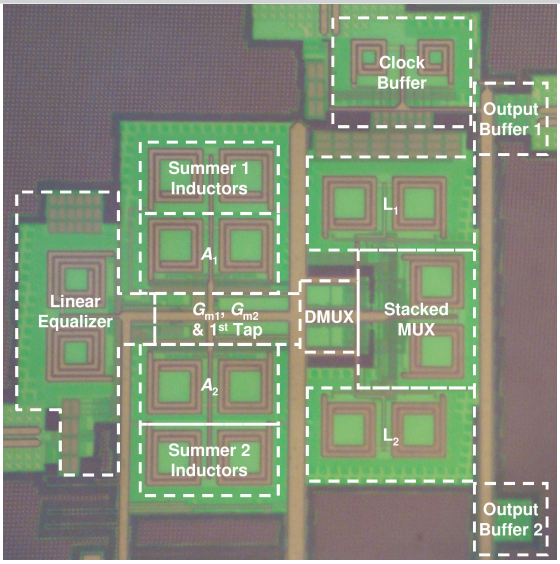

Figure 8.8.7: Equalizer die photo in 90-nm CMOS technology.

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