A 25-Gb/s 5-mW CMOS CDR/Deserializer

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Abstract — A half-rate clock and data recovery circuit and a deserializer employ charge-steering logic to reduce the power consumption. Realized in 65-nm technology, the overall circuit draws 5 mW from a 1-V supply, producing a clock with an rms jitter of 1.5 ps and a jitter tolerance of 0.5 UI$_{pp}$ at 5 MHz.

Broadband transceivers have recently achieved power consumptions as low as 0.98 mW/Gb/s [1] at a data rate of 12.5 Gb/s. With link speeds approaching several tens of gigabits per second, it is desirable to further reduce the power by relaxing the speed-power trade-offs present in broadband circuits. This paper presents a circuit technique and a CDR/deserializer architecture that lower the power consumption by about a factor of 20 with respect to prior 25-Gb/s prototypes.

Charge Steering The concept of "charge steering" as an alterative to current steering was originally introduced in regenerative BiCMOS comparators [2, 3]. In this work, we extend the idea to non-regenerative circuits, exploit the advantages of charge-steering logic (CSL), and architect the CDR and the deserializer so as to circumvent CSL's drawbacks.

Illustrated in Fig. 1 is a general transformation from current steering to charge steering: the tail current and the load resistors are replaced with capacitors. The resulting circuit operates as follows. In the reset phase, C_T is discharged to ground, and C_D's are precharged to V_{DD}. In the evaluation phase, the output nodes are released and C_T is switched into the tail of M_1 and M_2, drawing a differential current from the C_D's until node N rises to about one threshold below the (higher) input level. The CSL circuit can thus amplify and latch the input.

Operating with moderate signal swings and consuming power for only a fraction of the clock cycle, charge steering affords a design style faster than rail-to-rail logic and less power hungry than current steering. However, CSL must deal with two issues that arise from the need for a reset phase. (1) The differential output of the circuit collapses to zero during precharge, producing RZ data. (2) The CSL stage of Fig. 1 cannot be readily used in a master-slave configuration because when the slave enters the evaluation phase, the master begins to lose its output rather than hold it. The CDR/deserializer described here processes RZ data properly by design and eventually converts it to the NRZ format. The second issue is ameliorated through the use of additional circuit techniques presented below.

Architecture In order to relax speed issues and allow the processing of RZ data, the CDR circuit employs a half-rate architecture. The linear half-rate phase detector (PD) in [4] is attractive here as it obviates the need for quadrature clock phases. However, the PD topology must be modified so as to operate properly with RZ waveforms.

Fig. 2 shows the overall CDR/deserializer architecture. The half-rate PD employs six D-latches, L_1-L_6, to generate pulses at X_1 in proportion to the phase error and at X_2 and X_3 in proportion to half of the clock cycle. The latter two are summed with proper weighting and compared against X_1, yielding at the output of the V/I converter an error current that uniquely represents the phase error regardless of the bit pattern. The current flows through the loop filter, and the resulting voltage drives the voltage-controlled oscillator (VCO).

As mentioned above, the charge-steering latch of Fig. 1 cannot be easily cascaded in a master-slave configuration. To resolve this issue, we realize the master as a topology that combines reset and sampling, as originally proposed by [2]. We thus arrive at the implementation shown in Fig. 3 for the cascades L_1-L_3 and L_2-L_4. Here, the master samples the input at nodes P and Q when CK is low and regeneratively amplifies and holds the data when CK is high. The slave therefore robustly senses and stores the result. Note that the master and the slave outputs are in the form of NRZ and RZ data, respectively. The single-ended data swings in this circuit are about 0.45 V$_{pp}$. The RZ waveforms at nodes A and B in Fig. 2 are delayed by half a clock cycle by means of charge-steering latches L_5 and L_6, and the signals at E and F are combined with those at A and B by means of XOR_2 and XOR_3.

The half-rate PD inherently performs 1-to-2 demultiplexing, providing the retimed data at A and B in Fig. 2, but still in RZ form. To perform further demultiplexing, we divide the 12.5-GHz clock by 2 and use the resulting quadrature phases to drive another set of CSL latches. These phases along with the delay of the divider offer ample timing margin for sampling of the data.

In the last stage, the 6.25-Gb/s RZ data is converted to NRZ. A CMOS RS latch can readily accomplish this task but only if rail-to-rail data swings are available. To amplify the RZ levels efficiently, we employ a clocked comparator.

The LC VCO incorporates a symmetric inductor, MOS varactors, and a 2-bit bank of capacitors. To save power, the VCO directly drives all of the latches in Fig. 2, incurring a slight Q degradation as a result of the interconnects' resistance. Nonetheless, the power savings well offset this penalty.

Experimental Results The CDR/deserializer has been fabricated in digital 65-nm CMOS technology (die shown in Fig. 4). The VCO draws 1.4 mA, the PD 2.33 mA, and the divider 1.24 mA. Fig. 5 shows the measured recovered clock spectrum and one of the demulitplexed outputs. Integration of the clock phase noise from 100-Hz to 1-GHz offset yields an rms jitter of 1.52 ps. The BER is less than 10^{-12} with a PRBS of $2^{15}-1$. Fig. 6 plots the measured jitter transfer and jitter tolerance of the system, revealing a bandwidth of about 6 MHz and a tol-

erance of 0.5 UI_{pp} at jitter frequencies as high as 5 MHz. To study the robustness of the circuit, the jitter tolerance is also measured with a 1.1-V supply.

Acknowledgments Research supported by Texas Instruments and Realtek Semiconductor. The authors thank the TSMC University Shuttle Program for chip fabrication.

References

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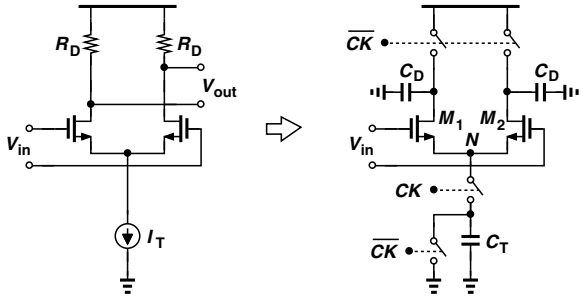


Fig. 1. Transformation from current steering to charge steering.

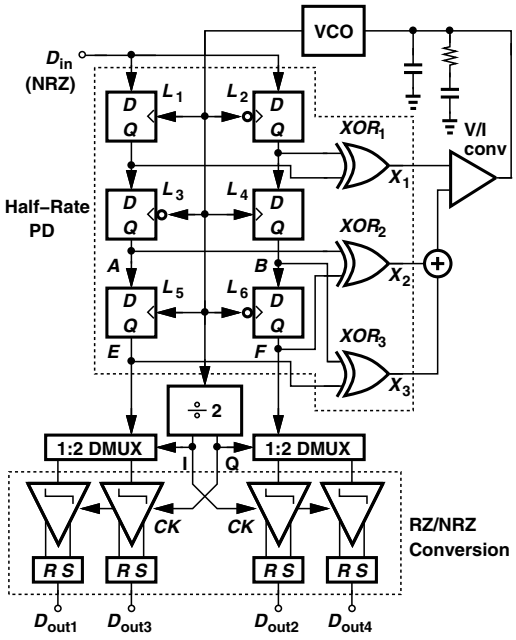


Fig. 2. CDR/deserializer architecture.

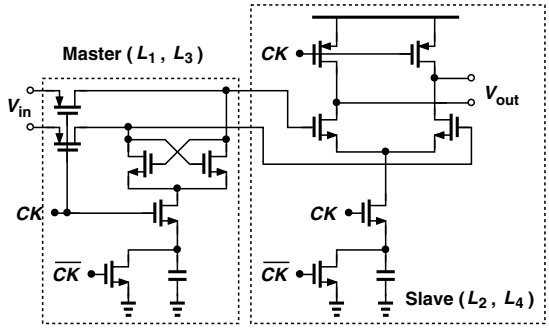


Fig. 3. Front-end master-slave charge-steering latches.

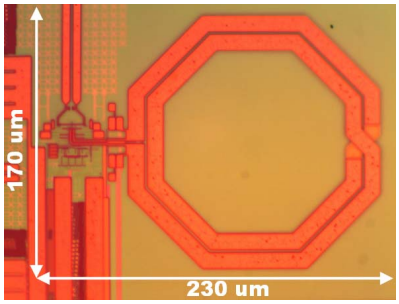
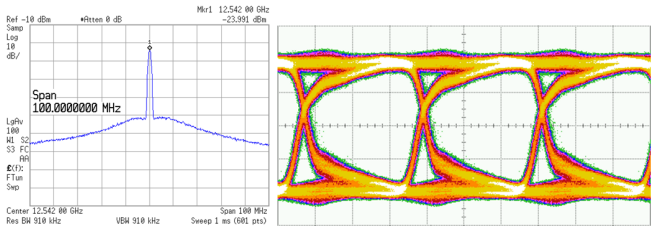


Fig. 4. Die photograph.



(a) (b)

Fig. 5. (a) Recovered clock spectrum, (b) recovered data [vertical scale: 100 mV/div, horizontal scale: 50 ps/div].

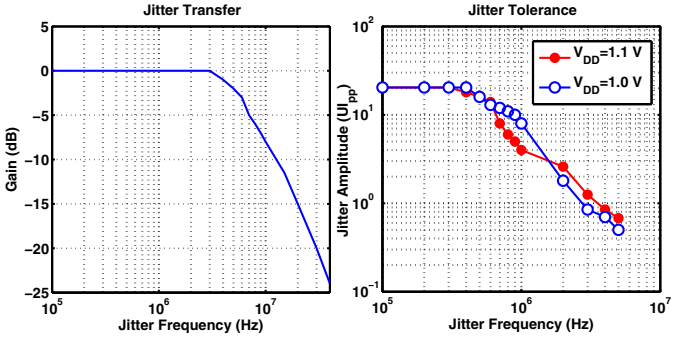


Fig. 6. Jitter transfer and jitter tolerance.

	This Work	[5]	CDR in [6]
Data Rate	25 Gb/s	25 Gb/s	25 Gb/s
DEMUX Ratio	1:4	1: 2	1:1
Power Consumption	4.97 mW	98 mW	99 mW
Technology	65 nm	90 nm	65 nm
Supply Voltage	1 V	1 .1 V	1.2 V

Fig. 7. Performance summary.