Phase Noise Integration Limits for Jitter Estimation in Wireline Transmitters

Kshitiz Tyagi
Mediatek Inc.
Irvine, CA, USA
ktyagi30@ucla.edu

Behzad Razavi
Electrical and Computer Engineering Department
University of California, Los Angeles
Los Angeles, CA, USA
razavi@ee.ucla.edu

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***Abstract*—The performance of high-speed wireline transceivers is significantly affected by the broadband phase noise of their clocking modules, thus requiring accurate noise integration limits for jitter calculation. We show that the correct bounds depend upon the transmitter architecture and the simulation/measurement environment, and present results for various clocking schemes relevant to different multiplexing techniques.**

I. Introduction

The matter of clock jitter in wireline links becomes increasingly critical as data rates continue to scale beyond 100 Gbaud [1], [2]. For link budget calculations dealing with bit error rates less than 10^{-12}, the rms jitter is typically multiplied by 10 to 20 so as to estimate its peak-to-peak value. With symbol periods falling below 10 ps [1], [2], and demanding rms jitter values less than a few hundreds of femtoseconds, accurate *calculation* of jitter also proves critical.

This paper prescribes phase noise (PN) integration limits for common clocking schemes in transmitter (TX) design. Specifically, we show how the PN must be integrated for serializers using a 2-to-1 or a direct 4-to-1 multiplexer (MUX). To this end, we also investigate the integration limits for frequency dividers and multipliers. Moreover, we demonstrate how the limits must change when different calculation methods ("timeaverage" and "jitter" in Cadence's pnoise simulations) are chosen.

II. Problem Statement

Suppose a TX incorporates a 2-to-1 MUX or a direct 4-to-1 MUX [3] to generate its final NRZ data rate [Fig. 1(a)], which is then applied to a driver or a digital-to-analog converter (DAC). Denoting the input data rate by r_b, we remark that the clocks must have a frequency, f_{ck}, equal to r_b in both cases. These clocks themselves originate from a differential oscillator that is followed by a $\div 2$ stage [Fig. 1(b)] [3] or, at very high speeds, followed by a programmable delay line [Fig. 1(c)] [4]. Assuming that the phase-locked oscillator exhibits the PN profile shown in Fig. 1(d), we wish to determine up to what offset frequency it must be integrated to yield the correct rms jitter in D_{out} in these scenarios.

III. Background

Conventional approaches estimate the jitter by integrating the PN up to the Nyquist rate, f_{Nyq} [3], [5]. However, for the cases depicted in Figs. 1(b) and (c) the definition of f_{Nyq}, particularly for the integration limit, is not straightforward. That is, the limit must be chosen based on a justifiable calculation.

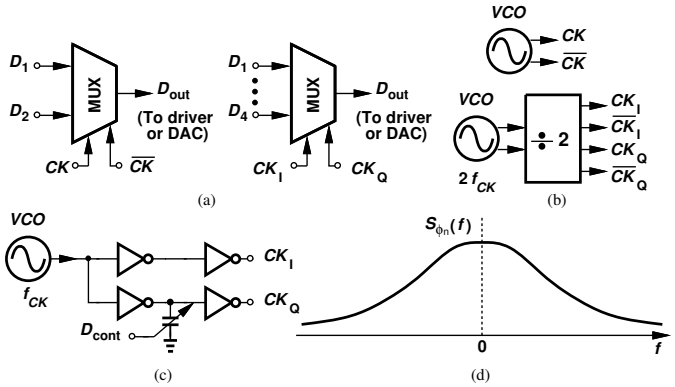

Fig. 1. Clocked circuits in wireline transmitters: (a) 2-to-1 and direct 4-to-1 multiplexers, (b) quadrature phase generation using a divide-by-2 stage, (c) quadrature generation using a programmable delay-line, and (d) typical oscillator phase noise profile in a phase-locked environment.

For a noisy sinusoidal clock, $x(t) = A\cos[2\pi f_{CK}t + \phi_n(t)]$, the work in [6] shows that the rms jitter is simply equal to

$$\sigma_j = \frac{T_{CK}}{2\pi}\sqrt{\int_{-\infty}^{+\infty} S_{\phi_n}(f)df}, \tag{1}$$

where $T_{CK} = 1/f_{CK}$ and $S_{\phi_n}(f)$ denotes the spectrum of $\phi_n(t)$. In practice, simulations or measurements inevitably sample $\phi_n(t)$, causing aliasing and a different spectrum, $S_\theta(f)$. It is proved in [6] that

$$\int_{-\infty}^{+\infty} S_{\phi_n}(f)df = \int_{-f_{CK}}^{+f_{CK}} S_{\theta_n}(f)df. \tag{2}$$

This result holds if the jitter computation takes into account both rising and falling edges. We can interpret this case as sampling at $2f_{CK}$. On the other hand, if only rising (or falling) edges are considered, the limits shrink to $\pm f_{CK}/2$.

IV. Jitter Analysis

With these preliminaries, we can now analyze the jitter at the MUX output in Fig. 1(a) in terms of the oscillator PN. To

ensure that the effect of clock jitter is clearly observed and is distinguishable from that due to intersymbol interference (ISI), we select the MUX inputs so as to create a periodic output at the Nyquist frequency.

A. 2-to-1 MUX

Let us begin with the 2-to-1 MUX shown in Fig. 2(a), where D_{out} simply follows the clock. Since both the rising and falling edges of CK affect D_{out}, the phase noise of CK must be integrated according to Eq. (2), i.e., from $-f_{CK}$ to $+f_{CK}$ [Fig. 2(b)].

If the MUX produces random NRZ data, some of the output transitions observed in Fig. 2(a) are absent. One may then ask whether the same integration limits still apply. We remark that, as seen from Fig. 2(c), the timing errors in the transitions of D_{out} are still equal to the jitter samples of CK, and therefore the rms jitter remains the same irrespective of the data pattern. This is verified by simulations (Section VI).

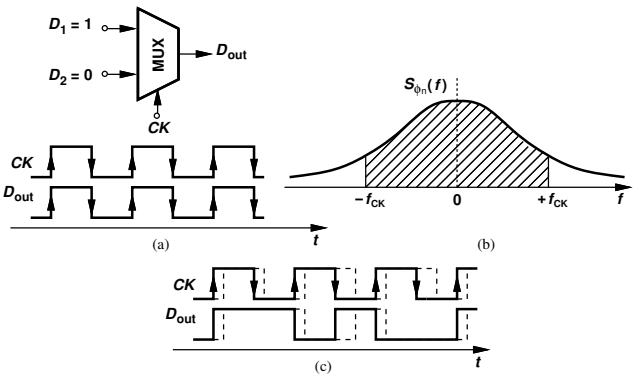

Fig. 2. (a) Phase noise analysis of a 2-to-1 multiplexer using fixed input data patterns, (b) integration limits for the output phase noise, and (c) jitter estimation with random input data patterns.

B. 4-to-1 MUX

Consider the arrangement shown in Fig. 3(a), noting that the odd-numbered edges of D_{out} are inherited from CK_I and the even-numbered edges from CK_Q. In the I/Q separation of Fig. 1(c), we recognize that the oscillator delivers "common" (correlated) phase noise to the two branches while the inverters contribute uncorrelated jitter to CK_I and CK_Q. Let us analyze these two phenomena.

Suppose, in Fig. 1(c), only the oscillator is noisy. As revealed by the waveforms in Fig. 3(b), the successive edges of CK_I and CK_Q fluctuate in tandem, yielding a relatively constant pulsewidth at the MUX output. That is, the oscillator PN primarily causes pulse-position modulation.

As is also evident from the waveform of D_{out} in Fig. 3(a), the MUX is equivalent to a frequency doubler in this arrangement, thus raising the correlated PN by 6 dB. Since the jitter is effectively sampled at $4f_{CK}$, the oscillator PN must be integrated across $\pm 2f_{CK}$.

Next, we assume that only the quadrature paths in Fig. 1(c) are noisy. As illustrated in Fig. 3(c), the MUX output experiences mostly pulsewidth modulation in this case.

We can view D_{out} as the sum of a jitterless waveform, $x_0(t)$, and a series of narrow pulses, $x_1(t)$ [Fig. 3(d)]. We approximate $x_1(t)$ by impulses and recognize that those at t_1, t_3, etc., arise from CK_I and those at t_2, t_4, etc., from CK_Q. That is,

$$x_1(t) \approx \Sigma_k a_k \delta\left(t - k\frac{T_{CK}}{2}\right) + \Sigma_k b_k \delta\left(t - k\frac{T_{CK}}{2} - \frac{T_{CK}}{2}\right), \quad (3)$$

where the first and second summations represent the sampled jitters of CK_I and CK_Q, respectively. Since each is sampled at a rate of $2f_{CK}$, the total jitter in D_{out} is expressed as

$$\sigma_j = \frac{T_{CK}/2}{2\pi}\sqrt{\int_{-f_{CK}}^{+f_{CK}} S_I(f)df + \int_{-f_{CK}}^{+f_{CK}} S_Q(f)df}, \quad (4)$$

where $S_I(f)$ and $S_Q(f)$ denote the phase noise profiles of the CK_I and CK_Q paths, respectively, and are assumed uncorrelated. This result indicates that the output jitter can be calculated as the mean square jitter of CK_I and CK_Q, which is confirmed by simulations (Section VI).

V. Simulation Environment

We wish to perform simulations in Cadence to confirm our theoretical results. For small $\phi_n(t)$,

$$A\cos[2\pi f_{CK}t + \phi_n(t)] \approx A\cos(2\pi f_{CK}t) - A\phi_n(t)\sin(2\pi f_{CK}t). \quad (5)$$

Based on this approximation, we construct the test bench depicted in Fig. 4, where $\phi_n(t)$ is modeled as the noise generated by a resistor (R_1) followed by an ideal low-pass filter, and is combined with ideal sinusoids that drive inverters to generate roughly square-wave outputs (the resistor R_2 is added to model the phase noise floor). The inverters' noise contribution is turned off.

Next, we build benches with appropriate models for clocked circuits of Figs. 1(a) and (b). The generation of quadrature clock phases necessary for some of these operations is done as shown in Fig. 5, which facilitates the modeling of both the correlated (contributed by R_1) and uncorrelated (contributed by R_2 and R_3) phase noise between the two phases.

We select $f_{CK} = 10$ GHz, and the 3-dB frequency of the low-pass filter in Fig. 4 is chosen to be 10 MHz (representing the typical value for wireline links).

VI. Simulation Results and Comparison

In Figs. 4 and 5, we select the resistors such that the theoretical rms jitter is predicted to be 94 fs for CK_I and 109 fs for CK_Q [calculated using Eqs. (1) and (2)]. Next, we perform circuit simulation using Cadence's 'pss' and 'pnoise' routines to obtain the phase noise profile of the clock signal in Fig. 4, and check the rms jitter using different integration limits. All the circuits discussed in this section have been designed and simulated in TSMC's 28-nm CMOS technology.

The pnoise simulation provides two options for the phase noise computation, namely, the 'time-average' and 'jitter'

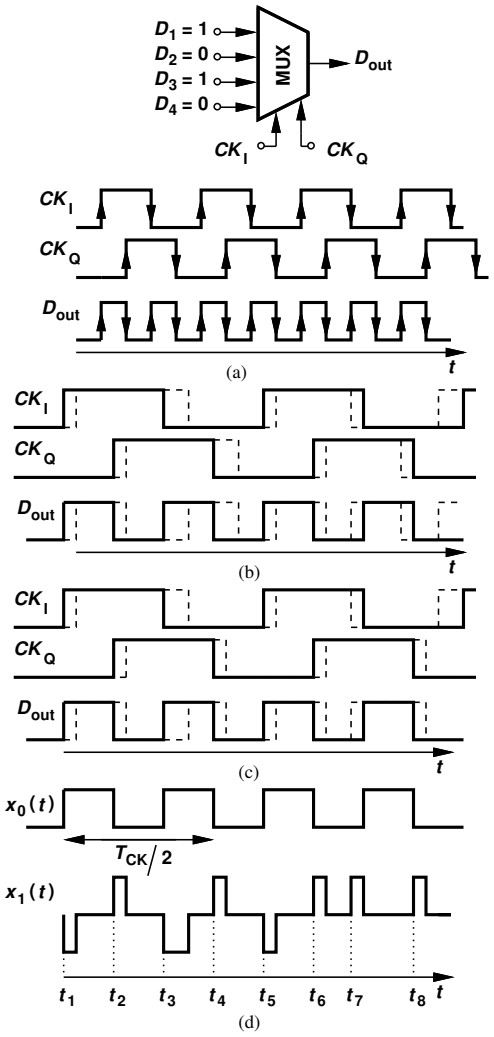

Fig. 3. (a) Phase noise analysis of a direct 4-to-1 MUX using fixed input data patterns, (b) output data jitter assuming only correlated jitter between the quadrature clock phases, (c) output data jitter assuming uncorrelated jitter between the quadrature clock phases, (d) impulse approximation of noisy output for jitter calculation.

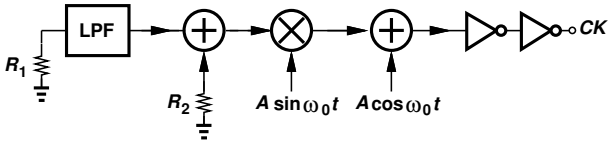

Fig. 4. Model test setup for phase noise simulation.

methods. The former method takes into account both the rising and falling edges of the signal of interest, which represents the 'both edges' scenario discussed in Section II. Thus, we expect the noise integration limits to extend to $\pm f_{CK}$. In contrast, the 'jitter' method involves sampling only either the rising or falling edges at the fundamental frequency specified in the pss options, which can be f_{CK} or a sub-harmonic (the integration limit should be $f_{CK}/2$ or lower).

We first examine the output generated in Fig. 4. Figure 6 shows the simulated phase noise of the 10-GHz clock obtained using the 'timeaverage' method. As shown in Table I, integration up to 10 GHz yields an rms jitter of 94 fs, identical to the predicted value, while integrating up to the Nyquist frequency (5 GHz) predicts only about 71 fs. Table I also covers the results obtained using the 'jitter' method (the pss fundamental frequency is set as 10 GHz); as expected, we find that integrating up to 5 GHz yields the correct jitter in this case.

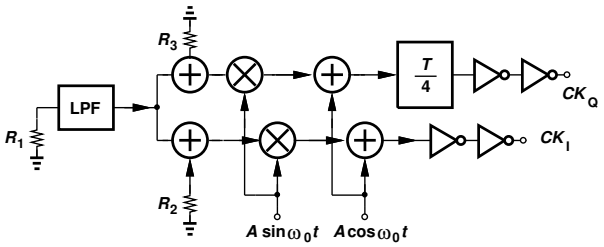

Fig. 5. Generation of quadrature clock phases with extra noise sources for modeling uncorrelated jitter.

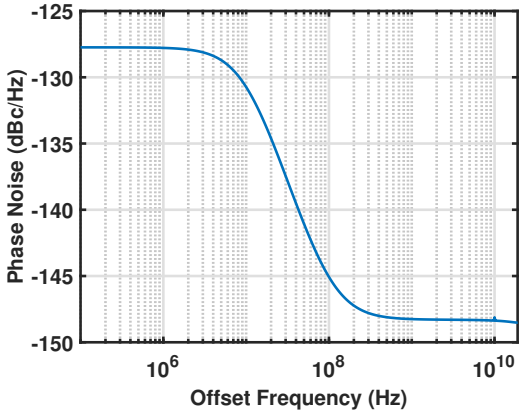

Fig. 6. Simulated phase noise of the 10 GHz clock in Fig. 4.

TABLE I
PHASE NOISE INTEGRATION RESULTS FOR THE 10 GHZ CLOCK

	Range = 1 Hz – 5 GHz	Range = 1 Hz – 10 GHz
Timeaverage method	71 fs	94 fs
Jitter method	95 fs	164 fs

A. 2-to-1 Multiplexer

As discussed in Section IV-A, the output data of the 2-to-1 MUX simply follows the clock when the input pattern is fixed as in Fig. 2(a) [the output frequency is thus 10 GHz]. We implement the MUX using a C^{2}MOS topology (Fig. 7), and use CK_I in Fig. 5 as the selector clock.

From the results in Table II, we see that integration up to 10 GHz yields the expected rms jitter with the 'timeaverage' method, while with the 'jitter' method the correct integration limit is 5 GHz (the pss fundamental is set to 10 GHz).

We also verify our predictions for the case where the MUX output is a random NRZ signal. Since 'pnoise' simulations cannot be performed for an aperiodic signal, we rely on transient noise simulations and extract the rms jitter by processing the edge displacements of the output signal from their ideal position. This simulation reveals the rms jitter to be 98 fs, confirming the accuracy of our jitter calculation model.

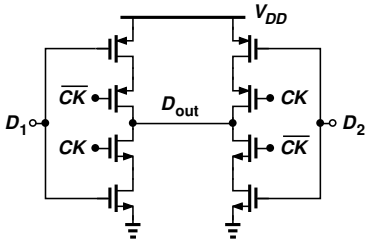

Fig. 7. Implementation of the 2-to-1 MUX using a C^{2}MOS topology.

TABLE II
PHASE NOISE INTEGRATION RESULTS FOR THE 2-TO-1 MULTIPLEXER

	Range = 1 Hz – 5 GHz	Range = 1 Hz – 10 GHz
Timeaverage method	71 fs	94 fs
Jitter method	93 fs	161 fs

B. 4-to-1 Multiplexer

To simulate the output data jitter of the 4-to-1 MUX, we set the data inputs as in Fig. 3(a). The output signal is equivalent to an XOR/doubler operation on CK_I and CK_Q (resulting in an output frequency equal to 20 GHz), and follows the waveforms of Fig. 3(a) - the odd edges follow CK_I, and the even edges follow CK_Q.

Since the 'timeaverage' method considers all the output edges, the integrated output jitter is theoretically expected to be the mean square of the rms jitter values of CK_I and CK_Q, i.e., 101.8 fs [Eq. (4)]. This is confirmed by the simulation results in Table III, which show that integration up to 20 GHz ($2f_{CK}$) yields 105 fs.

When using the 'jitter' method, since the fundamental frequency in the circuit must still be set to 10 GHz, integration up to 5 GHz yields the correct results (Table III) [integrating up to 10 GHz predicts the jitter to be 160 fs, which is nearly 70% larger].

Further, differences are observed depending on whether the rising or falling transitions of the output are considered for the jitter calculation. As explained by the timing diagrams in Fig. 3(a), the rising edges of the output are defined solely by CK_I, and thus those edge jitter samples are the same as the jitter samples of CK_I, while the falling edges follow CK_Q and exhibit a higher rms jitter since the phase noise in the CK_Q path was chosen deliberately higher. Both the CK_I and CK_Q timing jitter matches the theoretical estimations from Eqs. (1) and (2).

TABLE III
PHASE NOISE INTEGRATION RESULTS FOR THE DIRECT 4-TO-1 MULTIPLEXER

	Range = 1 Hz – 5 GHz	Range = 1 Hz – 10 GHz	Range = 1 Hz – 20 GHz
Timeaverage method	70 fs	86 fs	105 fs
Jitter method: rising edge	94 fs	160 fs	267 fs
Jitter method: falling edge	109 fs	178 fs	289 fs

C. Divide-by-2 Stage

Next, we check the case of the frequency divider [Fig. 1(b)], which is based on a C^{2}MOS topology. Using the 'timeaverage' routine, we expect that the output phase noise must be integrated up to the divided frequency, i.e: 5 GHz. Indeed, as shown in Table IV, integration up to 5 GHz reveals 93 fs jitter, while integration up to 2.5 GHz only yields about 70 fs. While using the 'jitter' method, the fundamental frequency is set as 5 GHz, and thus integration up to 2.5 GHz yields accurate results.

TABLE IV
PHASE NOISE INTEGRATION RESULTS FOR THE DIVIDE-BY-2 CIRCUIT

	Range = 1 Hz – 2.5 GHz	Range = 1 Hz – 5 GHz
Timeaverage method	70 fs	93 fs
Jitter method	93 fs	133 fs

VII. CONCLUSION

This work establishes phase noise integration limits for accurate jitter estimation in various circuits relevant to wireline transmitters, such as frequency dividers, and both 2-to-1 and direct 4-to-1 multiplexers. It is shown that the integration bounds generally depart from the Nyquist frequency of the clocked signal, and depend on the multiplexing scheme and the simulation/measurement environment.

ACKNOWLEDGMENT

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