A 2.6-GHz/5.2-GHz Frequency Synthesizer in 0.4-μm CMOS Technology

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Abstract

This paper describes the design of a CMOS frequency synthesizer targeting wireless local area network applications in the 5-GHz range. Based on an integer-N architecture, the synthesizer produces a 5.2-GHz output as well as the quadrature phases of a 2.6-GHz carrier. Fabricated in a 0.4-μm digital CMOS technology, the circuit provides a channel spacing of 23 MHz at 5.2 GHz while exhibiting a phase noise of -115 dBc/Hz at 2.6 GHz and -100 dBc/Hz at 5.2 GHz at 10-MHz offset. The reference sidebands are at -50 dBc at 2.6 GHz and the power dissipation from a 2.6-V supply is 47 mW.

I. Introduction

Wireless local area networks (WLANs) provide great flexibility in the communications infrastructure of environments such as hospitals, factories, and large office buildings. While WLAN standards in the 2.4-GHz range have recently emerged in the market, the data rates supported by such systems are limited to a few megabits per second. By contrast, a number of standards have been defined in the 5-GHz range that allow data rates greater than 20 Mb/s, offering attractive solutions for real-time imaging, multimedia, and high-speed video applications. One of these standards is High Performance Radio LAN (HIPERLAN) [1].

This paper presents the design of a frequency synthesizer for HIPERLAN transceivers. Employing an integer-N architecture, the circuit generates a 5.2-GHz output for the transmit path and the quadrature phases of a 2.6-GHz carrier for the receive path. Realized in a 0.4-μm CMOS technology, the synthesizer provides a channel spacing of 23 MHz while dissipating 47 mW from a 2.6-V supply.

Section II of the paper describes the synthesizer environment. Sections III and IV introduce the architecture and building blocks, and Section V summarizes preliminary experimental results.

II. Synthesizer Environment

HIPERLAN operates with Gaussian minimum shift keying (GMSK) using a channel spacing of 23 MHz and a total of 5 channels. The design of a 5-GHz HIPERLAN synthesizer in a 0.4-μm digital CMOS technology entails many difficulties at both the architecture and the circuit level. The high center frequency of the voltage-controlled oscillator (VCO), the poor quality of inductors due to skin effect and substrate loss, the limited tuning range, the nonlinearity of the VCO input/output characteristic, the high speed required of the dual-modulus divider, the mismatches in the charge pump, and the implementation of the loop filter are among the issues encountered in this design.

In order to relax some of the synthesizer requirements, the transceiver and the synthesizer have been designed concurrently. Fig. 1 shows the transceiver architecture [2] and its interface with the synthesizer. The receive path consists of two downconversion stages, each using a local oscillator (LO) frequency of 2.6 GHz, and the transmit path modulates the VCO by the Gaussian-filtered baseband data, producing a GMSK output. For transmission, the VCO is first placed in the synthesizer loop so as to define its center frequency, and it is subsequently operated open-loop while sensing the shaped data pulses.

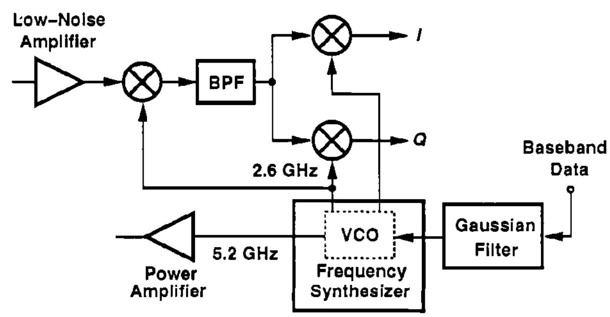

Fig. 1. Synthesizer Environment.

An important feature of this architecture is that the synthesizer is shared between the transmitter and the receiver, reducing the system complexity substantially. This is possible because HIPERLAN incorporates time-division duplexing (TDD). Also, the transceiver requires the generation of the quadrature phases of the 2.6-GHz carrier rather than the 5.2-GHz carrier, a task readily accomplished by the synthesizer itself.

III. Synthesizer Architecture

In order to alleviate the difficulties in the design of a high-speed frequency divider, the synthesizer employs an integer-N

[1]This work was supported by Rockwell, Lucent, the California MICRO program, and a Hewlett-Packard equipment grant.

loop sensing the 2.6-GHz output of the VCO. As shown in Fig. 2, a ÷218-224 controlled by the digital channel-select

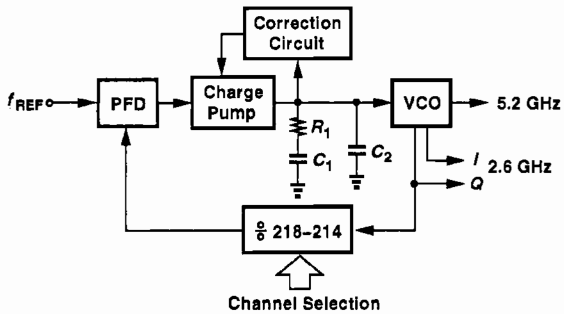

Fig. 2. Synthesizer architecture.

input generates frequency steps of f_{REF} = 12.5 MHz in the 2.6-GHz band and 23 MHz in the 5.2 GHz band. The divider output is compared with f_{REF} by means of a phase/frequency detector (PFD), and the result is applied to a charge pump and a loop filter.

A critical issue in the architecture of Fig. 2 is the nonlinearity of the VCO characteristic, i.e., the variation of the VCO gain K_{VCO} with the control voltage V_{cont}. This effect manifests itself in both the settling behavior and the magnitude of the reference sidebands. The problem is partially resolved through the use of a correction circuit that adjusts the charge pump current according to the value of V_{cont} [3].

An interesting property of the architecture of Fig. 2 is the position of the reference spurs with respect to the main carrier. Since the reference frequency is half the channel spacing, such spurs fall at the *edge* of the channel rather than at the center of the adjacent channel for both 2.6-GHz and 5.2-GHz outputs (Fig. 3). Since the interference energy received by the antenna

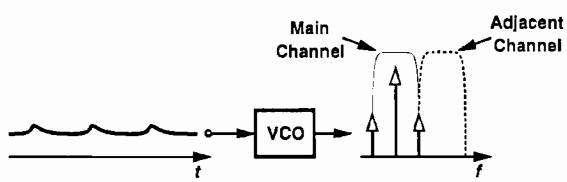

Fig. 3. Position of reference sidebands.

is small at the edge, the maximum allowable magnitude of the spurs can be quite higher.

IV. Building Blocks

A. VCO

The voltage-controlled oscillator is described in [2] and reproduced in Fig. 4 for completeness. The core of the circuit consists of two coupled oscillators generating quadrature outputs [4] at 2.6 GHz. Nodes A and B provide the 5.2-GHz signal in differential form. With proper choice of device dimensions and bias currents, a voltage swing of approximately 0.5 V is obtained at these nodes.

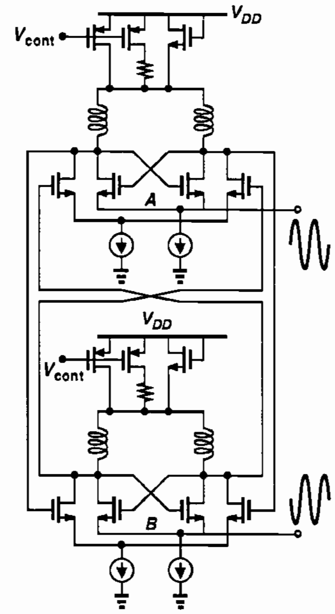

Fig. 4. VCO implementation.

B. Frequency Divider

The design of a 2.6-GHz divider with a reasonable power dissipation in 0.4-μm CMOS technology is quite difficult. A number of circuit techniques are introduced in this design to improve the speed of a pulse-swallow divider topology.

Fig. 5(a) depicts a conventional implementation providing a divide ratio of $NP + S$. A drawback of this configuration is

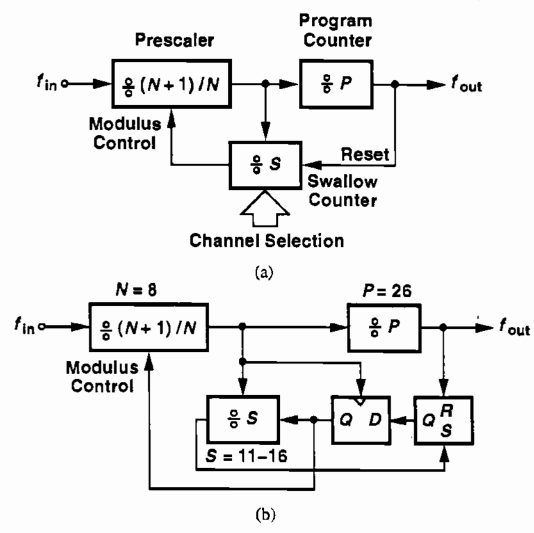

Fig. 5. (a) Conventional pulse-swallow divider, (b) divider used in this work.

the long delay through the asynchronous swallow counter in the path controlling the modulus of the prescaler. Even with proper choice of clock edges, the maximum propagation delay of the swallow counter must not exceed 1.9 ns in this design, requiring a high power dissipation. For this reason, the divider is pipelined as shown in Fig. 5(b), allowing a total delay of

3.1 ns. With this modification, the divide ratio is equal to $NP + S + 1$.

The design of the 8/9 prescaler for 2.6-GHz operation presents a great challenge. Shown in Fig. 6, the prescaler consists of a synchronous $\div 2/3$ circuit and two asynchronous $\div 2$ circuits.

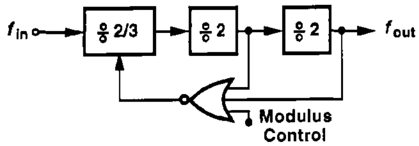

Fig. 6. 8/9 prescaler.

In a conventional $\div 2/3$ realization [Fig. 7(a)], one of the flipflops experiences a fanout of 1 and the other a fanout of 3.

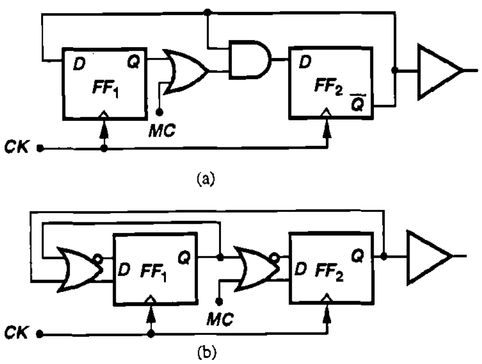

Fig. 7. (a) Conventional $\div 2/3$ circuit, (b) $\div 2/3$ topology used in this work.

The $\div 2/3$ circuit used here [Fig. 7(b)] is modified such that each flipflop has a fanout of 2. Simulations indicate that this technique increases the maximum operating speed by approximately 40%.

The prescaler utilizes differential current steering logic. Fig. 8 depicts the NOR/flipflop used in the $\div 2/3$ circuit as a representative implementation.

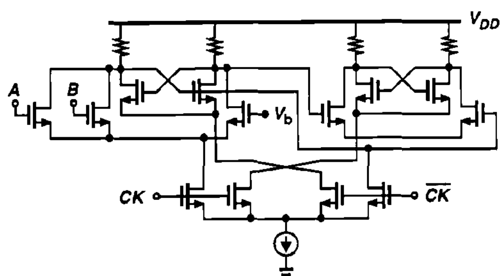

Fig. 8. Implementation of NOR/flipflop circuit in prescaler.

The output of the prescaler drives a differential to single-ended converter, producing rail-to-rail swings for the remainder of the divider.

C. Charge Pump, Loop Filter, and Correction Circuit

The charge pump is based on the topology in [5] and shown in Fig. 9 along with the loop filter. In addition to settling and spur issues, the filter also impacts the VCO phase noise because the thermal noise of R_1 is typically quite large. With the aid of narrowband frequency modulation approximations, it can be readily shown that the noise of R_1 creates a relative phase noise per unit bandwidth at an offset frequency $\Delta\omega$ equal to

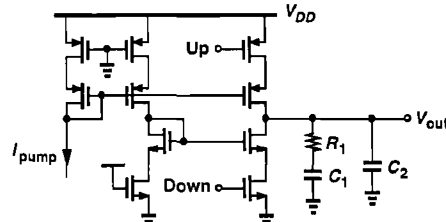

Fig. 9. Charge pump and loop filter.

$$\frac{P_n}{P_{carrier}} = \left(\frac{C_1}{C_1 + C_2}\right)^2 \frac{4kTR_1}{1 + \left(R_1 \frac{C_1 C_2}{C_1 + C_2} \Delta\omega\right)^2} \left(\frac{K_{VCO}}{2\Delta\omega}\right)^2. \tag{1}$$

To achieve a reasonable settling behavior, we have $C_1 = 5$ pF, $C_2 = 1$ pF, and $R_1 = 86\,\text{k}\Omega$. Thus, with $K_{VCO,max} = 2\pi \times 1$ Grad/s/V, we obtain a relative phase noise of -141 dBc/Hz at 20-MHz offset, a negligible amount with respect to the VCO intrinsic noise. While it is desirable to reduce the value of R_1, the required increase in C_1 and C_2 leads to severe area penalty. This is because the near rail-to-rail voltage range at the output of the charge pump prohibits implementing these capacitors with MOSFETs, necessitating the use of low-density metal sandwiches.

The correction circuit adjusts the charge pump current, I_{pump}, so as to compensate for the variation of K_{VCO}. Shown in Fig. 10(a) are the VCO characteristics, suggesting that I_{pump} must vary as depicted in Fig. 10(b). Rather than use piecewise linearization [3], this design incorporates an analog folding technique. Illustrated in Fig. 11, the correction circuit consists of two imbalanced differential pairs whose outputs are added with opposite polarity in the current domain. Thus, as V_{cont} goes from zero to V_{DD}, I_{out} begins from I_{SS}, drops to a low value for $V_{cont} \approx V_b$, and returns to I_{SS}. The asymme-

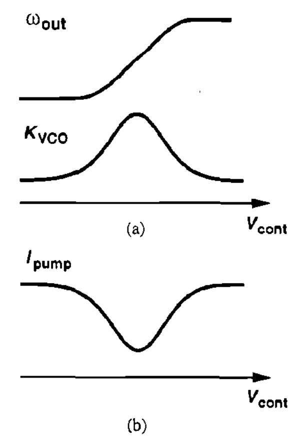

Fig. 10. (a) VCO characteristics, (b) required behavior of charge pump current.

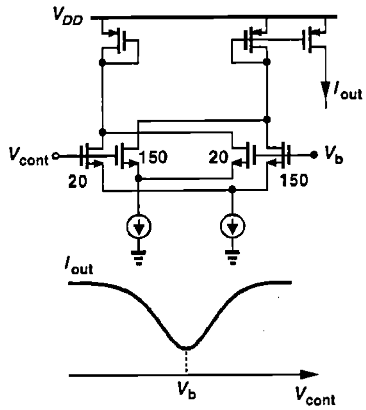

Fig. 11. Correction circuit.

try in each differential pair is chosen to establish the required high-to-low ratio for I_{out}.

V. EXPERIMENTAL RESULTS

The frequency synthesizer has been fabricated in a 0.4-μm digital CMOS technology. All of the inductors and capacitors are included on the chip. Fig. 12 is a photograph of the die, which measures 1.75 mm $\times$ 1.15 mm. The circuit has been

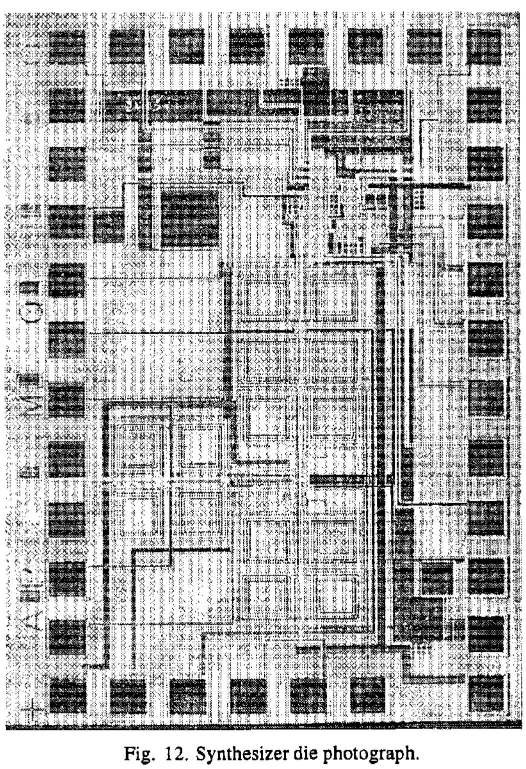

Fig. 12. Synthesizer die photograph.

tested with a 2.6-V supply. The preliminary results reported here were obtained one day before the submission of the paper.

Figs. 13(a) and (b) depict the measured output spectra in the locked condition. The phase noise at 10-MHz offset is -115 dBc/Hz at 2.6 GHz and -100 dBc/Hz at 5.2 GHz. A signifcant

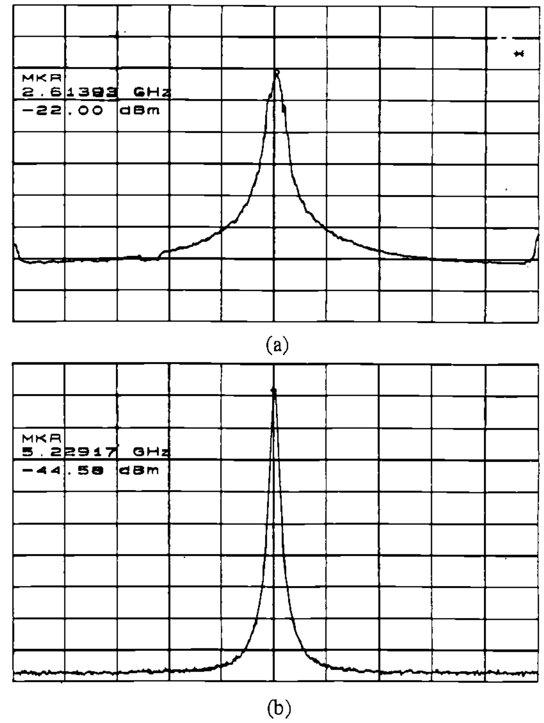

Fig. 13. Output spectra at (a) 2.6 GHz (horiz. scale: 2.5 MHz/div., vert. scale: 10 dB/div.), (b) 5.2 GHz (horiz. scale: 5 MHz/div., vert. scale: 5 dB/div.). (Resolution BW: 300 kHz)

part of the phase noise at 5.2 GHz is attributed to the loss of the output buffer. The reference sidebands at 2.6 GHz are 50 dB below the carrier. The loss of the output buffer has buried the sidebands around the 5.2-GHz output under the noise floor. The circuit, excluding the output buffers, dissipates 47 mW, of which 30 mW is drained by the VCO and 17 mW by the divider, the charge pump, and the correction circuit.

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