

# A 2.4-GHz 6.4-mW Fractional-N Inductorless RF Synthesizer

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**Abstract** — A ring-oscillator-based cascaded synthesizer architecture incorporates a digital synchronous delay line and an analog noise trap to suppress the quantization noise of the  $\Sigma\Delta$  modulator. Realized in 45-nm digital CMOS technology, the synthesizer exhibits an in-band phase noise of -109 dBc/Hz and an integrated jitter of 1.68 ps<sub>rms</sub>.

It has been demonstrated that a wideband type-I integer-N phase-locked loop (PLL) architecture can achieve a bandwidth close to  $f_{REF}/2$ , thereby suppressing the phase noise of ring oscillators to levels commensurate with 2.4-GHz wireless standards while drawing moderate power [1]. The useful attributes of ring oscillators, such as a wide tuning range and more compact design, motivate us to extend this concept to fractional-N operation as well. However, we face the basic trade-off between the loop bandwidth and the  $\Sigma\Delta$  modulator quantization noise contribution, an issue that has severely limited the former even in the presence of various noise cancellation techniques. For example, the design in [2] provides a bandwidth of about  $f_{REF}/13$ , which does not adequately reduce the oscillator phase noise if  $f_{REF}$  is around 20 MHz.

**Synthesizer Design** Rather than deal with fractional-N issues such as charge pump nonlinearity, DAC gain error and nonlinearity, etc., one can contemplate inserting a noise filter immediately after the feedback divider [Fig. 1(a)]. If the filter sufficiently attenuates the phase noise peaking below and above  $f_{REF}$ , then the loop bandwidth can be widened. The design therefore becomes nearly as simple as that of an integer-N synthesizer.

The noise filter must (a) exhibit a band-pass response precisely centered at  $f_{REF}$ , with a steep roll-off before reaching the peaks of phase noise, (b) contribute negligible noise and, (c) be linear enough to avoid folding the quantization noise peaks. These issues discourage the use of an analog implementation. More fundamentally, we must also recognize that a narrowband noise filter can degrade the loop stability, thus posing its own limitations on the synthesizer bandwidth.

We propose a digital solution that resolves all of the above issues. Illustrated in Fig. 1(b), the idea is to delay the divider output phase,  $\phi_1$ , to obtain  $\phi_2$  and then add  $\phi_2$  to  $\phi_1$ . If the delay is long enough to invert the phase noise components of interest, then  $\phi_1 + \phi_2$  contains less noise. More accurately, the filter transfer function is equal to  $1 + \exp(-T_D s)$ , where  $T_D$  denotes the delay, exhibiting notches at  $f = (2n + 1)/(2T_D)$  for  $n = 0, 1, \dots$ . Since these operations occur in the phase domain, the voltage-domain transfer function is centered at  $f_{REF}$ , as required.

Two aspects of the proposed solution merit remarks. First, while asynchronous delay lines suffer from trade-offs between

the delay value, phase noise, and power consumption, their synchronous counterparts do to a much lesser extent. Our delay line employs 24 static flipflops that are clocked by the VCO output, generating negligible phase noise and drawing 300  $\mu$ W at 2.4 GHz. Second, unlike the simple noise filter shown in the top part of Fig. 1, the proposed technique does not affect the loop stability. This can be seen by assuming a phase step at the VCO output and noting that this step directly reaches the end of the delay line by clocking the last flipflop. In other words, only the quantization noise—and not the desired signal—experiences the notch.

The delay-line-based filter entails two issues. First, with only 24 flipflops, the first notch appears at 50 MHz, failing to suppress the quantization noise if  $f_{REF} \approx 20$  MHz. Second, the filter frequency response periodically rises to a peak value of 2 between the notches, causing noise peaking at the synthesizer output. Shown in Fig. 2, the overall synthesizer architecture resolves both issues. An integer-N PLL based on the work in [1] multiplies  $f_{REF}$  by about a factor of 50, delivering a 1-GHz signal to the fractional-N loop. Thus, the latter can be designed for a wide loop bandwidth ( $\approx 12$  MHz), with its  $\Sigma\Delta$  modulator running at 1 GHz and producing phase noise peaks at 500-MHz offset. The notches created by the delay-line-based filter therefore suppress the noise as it begins to rise with frequency. (We should point out that the design in [3] also employs cascaded PLLs but with an LC-VCO and a fractional-N loop bandwidth of about 1/800 times its input frequency.)

In order to suppress the quantization noise peaking between the first two notches (at 50 MHz and 150 MHz), we introduce on the VCO control line in Fig. 2 a “noise trap” circuit. The trap employs a  $G_m$ -based integrator that is loaded by a gyrator. This combination presents an imaginary zero—and hence a notch—at 100 MHz, and a real pole at 120 MHz, ensuring that  $|Z_T|$  remains low beyond this frequency. Since  $V_{cont}$  assumes a wide range, the integrator consists of complementary differential pairs,  $G_{m1}$  and  $G_{m2}$ . The bias voltage,  $V_b$ , is generated using a scaled, heavily-filtered replica of the main path.

Both PLLs in Fig. 2 employ three-stage ring oscillators with varactor tuning for continuous control and capacitor banks for discrete control [1]. The 1-GHz and 2.4-GHz VCOs respectively consume 2.7 mW and 2.25 mW and have a phase noise of -130 dBc/Hz and -121 dBc/Hz at 10-MHz offset.

**Experimental Results** The cascaded synthesizer of Fig. 2 has been fabricated in TSMC’s 45-nm digital CMOS technology. Shown in Fig. 3(a) is the die photograph, with an active area of about 300  $\mu$ m  $\times$  100  $\mu$ m. Plotted in Figure 3(b) are the measured output spectra before and after the delay-line-based

filter and the noise trap are turned on. No injection-pulling has been observed between the two PLLs.

Figure 4 plots the measured output phase noise profile. The in-band plateau is at  $-109$  dBc/Hz and the integrated jitter from 10 kHz to 50 MHz is equal to  $1.68$  ps<sub>rms</sub>. Plotted in Fig. 5 is the magnitude of the fractional spurs as a function of the fractional frequency offset. Note that the spur levels satisfy both IEEE 802.11 a/g and Bluetooth blocking requirements. Table I summarizes the performance of our prototype and compares it to state-of-the-art synthesizers in the range of 1.9 GHz to 2.4 GHz. Compared to the ring-based fractional-N design in [5], the proposed architecture achieves 11 dB lower phase noise with 30% less power consumption.

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## References

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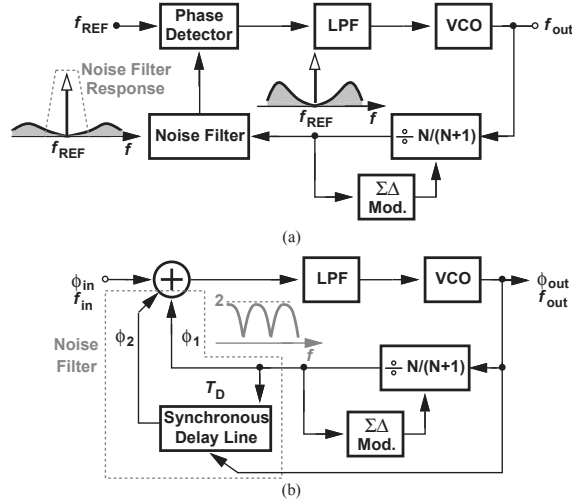


Fig. 1. (a) Conceptual synthesizer with noise filter, and (b) filter implementation using a delay line.

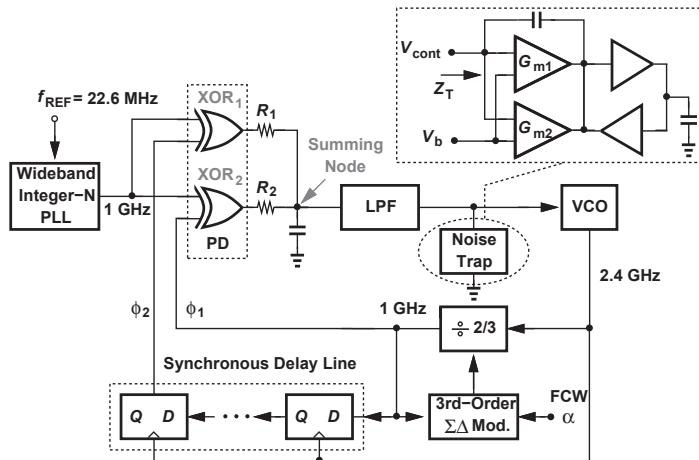


Fig. 2. Proposed synthesizer architecture.

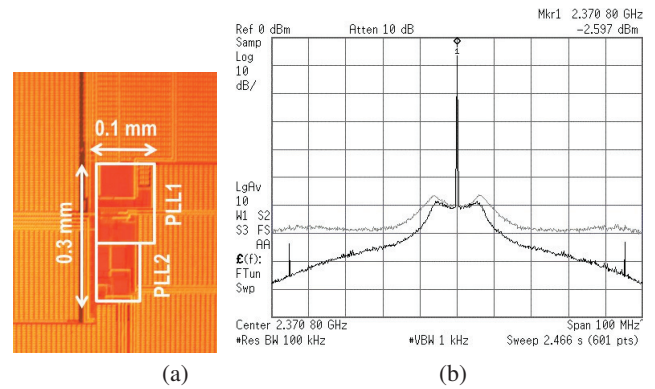


Fig. 3. (a) Die photograph, and (b) measured output spectra before (grey) and after (black) delay-line-based filter and noise trap are on.

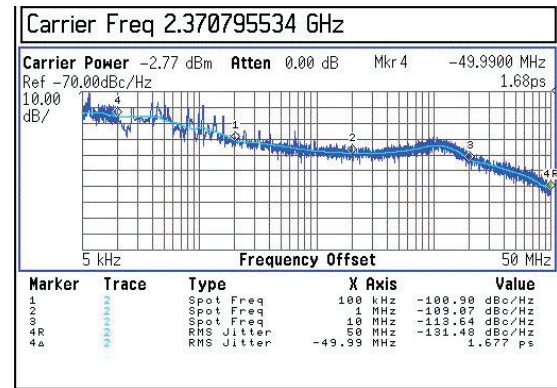


Fig. 4. Measured phase noise.

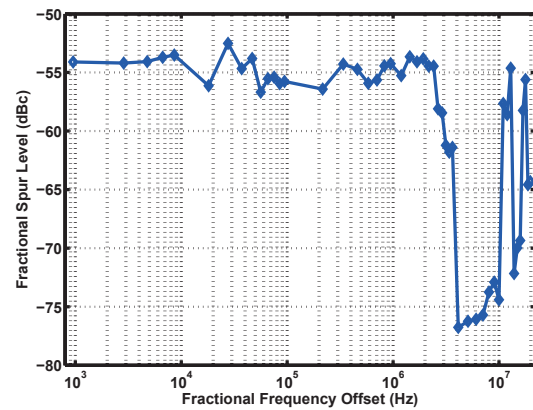


Fig. 5. Measured fractional spurs.

TABLE I. Performance summary.

	ISSCC'13	ISSCC'14	ISSCC'15	This Work
Oscillator Topology	[2]	[4]	[5]	Ring
Reference Freq. (MHz)	26	48	26	22.6
Frequency Range (GHz)	1.87 ~ 1.98	2.2 ~ 2.4	2	2.3 ~ 2.6
Phase Noise @ 1MHz offset (dBc/Hz)	-98	-117	-98	-109
RMS Jitter (ps)	3.4	0.3	2.36	1.68
Integ. range (MHz)	(0.004-2)	(0.01-30)	(0.001-40)	(0.01-50)
In-band Frac. Spur (dBc)	-50	-53	-70	-52.5
Ref. Spur (dBc)	-67	-55	-87	-70
Power (mW)	10	17.3	9.1	6.4
Area (mm <sup>2</sup> )	0.047	0.75	0.046	0.03
Tech. (nm)	40	180	40	45
FoM <sub>1</sub> (dB)	-219.4	-238	-223	-227.4
FoM <sub>2</sub> (dB)	153.9	171.9	154.4	168.4

$$FoM_1 = 10 \log_{10} \left[ \left( \frac{\text{Jitter}}{1 \text{ s}} \right)^2 \left( \frac{\text{Power}}{1 \text{ mW}} \right) \right] \quad FoM_2 = 10 \log_{10} \left[ \left( \frac{f_{\text{osc}}}{\Delta f} \right)^2 \left( \frac{1 \text{ mW}}{\text{Power}} \right) \right] - \text{Phase Noise (dBc/Hz)}$$