21.6 A 60GHz Direct-Conversion CMOS Receiver

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The 7GHz unlicensed band around 60GHz provides the possibility of gigabit-per-second wireless communications. In addition to satisfying speed-intensive applications, such high data rates can also *reduce* the energy dissipated per bit because the power consumption of RF transceivers has historically increased sublinearly with the data rate. Moreover, the millimeter wavelength permits the integration of multiple antennas on one chip, calling for multiple transceivers and hence high levels of integration.

The design of a 60GHz direct-conversion receiver in 0.13μm CMOS technology for short-range communications is described. Figure 21.6.1 shows the receiver architecture. The circuit consists of a low-noise amplifier (LNA), quadrature mixers, and baseband amplifiers. A single-ended to differential (S/D) converter for one of the local oscillator (LO) phases is also included to facilitate testing. Since the f_T of NMOS devices having a channel length of 0.13μm is around 80GHz, a number of circuit and device techniques are introduced that boost the performance of transistors at 60GHz.

The use of resonance can markedly improve the performance of transistors. In principle, if C_{GS} resonates with an inductor having a quality factor of Q_1, then the f_T rises by the same factor. Unfortunately, the design of spiral inductors for operation at 60GHz demands a detailed knowledge of the substrate doping profiles as eddy currents both limit the Q and alter the inductance value at these frequencies. Alternatively, on-chip microstrip lines realized by metal layers can serve as inductors, with their properties negligibly affected by the substrate and accurately predicted by field simulators. Nevertheless, the necessary length of such lines (e.g., 300μm) leads to disproportionately tall layouts, making the routing of signal and power lines difficult.

This design incorporates a "folded" microstrip geometry to simplify the receiver layout. Shown in Fig. 21.6.2, the structure is realized as a metal 8 signal line over a metal 1 ground plane. Carrying currents in opposite directions, the two legs must bear a minimum spacing S_{min}, so as to experience negligible magnetic coupling. For example, if W=6μm, the Q of the line approaches a maximum (≈12 at 60GHz) for S≥15μm. Greater values of S do not degrade the performance significantly but make the layout of the overall receiver more difficult. Approximating the folded microstrip by the lumped tank shown in Fig. 21.6.2, we note that the dimensions of the structure must be chosen to maximize R_p and minimize C_p at 60GHz while maintaining an L_p small enough to resonate with transistor capacitances. For example, if W=6μm and each leg is 150μm long, then R_p =720Ω, C_p =9.2fF, and L_p = 155pH, leaving 45fF of capacitance to be absorbed for resonance at 60GHz. Narrower lines exhibit a slightly smaller capacitance but also a lower value for R_p. Thus, W=6μm is used in this design.

At frequencies well below the f_T of transistors, cascode topologies provide a low noise figure, good input matching, and a high reverse isolation. At higher frequencies, on the other hand, the pole at the cascode node (typically on the order of $f_T/2$) shunts a considerable portion of the RF current to ground, thereby lowering the gain and raising the noise contributed by the cascode device. Furthermore, the very small degeneration and gate series inductances required for input matching make the circuit sensitive to package parasitics. These observations suggest that the LNA must contain a single transistor before voltage amplification occurs, pointing to a common-gate (CG) stage. However, the required 50Ω input resistance translates to a large device width (20μm), degrading the input match (S_{11} = –1.5dB) and increasing the noise figure. That is, the capacitance seen at the source node must be cancelled by means of resonance. Similarly, the output node must also resonate so as to cancel the capacitance seen at the drain of the transistor and introduced by the next stage.

Figure 21.6.3 depicts the LNA implementation, where L_1 resonates with C_{GS1}+ C_{SB1} and the pad capacitance, and L_2 with the total capacitance at node X. Transistor M_2 provides additional gain and drive capability for the subsequent quadrature mixers. The three inductors are realized as the folded microstrip shown in Fig. 21.6.2.

The use of coupling capacitors in the 60GHz path to isolate bias levels must deal with both bottom-plate parasitics and possible resonances within the capacitors (especially those utilizing lateral fringe fields). For this reason, a biasing scheme is introduced here that obviates the need for coupling capacitors. In the circuit of Fig. 21.6.3, M_2 serves as a diode-connected device, carrying a current equal to $I_T - I_{D1}$. Thus, with negligible DC drops across L_2 and L_3, M_2 can form a current mirror along with the common-source device(s) in the next stage. The LNA simulations indicate a noise figure of 4.5dB and a voltage gain of 12dB while drawing a supply current of 4mA.

Each of the quadrature mixers is implemented as shown in Fig. 21.6.4. The dimensions of M_1 (8μm/0.13μm) are dictated by the 60GHz resonance at the LNA output. Inductor L_1 (also realized as a folded microstrip) resonates with the capacitances of M_1-M_3, thereby allowing most of the RF current produced by M_1 to be commutated by M_2 and M_3. Additionally, this inductor provides about 1/3 of the bias current of M_1, helping to minimize the noise contributed by M_2 and M_3 and maximize the value of R_D and hence the conversion gain. The mixer core simulation reveals a noise figure of 10dB and a conversion gain of 8dB while drawing 0.9mA from the supply. It is exceedingly difficult to generate external differential signals at 60GHz. For test purposes, a single-ended to differential converter is included on the chip. As shown in Fig. 21.6.5, the converter consists of two equal coupling capacitors (realized as metal sandwiches) and an inductor (implemented as a folded microstrip). The operation can be seen by assuming an ideal *current* source at the input (and no 50Ω termination). At the series resonance frequency of C_1, L_1, and C_2, the input voltage falls to zero, and the current flowing through the series network generates equal and opposite voltages across C_1 and C_2. With a finite load impedance (the input capacitance of the mixer), the balance between LO and $\overline{LO}$ degrades to some extent.

The receiver has been implemented in a 0.13μm CMOS technology. Fig. 21.6.6 shows the floor plan of the chip . The longest 60GHz interconnect occurs between the LNA and the inputs of the two mixers. This line is about 35μm long and is modeled by field simulations. Figure 21.6.7 depicts the die, whose active area is approximately 400μm×300μm. The circuit has been tested on a high-speed probe station while operating with a 1.2V supply. The measured voltage gain is 28dB, about 8dB lower than expected. This is attributed to the LO imbalance produced by the network of Fig. 21.6.6. The noise figure is obtained as follows. A 60GHz signal having a precisely measured level of –35dBm (by means of a power meter) is applied to the receiver. The input SNR in 1Hz is thus equal to 174dBm – 35dBm = 139dB. The down-converted signal at an IF of 100MHz is then displayed on a spectrum analyzer and the output SNR in 1Hz is calculated. Also, the loss of the connectors, cables, and the probes is determined using an on-chip calibration pad frame. The resulting noise figure is 12.5dB, about 4dB higher than expected. This discrepancy is attributed to the LO imbalance, the noise floor of the spectrum analyzer, and other noise components picked up by the probes. The 1dB compression point is –22.5dBm and the power dissipation is 9mW.

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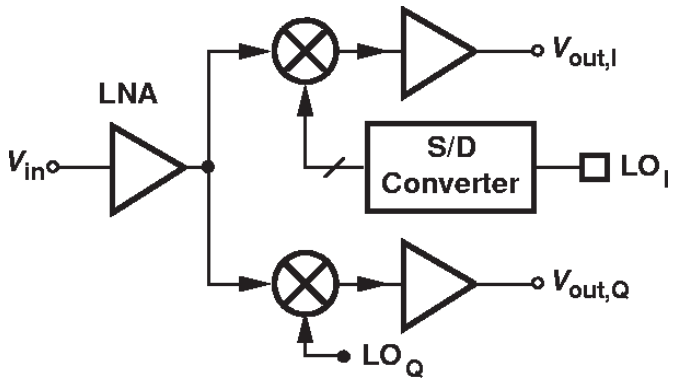

Fig. 21.6.1. Receiver architecture.

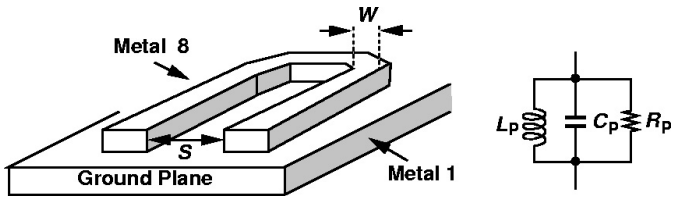

Fig. 21.6.2. Folded microstrip and its narrowband equivalent circuit.

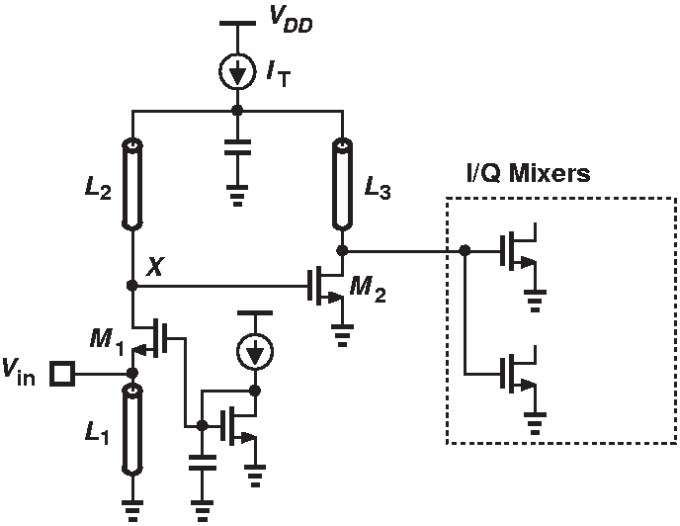

Fig. 21.6.3. Low-noise amplifier.

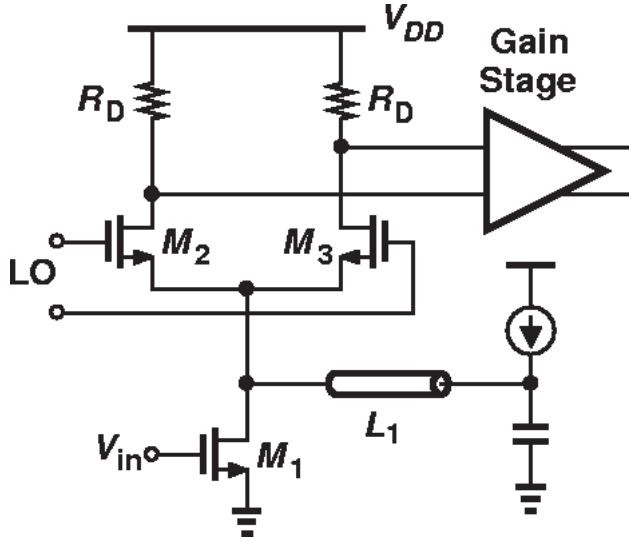

Fig. 21.6.4 Mixer.

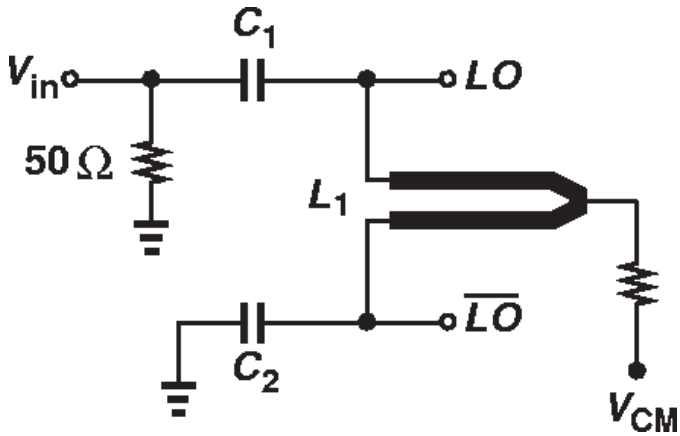

Fig. 21.6.5. Single-ended to differential converter.

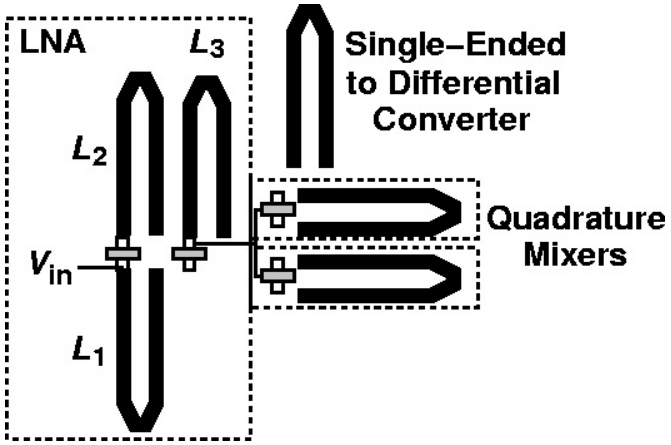

Fig. 21.6.6. Receiver floor plan.

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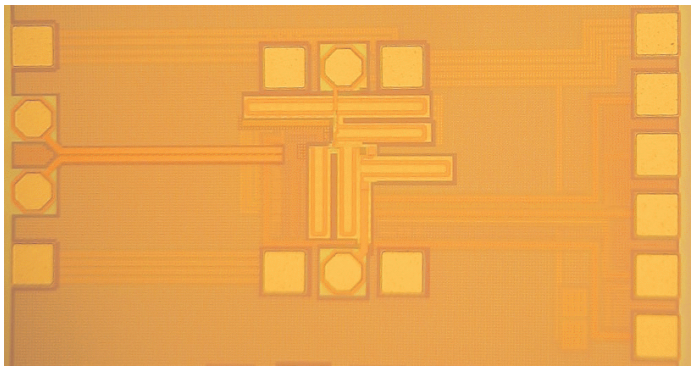

Figure 21.6.7. Receiver die photograph.

