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A 900-MHz/1.8-GHz CMOS Transmitter for Dual-Band Applications

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Abstract

This paper introduces a 900-MHz/1.8-GHz CMOS transmitter designed for dual-band applications. Configured as a two-step architecture, the circuit generates the first upconverted signal in quadrature phases and subsequently performs single-sideband modulation to produce the output in the two bands. Fabricated in a 0.6-μm CMOS technology, the transmitter draws 70 mW from a 3-V supply.

I. Introduction

Multi-standard transceivers have recently become the topic of active research as they provide substantially higher flexibility in mobile communications in different geographical areas while exploiting the newly-released bands in the 1.8-GHz range to increase the capacity. Cost and form factor considerations, however, severely constrain the choice of the architecture and the frequency planning as well as the design of the building blocks of such transceivers. In particular, the number of oscillators, frequency synthesizers, and external filters and resonators must be minimized.

This paper describes the design of a 900-MHz/1.8-GHz CMOS transmitter for dual-band applications, with emphasis on compatibility with the Global System for Mobile Communication (GSM) and Digital Communication System at 1800 MHz (DCS1800) standards. Employing two upconversion steps, the circuit generates 900-MHz and 1.8-GHz outputs that can assume linear or nonlinear modulation depending on the type of signals applied to the baseband ports. Fabricated in a 0.6-μm digital CMOS technology, the transmitter consumes 70 mW from a 3-V supply.

Section II of the paper presents general issues in dual-band transceivers, Section III introduces the transmitter architecure, and Section IV describes the design of the building blocks. Section V summarizes preliminary experimental results.

II. General Considerations

The GSM and DCS1800 standards incorporate the same modulation format, channel spacing, and antenna duplexing. Summarized in Table I are the characteristics of each standard, indicating that a dual-band transceiver can exploit the properties common to both so as to reduce the off-chip hardware.

In order to minimize the number of oscillators and synthesizers, the receivers and transmitters in a dual-band system must be designed concurrently, with the frequency planning carried out such that the receive and transmit paths are driven by the same synthesizers. Although GSM and DCS1800 utilize frequency-division duplexing (FDD) at the front end, their actual operation is somewhat similar to time-division duplexing (TDD) because their receive and transmit time slots are offset by 1.73 ms (three time slots) (Fig. 1). Thus, frequency synthesizers can be time-shared between the receiver and the transmitter.

	GSM	DSC1800
Modulation	Gaussian Minimum Shift Keying	
Multiple Access	Time-Division Multiple Access	
Duplexing	Frequency-Division Duplexing	
Receive Band	935–960 MHz	1805–1880 MHz
Transmit Band	890–915 MHz	1710–1785 MHz
Channel Spacing	200 kHz	
Number of Channels	124	350

Table 1. System characteristics of GSM and DCS1800.

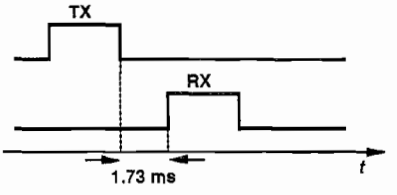

Fig. 1. Time offset between receive and transmit time slots.

The dual-band transmitter described here is designed in conjunction with the dual-band receiver reported in [1]. To understand the frequency planning issues, we briefly review the receiver (Fig. 2). Based on the Weaver image-reject architecture [2], the receiver performs the first downconversion such that the GSM and DCS1800 bands appear as images of each other. The Weaver topology then selects one band and rejects the other by addition or subtraction of the spectra at points A and B. The first local oscillator (LO) frequency is therefore equal to 1350 MHz —midway between the two bands— and the second LO frequency is in the vicinity of 450 MHz.

To minimize the number of LOs and synthesizer loops, it is desirable to utilize the same LO frequencies for the transmit path as well. Fig. 3 illustrates an example, where the baseband in-phase (I) and quadrature (Q) signals are upconverted to 450 MHz, separated into quadrature components by means of the RC-CR network, and mixed with quadrature phases of the second LO (operating at 1350 MHz). Since the signals at points M and N are of the form $\cos(\omega_1 t - \theta - \pi/4)$ and $\cos(\omega_1 t - \theta + \pi/4)$, the addition or subtraction of the spectra

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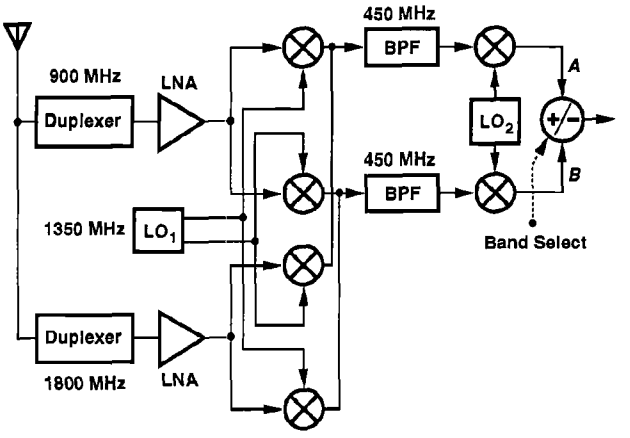

Fig. 2. Dual-band receiver architecture.

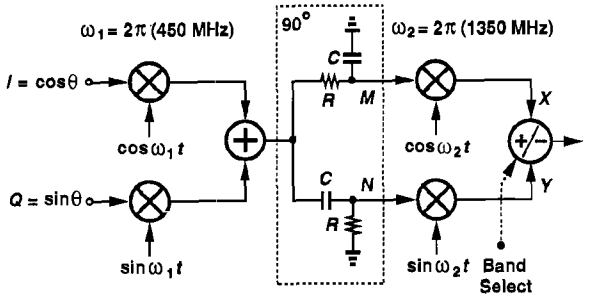

Fig. 3. Simple dual-band transmitter.

at X and Y generates the modulated waveform at 900 MHz or 1.8 GHz.

The principal drawback of the above architecture stems from the use of an RC-CR network to perform quadrature separation. Even with perfect matching between the two paths, the variation of RC with process and temperature introduces considerable gain mismatch between V_M and V_N, thereby creating a significant unwanted sideband at the output. Illustrated in Fig. 4 for DCS1800 generation, this effect may seem unimportant because the 900-MHz spur is further suppressed

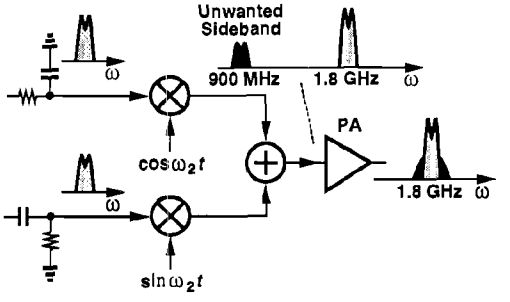

Fig. 4. Effect of unwanted sideband on DCS1800 output.

by the limited bandwidth of the following power amplifier (PA) and the antenna. However, second-oder distortion in the PA produces the second harmonic of the unwanted sideband, corrupting the desired channel with a signal that, from Carson's rule [3], occupies nearly twice the bandwidth. In other words, the 900-MHz spur ultimately increases the adjacent-channel power (ACP) of the transmitted signal.

Another issue in this architecture is that the 900-MHz and 1.8-GHz signals appear at the same output port, making it difficult to employ narrowband tuned amplification at this port.

The architecture of Fig. 3 is nonetheless an attractive option if the quadrature components of the first intermediate frequency (IF) can be generated with less susceptibility to gain error.

III. Dual-Band Transmitter Architecture

In order to generate the quadrature components of the 450-MHz IF signal, we recognize that the *baseband* signal is available in quadrature form. A Gaussian minimum shift keying (GMSK) waveform with center frequency ω can be expressed as $x(t) = A\cos[\omega t + \int \sum p(t - kT_S) * h(t)dt]$, where $\sum p(t - kT_S)$ denotes the baseband binary stream and $h(t)$ is the impulse response of a Gaussian filter [4, 5]. Thus, $x(t) = A\cos\omega t\cos[\int \sum p(t-kT_S)*h(t)dt] - A\sin\omega t\sin[\int \sum p(t-kT_S) * h(t)dt]$, indicating that the baseband quadrature components are $I = \cos\theta$ and $Q = \sin\theta$, where $\theta = \int \sum p(t - kT_S) * h(t)dt$. The I and Q waveforms are usually generated from $\sum p(t - kT_S)$ by mixed-signal techniques [5, 4].

With the I and Q signal available, generation of the IF in quadrature form can be performed as depicted in Fig. 5. While using two more mixers than the first upconversion in Fig. 3,

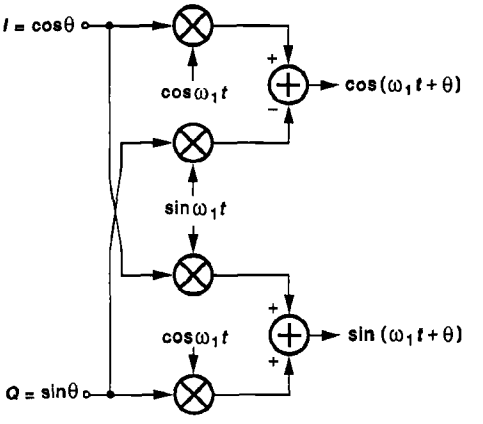

Fig. 5. Upconversion with quadrature outputs.

this technique provides higher precision in the phase and gain balance between the two paths. The output components of the first upconverter can now be multiplied by the quadrature phases of the second LO and added or subtracted to generate the GSM and DCS1800 signals. However, it is desirable to design the second upconversion such that the 900-MHz and 1.8-GHz waveforms appear at the outputs of two *different* circuits, thus allowing efficient narrowband amplification. This can be accomplished as illustrated in Fig. 6, where two independent single-sideband (SSB) modulators produce the two bands according to the band select command. Note that only one of the modulators is active in either mode, saving power consumption.

The overall architecture of the dual-band transmitter is shown in Fig. 7. Note that all of the signals up to ports A and B are differential. Each band incorporates a differential to single-

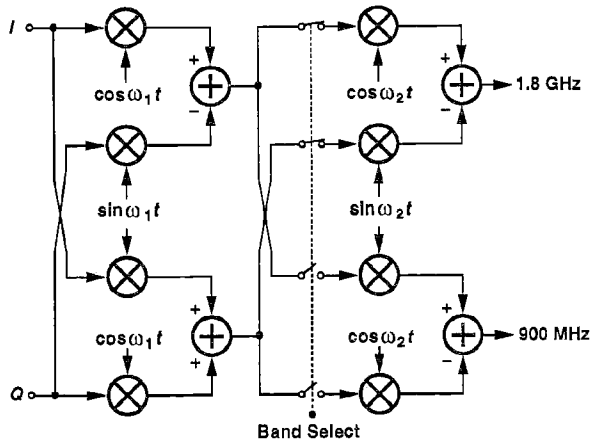

Fig. 6. Two-step upconversion generating 900-MHz and 1.8-GHz outputs.

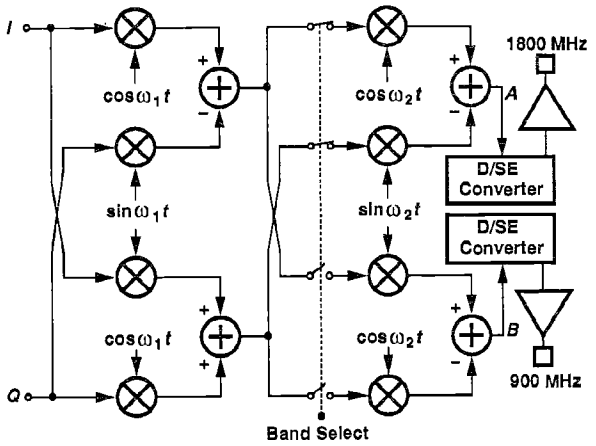

Fig. 7. Dual-band transmitter architecture.

ended (D/SE) converter, applying the result to an output buffer.

IV. Building Blocks

Fig. 8 shows the implementation of the first upconversion modulator. The baseband signals are multiplied by the quadrature components of the first LO and the results are added in the current domain. Two 100-nH inductors resonating at 450 MHz convert the current to voltage. To minimize the area occupied by each inductor, a stack of three spiral structures made of three metal layers is used, reducing the area by a approximately a factor of 8.1 [6].

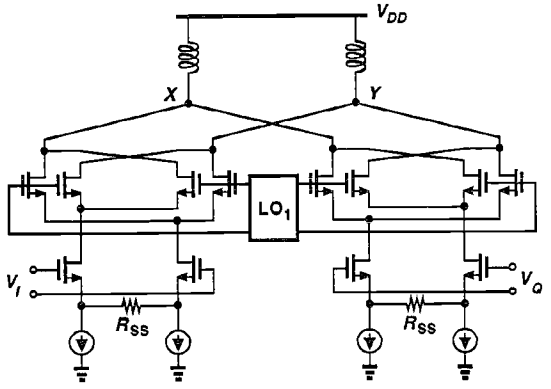

Fig. 8. First upconversion modulator.

The odd-order nonlinearity of the upconversion mixers impacts the purity of the modulated output. Calculations indicate that if V_I and V_Q in Fig. 8 experience third-order *harmonic* distortion, the resulting GMSK signal exhibits substantial adjacent-channel power. It can also be shown that to comply with the GSM transmission mask, the third harmonic must be roughly 40 dB below the fundamental. Each mixer therefore incorporates source degeneration to achieve the required linearity with a 0.5-V_{pp} baseband input.

The signals generated at nodes X and Y in Fig. 8 must be "routed" to one of the single-sideband modulators according to the band select command. As shown in Fig. 9, the routing is performed in the current domain to minimize signal loss due to addition of the switches. Capacitively-coupled to the output of the 450-MHz modulator, the voltage-to-current converter employs grounded-source input devices to save the voltage headroom otherwise consumed by a current source. The bias current of the circuit is defined by I_0 and M_0. Note that S_1-S_4 operate in deep triode region. Also, the linearity of this and subsequent stages is not critical because GMSK signals have a constant envelope [5].

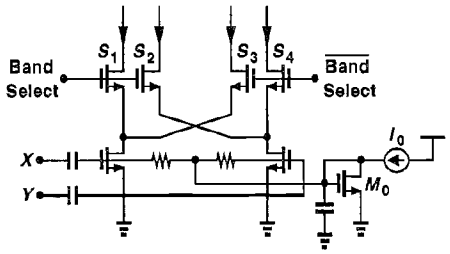

Fig. 9. Voltage-to-current converter with output switching.

Each SSB modulator in Fig. 7 is realized as depicted in Fig. 10. Sensing the differential current signals routed from each 450-MHz modulator, the circuit performs mixing with the second LO, adds the resulting currents, and converts the output to single-ended form. Fig. 11 shows two types of D/SE converters studied in this work. In Fig. 11(a), a current mirror arrangement incorporates resonance at nodes E and F, reducing the effect of device capacitance. The difficulty here is the large gate-source capacitance of the two PMOS devices, mandating a small value for L_1 and hence a low conversion

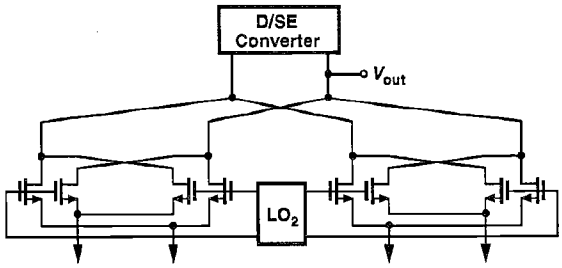

Fig. 10. Single-sideband modulator circuit.

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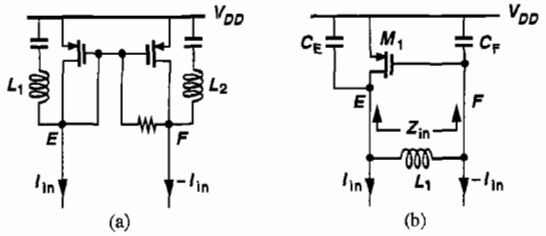


Fig. 11. Differential to single-ended conversion using (a) tuned current mirror, (b) negative resistance generator.

gain. Fig. 11(b) presents an alternative topology where a PMOS device introduces a negative resistance in parallel with a floating inductor. It can be shown that

$$Z_{in} = \frac{g_{m1}}{C_E C_F s^2} + \frac{1}{C_E s} + \frac{1}{C_F s}, \qquad (1)$$

where C_E and C_F denote the total capacitance at nodes E and F, respectively [5]. As a compromise between margin to oscillation and boost in gain, the negative resistance, $-g_{m1}/(C_E C_F \omega^2)$, is chosen to increase the Q of the inductor by approximately a factor of two. Note that L_1 can assume a relatively large value because it sees C_E and C_F in *series*. In this design, the signal is sensed at F because this port exhibits a lower output impedance. Simulations indicate that the topology of Fig. 11(b) provides about three times the voltage gain of the circuit in Fig. 11(a).

The output buffer is shown in Fig. 12. Two common-source stages boost the signal level, delivering power to the 50-Ω input

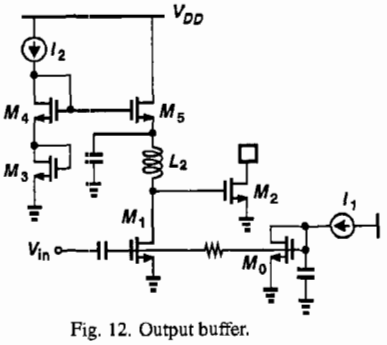


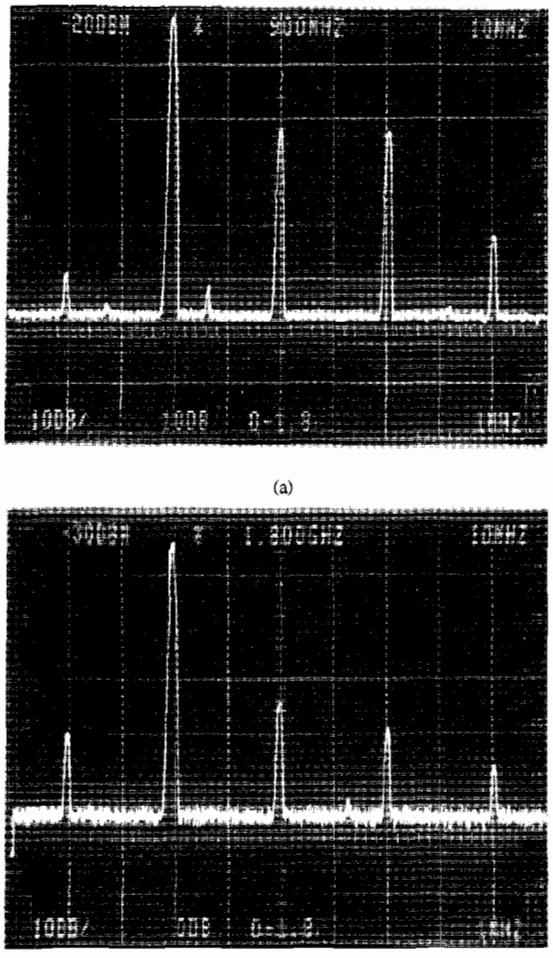
Fig. 12. Output buffer.

impedance of an external power amplifier. The bias current of M_2 is defined by I_2 and M_3 [1]. Neglecting the dc drop across the inductor, we can write $V_{GS3} + V_{GS4} = V_{GS5} + V_{GS2}$, that is, I_{D2} can be ratioed with respect to I_2.

V. Experimental Results

The transmitter has been fabricated in a 0.6-μm digital CMOS technology, occupying an active area of approximately 1300 μm $\times$850 μm. All of the inductors shown in Figs. 8, 11(b), and 12 are integrated with no additional processing steps.

The fabricated prototype was received a few days before the submission of the paper. Fig. 13 shows the measured output in the two bands with a baseband signal frequency of 20 MHz. The power dissipation is 70 mW from a 3-V supply. More measurements are under way.



(a)

(b)

Fig. 13. Measured output spectrum at (a) 880 MHz and (b) 1.78 GHz. (Horiz. 10 MHz/div., vert. 10dB/div.)

References

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