

TP 16.3 A CMOS Interface Circuit for Detection of 1.2Gb/s RZ Data

Jafar Savoj, Behzad Razavi

University of California, Los Angeles, CA

This CMOS interface circuit is used in a radar system that digitizes the reflected signal by a multi-gigahertz analog-to-digital converter (ADC) employing Josephson junctions, producing a return-to-zero (RZ) differential binary stream with 2mV peak-to-peak amplitude at 1.2Gb/s. The interface amplifies, detects, and demultiplexes the signal, generating a parallel output with 1V_{pp} amplitude at 150Mb/s so the subsequent digital signal processor can receive and process the data reliably.

The design of the interface entails severe trade-offs between bandwidth, gain, noise, and power dissipation. The return-to-zero nature of the 1.2Gb/s signal necessitates a bandwidth roughly equal to that required for a 2.4Gb/s nonreturn-to-zero (NRZ) stream - approximately 1.7GHz. In addition, to generate a signal that overcomes the offset of a high-speed decision circuit, the interface must exhibit gain on the order of 40dB. Moreover, the input-referred noise of the circuit must be small enough that, when integrated across a bandwidth of 2GHz, it yields an error rate <10⁻⁶. The combination of these requirements makes it difficult to design the interface in a 0.6μm CMOS technology.

This work introduces the concept of interleaved matched filters (MFs) as a means of detecting binary streams while relaxing the gain and input-referred noise required of the front-end. While applied to RZ data in this application, the concept can easily be extended to NRZ sequences as well.

Figure 16.3.1 shows the interface architecture. A multi-stage broadband amplifier boosts the signal amplitude with minimal intersymbol interference (ISI), applying the result to two matched filters interleaved in time. For a square pulse, the matched filter can be implemented as an integrate-and-dump operation, with the important advantage that the decision is based on the integral of one bit rather than only the peak value (Figure 16.3.2). Averaging the noise over one bit period, the matched filter, in principle, improves the signal-to-noise ratio by 3dB.

The timing diagram in Figure 16.3.2 illustrates the operation of the interleaved MFs. In this figure, $n(t)$ represents the input-referred additive noise of the system. Each filter operates in three phases: integrate, hold, and dump (reset). As shown in the $x_2(t)$ and $x_3(t)$ waveforms, the two integrators are interleaved in time so when one integrates, the other resets. The idle zero between every two bits in the RZ stream is used to hold the integrated value. The hold phase permits the following decision circuit to sample the integrated level, thus relaxing circuit set-up time. Also, the dump phase allows complete reset, minimizing residual errors in the integrator. The timing of the matched filters and decision circuits is controlled by quadrature phases of CK, which can be generated using a master-slave divider.

To achieve a wide band and low noise with 50Ω input impedance, the amplifier employs a differential common-gate stage followed by six differential common-source pairs. As depicted in Figure 16.3.3, each stage incorporates inductive peaking and the differential pairs also utilize capacitive/resistive degeneration to minimize the pass-band ripple of the amplifier. Using on-chip stacked spiral inductors, each stage overall phase remains a relatively linear function of frequency. Since the quality factor of the inductors is not critical here, the spiral structures have a line width

of only 4.2μm so as to attain a high self-resonance frequency. The value of the inductors ranges from 11nH to 17nH.

The design of the matched filter for gigahertz operation requires a high-speed integrator that can be reset rapidly. The speed and input-referred offset issues mandate a simple, compact topology such as that shown in Figure 16.3.4a. Here, M_1 and M_2 convert the input voltage to current and the result flows through the total capacitance at nodes X and Y. The use of current-source loads requires common-mode feedback (CMFB). Note that this implementation does not provide a hold phase.

The final integrator is depicted in Figure 16.3.4b. Switch S_2 is added to allow a hold operation after integration is completed. Also, the load is realized as two saturated pMOS devices, with R_1 and R_2 serving as the CMFB network. These resistors are in fact realized as pMOS transistors so as to minimize their capacitance. The transistor dimensions are chosen as a compromise between input-referred offset (~10mV) and speed. Each matched filter is biased at a total current of 1mA and provides a voltage gain of approximately 2 at the end of the integrate phase.

The integrated signal produced by each matched filter is subsequently sampled by a decision circuit, i.e., a master-slave flip-flop. To achieve short set-up and hold times, the flip-flops employ current steering with 2V differential swings.

Reset in the integrators requires sharp, rail-to-rail clock edges, while the decision circuit demands fully-balanced clock phases to maximize the timing budget for set-up and hold periods. Note that the integrator reset signal is single-ended, but must exhibit a 50% duty cycle. As depicted in Figure 16.3.5, resistor R_1 serves as both a termination and an equalizing device, thereby ensuring that CK and \overline{CK} cross each other at mid-supply.

The interface circuit in a 0.6μm CMOS technology, occupies 575x1323μm². All inductors are integrated with no process modification. The prototype is characterized at room temperature running from a 3.3V supply.

The front-end amplifier exhibits a gain of 43dB over 2.1GHz bandwidth. With 2mV_{pp} 1.2Gb/s RZ data, both channels yield a relatively open eye diagram. Figure 16.3.6 shows one of the demultiplexed outputs. The circuit consumes 142mW under these conditions. Of this power, 80mW is drained by the preamplifier and 4mW by each matched filter. A die micrograph is shown in Figure 16.3.7.

Acknowledgments:

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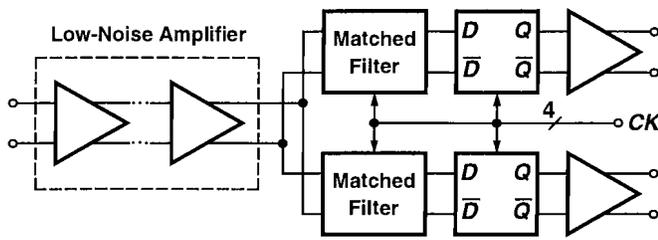


Figure 16.3.1: Interface architecture.

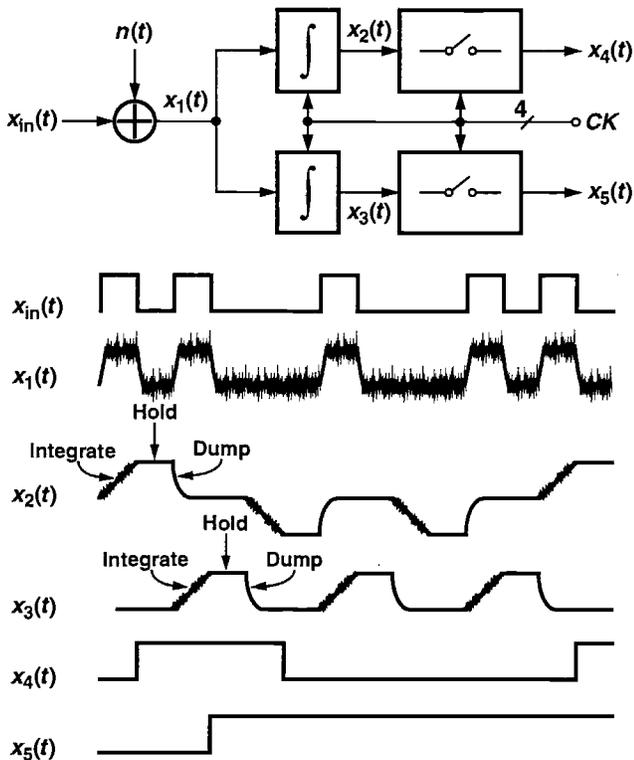


Figure 16.3.2: Operation of interleaved MFs.

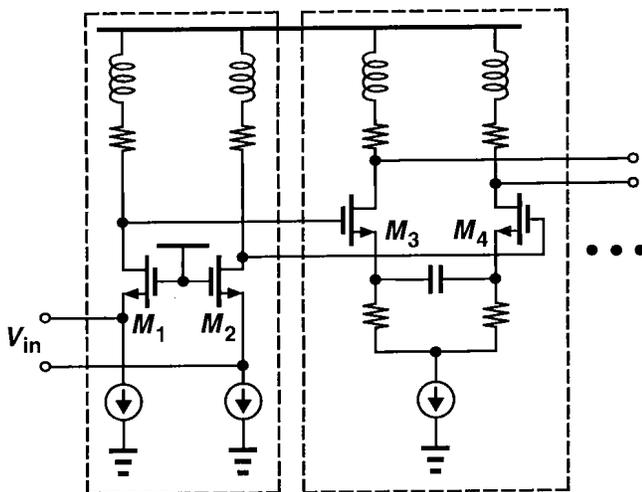


Figure 16.3.3: Front-end amplifier.

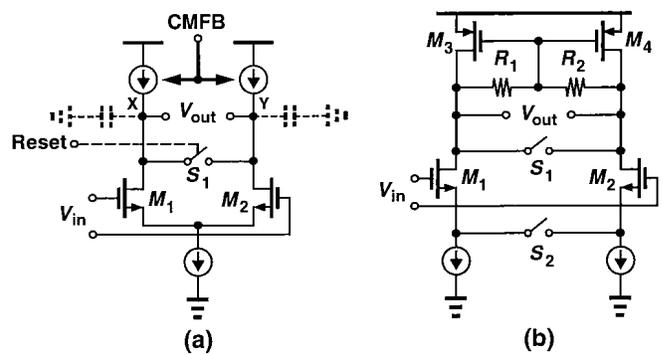


Figure 16.3.4: (a) High-Speed integrate-and-dump, (b) circuit of (a) with hold phase.

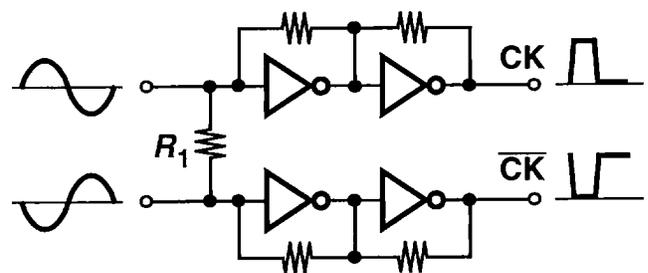


Figure 16.3.5: Clock buffer.

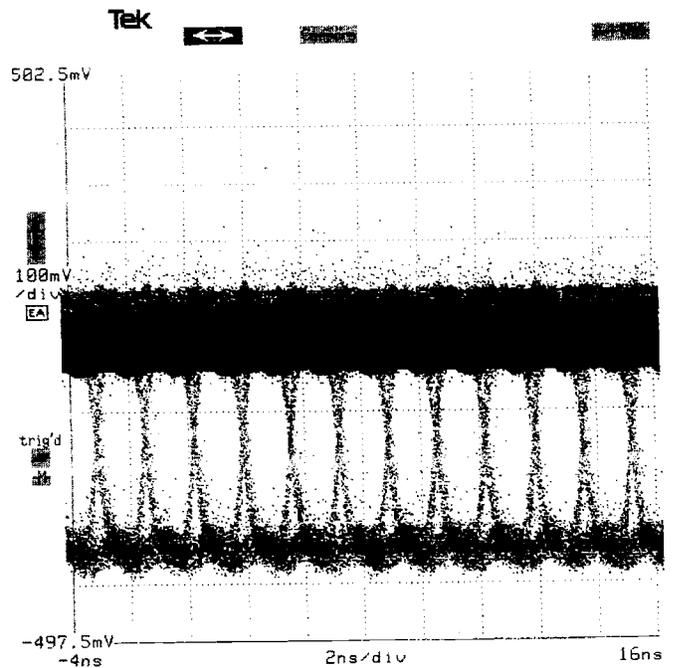


Figure 16.3.6: Eye diagram of demultiplexed output.

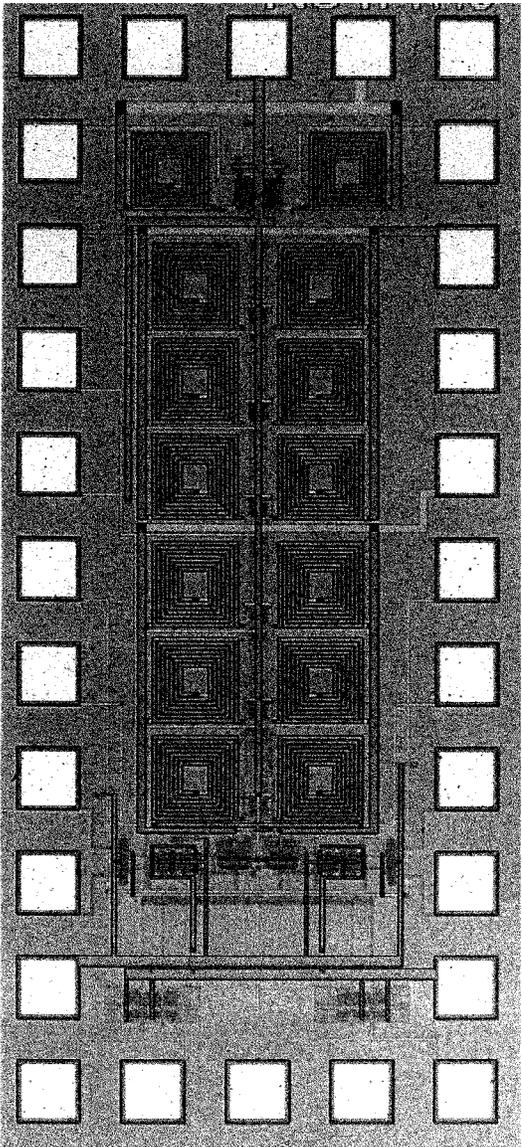


Figure 16.3.7: Chip micrograph.

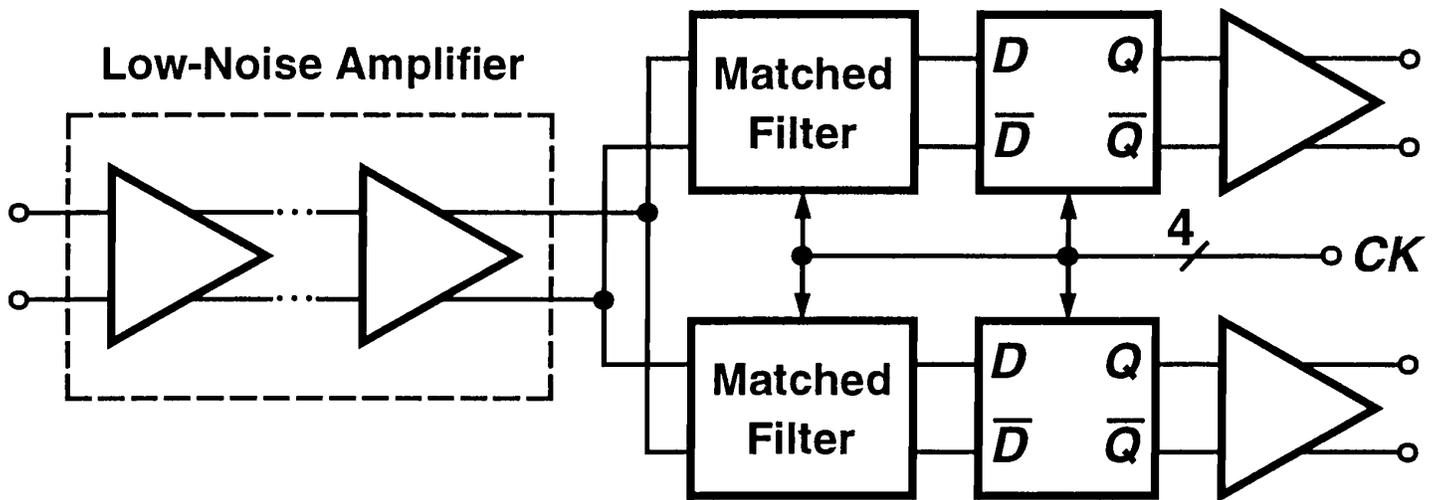


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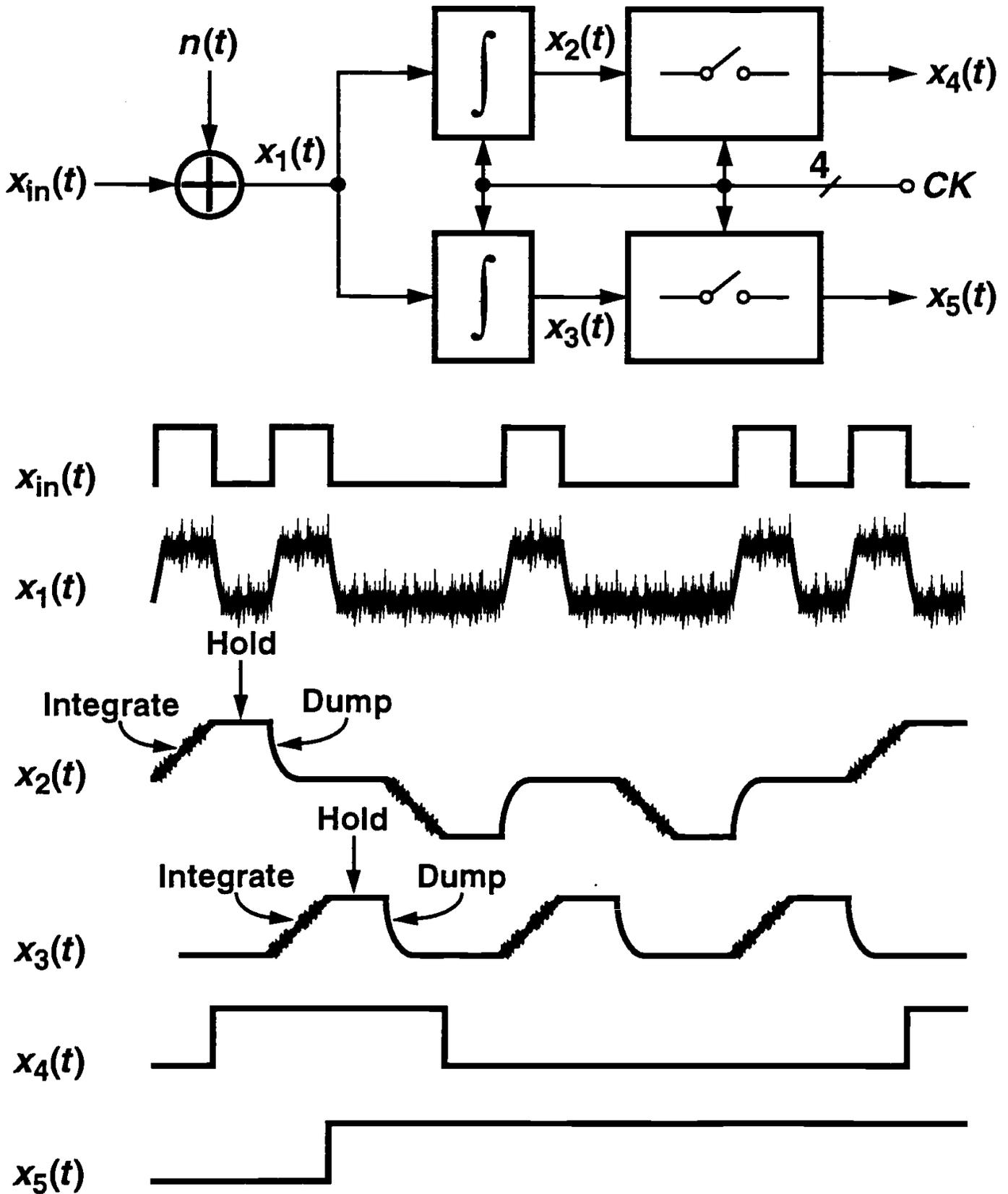


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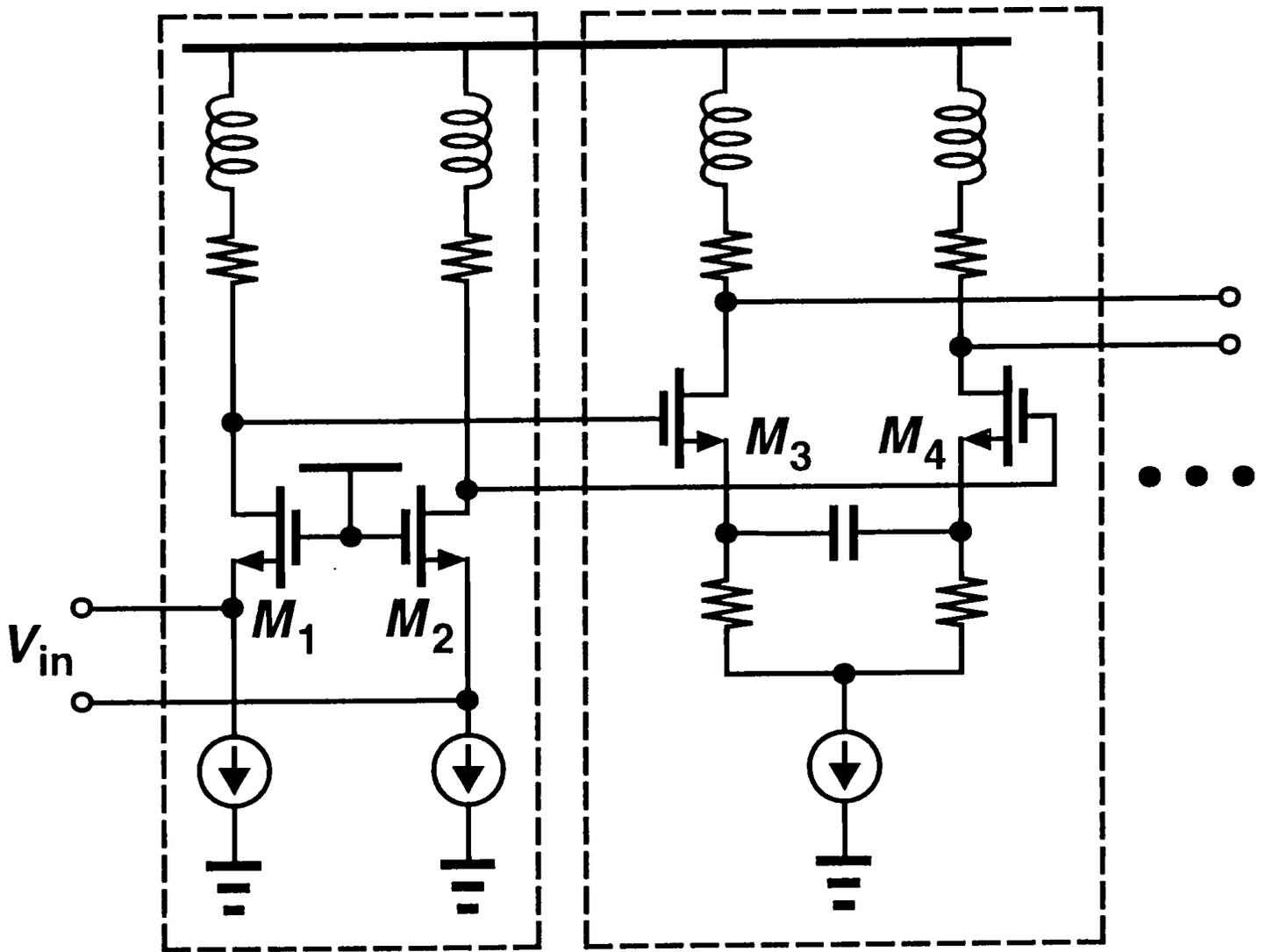


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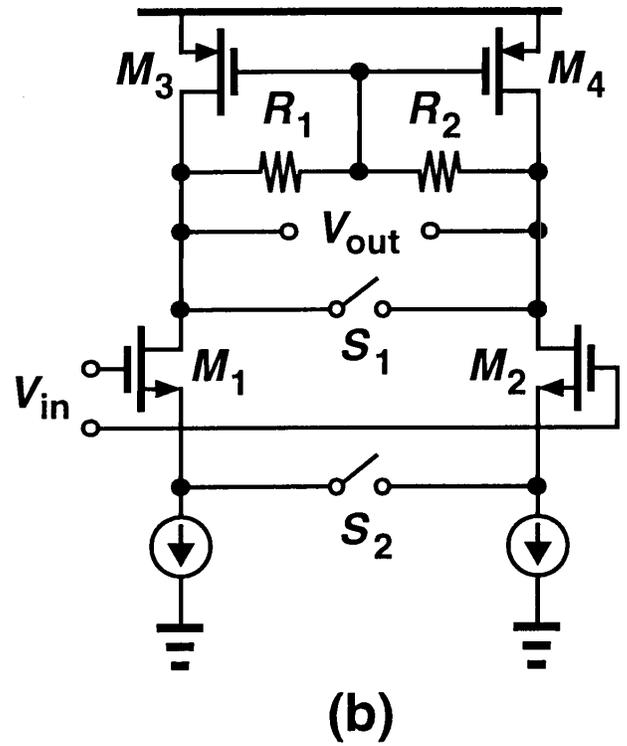
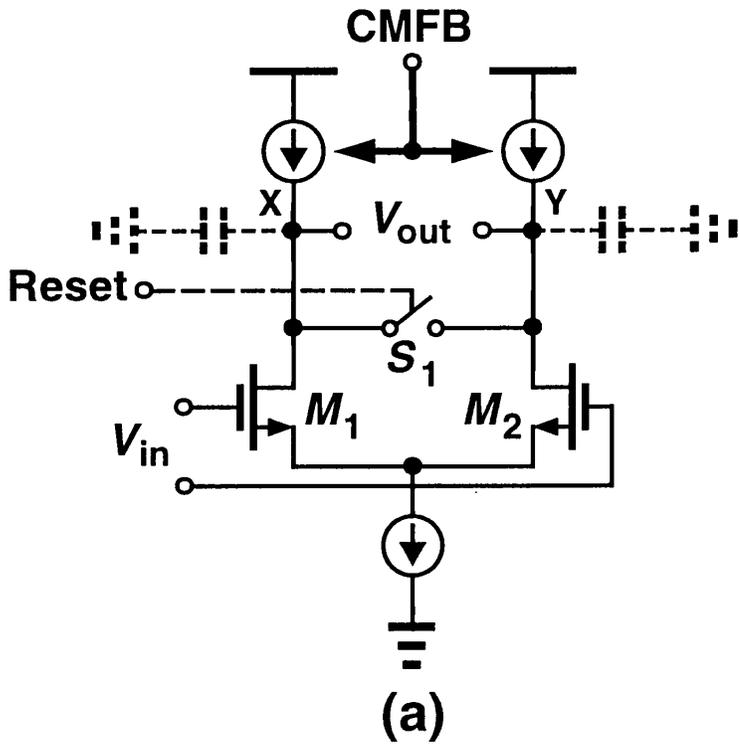


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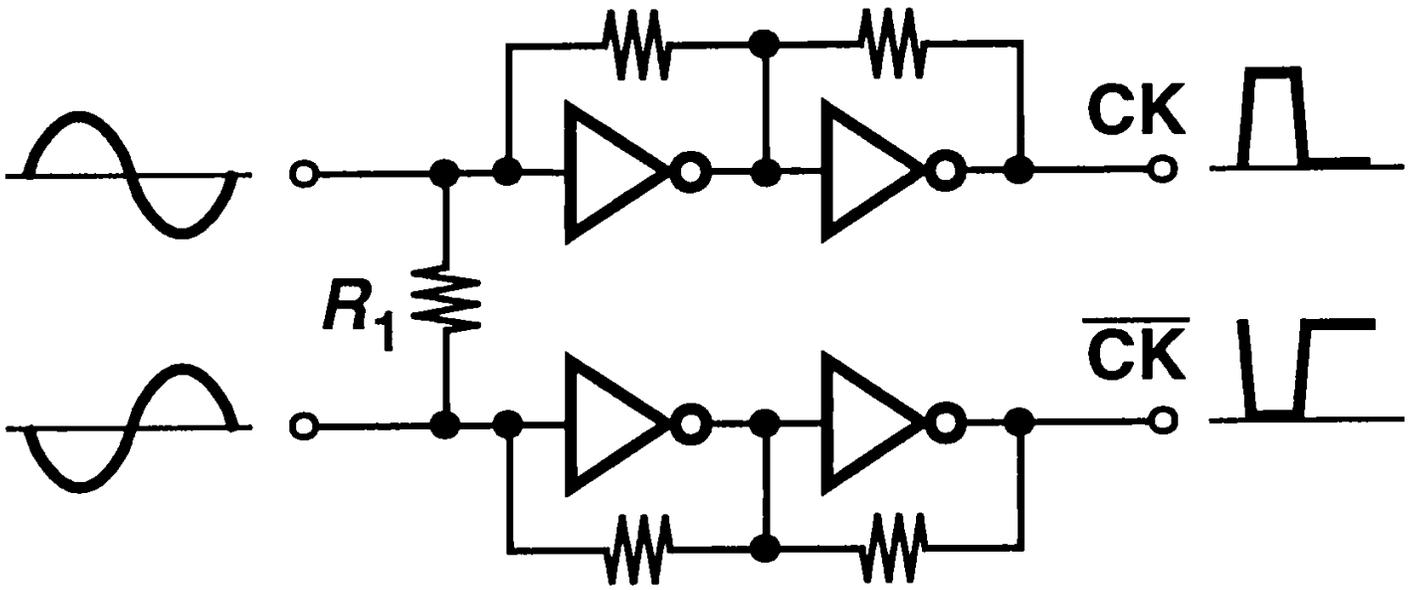


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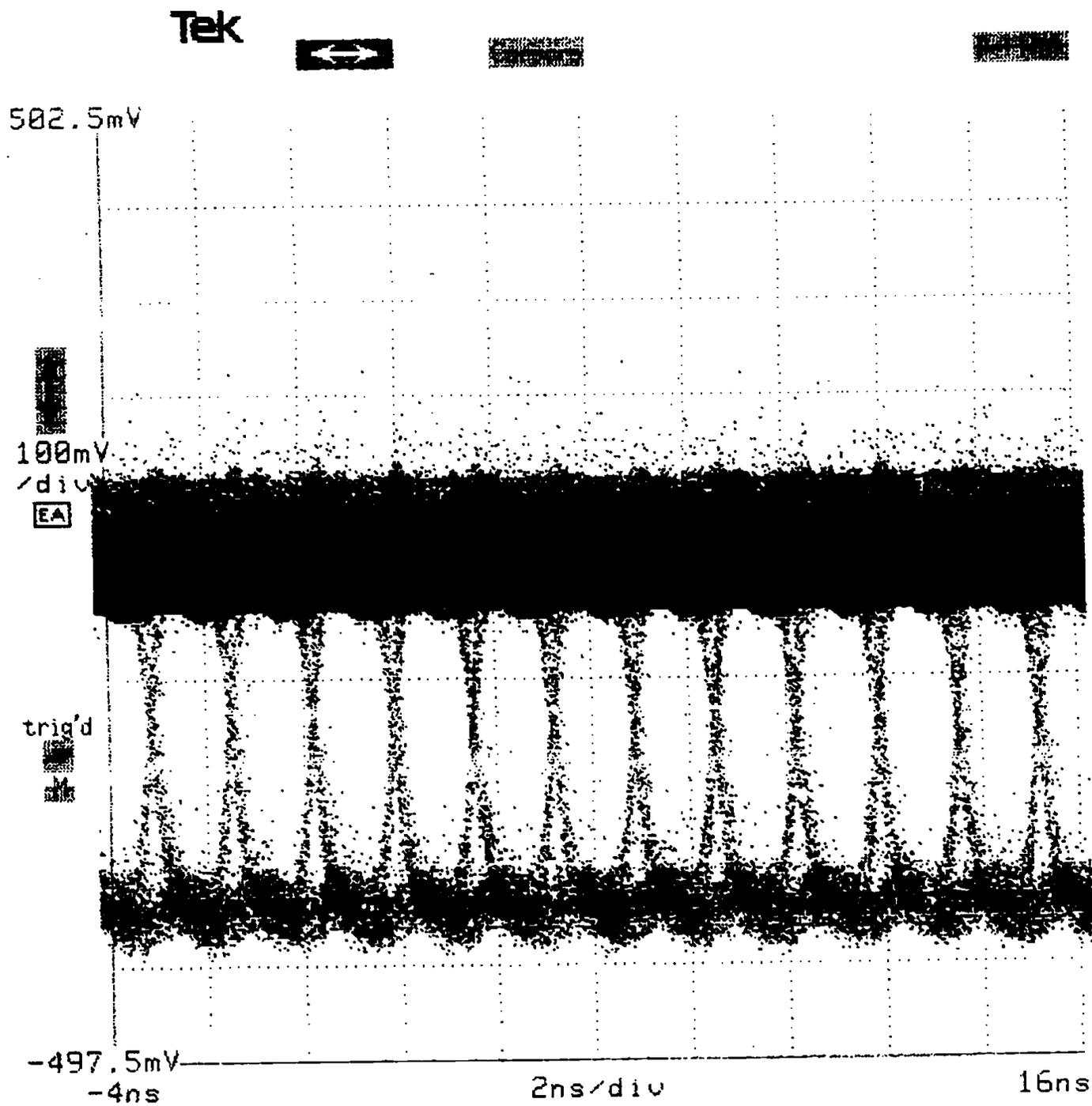


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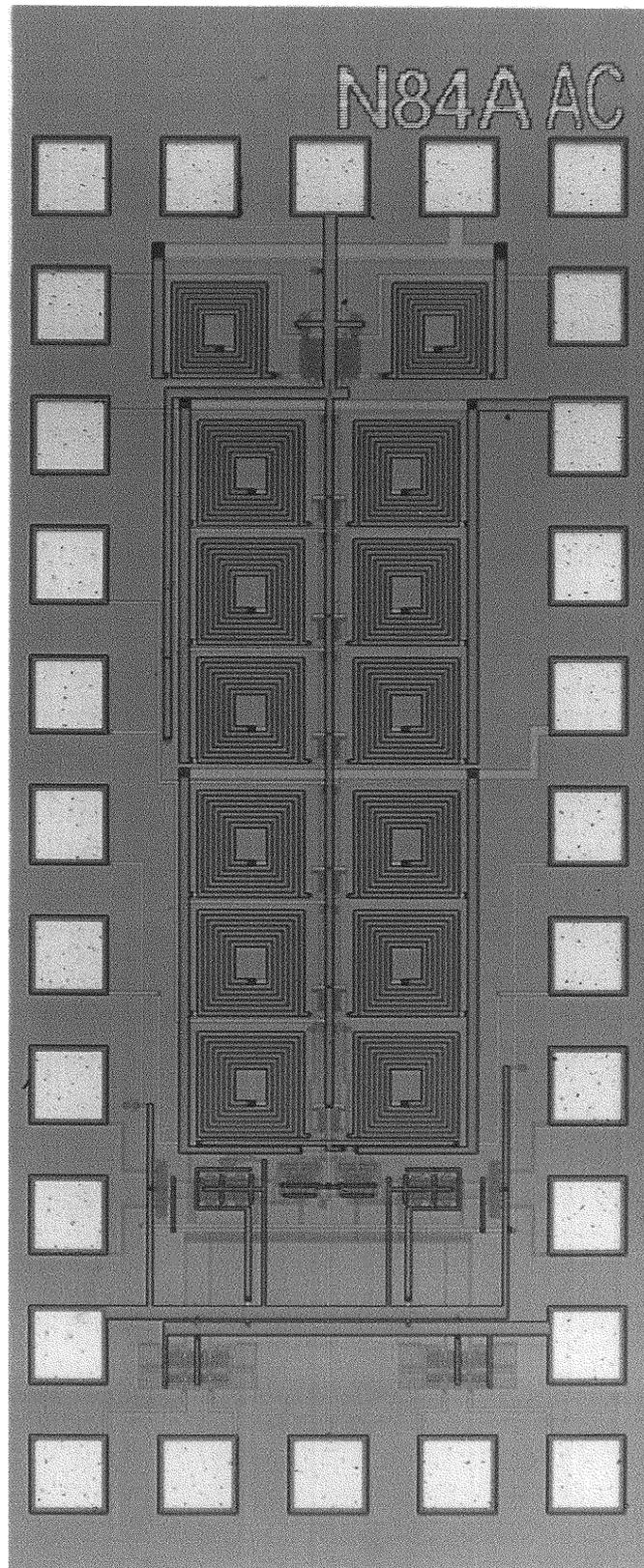


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