A 10-Bit 1-GHz 33-mW CMOS ADC

Bibhu Datta Sahoo and Behzad Razavi

University of California, Los Angeles, CA, USA
bsahoo@ee.ucla.edu and razavi@ee.ucla.edu

Abstract - A pipelined ADC digitally calibrates capacitor mismatches in its 4-bit first stage and the gain error in the first 5 stages. Using a one-stage op amp with a gain of 10 and realized in 65-nm CMOS technology, the ADC digitizes a 490-MHz input with an SNDR of 52.4 dB, achieving an FOM of 0.097pJ/conversion-step.

This paper describes a pipelined ADC architecture that inherently obviates the need for a high-gain, linear op amp. The ADC instead deals with capacitor mismatches by digital calibration. It also corrects for the gain error of each stage in the digital domain.

Architecture The key to easing the op amp linearity requirements is to resolve as many bits as possible in the first stage. This also relaxes the tolerable gain error in subsequent stages. A practical limit arising from kickback noise, power consumption, and input capacitance would be about 6 bits. However, the resolution is further limited by other constraints such as comparator offset and the timing mismatch between the sub-ADC and the multiplying digital-to-analog converter (MDAC) (if no front-end sampler is used). As a compromise, a resolution of 4 bits is chosen in this work.

Fig. 1 shows the ADC architecture. It consists of a SHA-less 4-bit front end, seven 1.5-bit stages, and one 2-bit stage. Digital calibration corrects for capacitor mismatch and gain error in the first stage and only gain error in stages 2 to 5.

The ADC architecture is governed by the choice of the op amp topology. In order to improve the speed-power trade-off, a single differential pair with current-source loads is adopted here. This means that the resolution of the first stage must be high enough and the gain of its MDAC *low* enough to allow such an op amp. Unlike its two-stage counterparts, this topology lends itself to a low closed-loop gain with no need for frequency compensation. In this work, the first MDAC has a nominal gain of 2, achieving a fast settling time (400 ps) with a tail current of 4.8 mA and a load capacitance of 300 fF.

With an MDAC gain of only 2 and a resolution greater than 1 or 1.5 bits, the first stage entails two issues. First the reference voltages required for the subsequent stages are not equal to that of the first. These voltages are sensed from the first sub-ADC resistor ladder (which consumes 3.6 mW). Second, the mismatches among the MDAC sampling capacitors give rise to integral nonlinearity. While these mismatches can be removed by dynamic element matching [1], the three-level multiplexing required in this approach (for a 4-bit stage) would substantially increase the MDAC settling time.

Calibration Algorithm The calibration of the first stage assumes that the remaining stages (the "back end") are ideal. Before describing the calibration (which occurs in the foreground), we note from Fig. 2 that, for a given analog input voltage, V_{in}, the residue output of the first stage can be expressed as $V_{res}=\alpha V_{in}-\beta_j V_R$, where α is the gain of the MDAC, β_j is a function of the thermometer code $T_{15}\ldots T_1$ and the individual capacitor values, and V_R denotes the full-scale reference. The inverse function can thus be written as $V_{in}=V_{res}/\alpha+\beta_j V_R/\alpha$ and, in the digital domain, as $D_{IN}=D_{BE}/\alpha+\beta_j/\alpha$, where D_{BE} is the digital output of the back end. In a multi-bit stage, α does not vary with the input value, introducing a constant gain error. On the other hand, β_j depends on the analog input (as different MDAC capacitors come into play), creating nonlinearity.

Illustrated in Fig. 2, the calibration proceeds as follows. (1) Apply to the main input the voltage V_j in region j (close to the comparator threshold), digitize the residue by the back end to obtain $D_{BE,j}$, and write $D_j=D_{BE,j}/\alpha+\beta_j/\alpha$. (2) Apply V_j again but force the ADC into region j+1, digitize the residue, and write the forced values as $D_{j,f}=D_{BE,j,f}/\alpha+\beta_{j+1}/\alpha$. We must then have $\beta_j-\beta_{j+1}=D_{BE,j,f}-D_{BE,j}$, a quantity independent of α. (3) Repeat these steps for j=1 to 15. These measurements yield 15 equations and 15 unknowns, namely, $\beta_1-\beta_{15}$. Fortunately, the coefficients of β's in these equations form a matrix with a simple inverse, allowing the computation of β's from D_{BE}'s with only right shifts and left shifts and obviating the need for digital multipliers.

The first MDAC also suffers from gain error due to the finite op amp gain and the mismatch between its feedback capacitor and each of the input capacitors. The calibration of gain error proceeds as above but with the roles of C_1 and C_{16} in Fig. 2 swapped. A similar matrix is obtained and another set of β's is calculated. The gain error of stages 2 to 5 is calibrated using the technique described in [2].

The proposed calibration technique offers two advantages over that in [3]. First, the approach in [3] applies to only the mismatch between the input and feedback capacitors in a 1-bit stage, whereas our method is suited to multi-bit stages and deals with mismatches among the input capacitors as well as mismatches between the input capacitors and the feedback capacitor. Second, [3] requires an MDAC gain less than 2 to avoid missing codes while, by virtue of redundancy, our approach can tolerate gains even slightly greater 2, a critical benefit because the closed-loop gain of 2 is established in this design by skewing the capacitor ratio to compensate for the op amp's low gain and is hence subject to variations.

Experimental Results The ADC is realized in digital 65-nm CMOS technology, consuming 15 mW in the analog section, 14.3 mW in the clock tree, and 3.6 mW in the reference. Fig. 3 shows the active die area, which measures 0.225 mm^2.

Figure 4 shows the measured differential nonlinearity (DNL) and integral nonlinearity (INL) at a sampling rate of 1 GHz in three cases: with no calibration, with gain error calibration, and with both capacitor mismatch and gain error calibration. The ADC in fact achieves a resolution of 11 bits but its performance is limited by noise. Fig. 5 plots the measured SNDR as a function of the analog input frequency with a sampling rate of 1 GHz. The SNDR is 52.4 dB at an input frequency of 490MHz, yielding a figure of merit of 0.097pJ/conversion-step. Fig. 6 extends the FOM plot in [4] to include our work.

The calibration logic has been synthesized to estimate its power dissipation. According to simulations, it consumes 1.13 mW.

Acknowledgment The authors thank the TSMC University Shuttle Program for fabrication support. Research supported by DARPA HEALICS Program.

References

[1] E. Siragusa and I. Galton, "A Digitally Enhanced 1.8-V 15-bit 40-MSamples/s CMOS Pipelined ADC", IEEE JSSC, pp. 2126-2138, Dec. 2004.
[2] B. Sahoo and B. Razavi, "A 12-Bit 200-MHz CMOS ADC", IEEE JSSC, pp. 2366-2380, Sept. 2009.
[3] A. N. Karanicolas, H. Lee, and K. Bacrania, "A 15-b 1-Msamples/s Digitally Self-Calibrated Pipeline ADC," IEEE JSSC, pp. 2040-2050 , Dec. 1993.
[4] Jan Mulder et al, "An 800MS/s Dual-Residue Pipeline ADC in 40nm CMOS," ISSCC Dig. Tech. Papers, pp. 184-185, Feb. 2011.

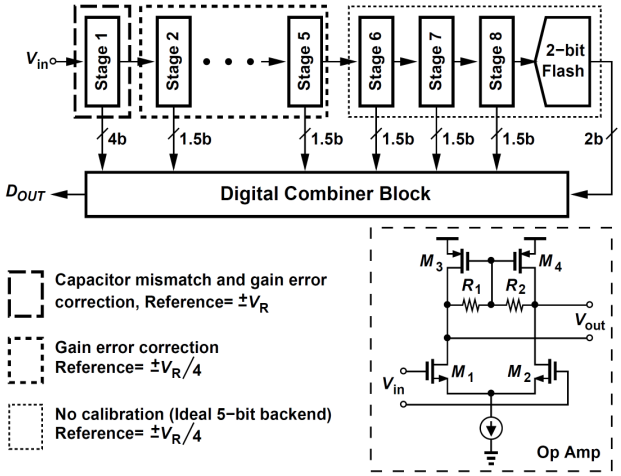

Fig. 1 ADC Architecture.

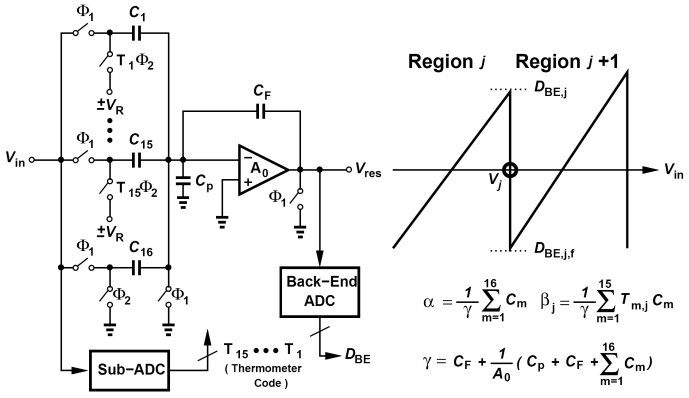

Fig. 2 Capacitor mismatch and gain error calibration methodology.

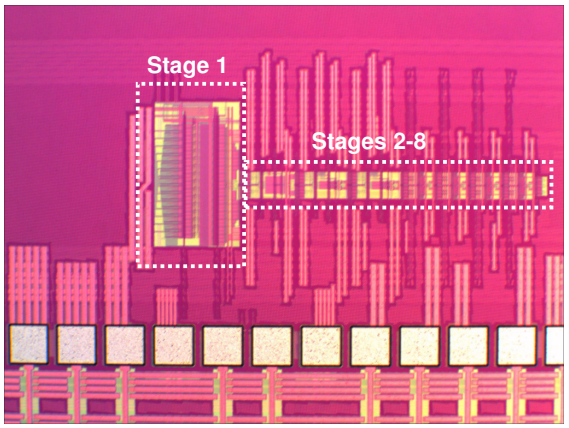

Fig. 3. ADC die photograph.

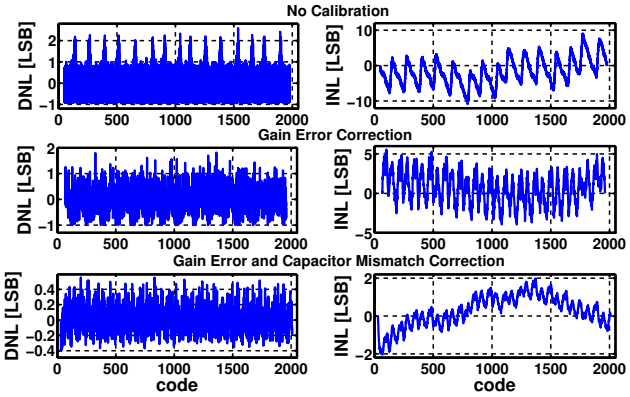

Fig. 4 Measured DNL and INL for 11-bit resolution at f_{CLK} of 1 GHz.

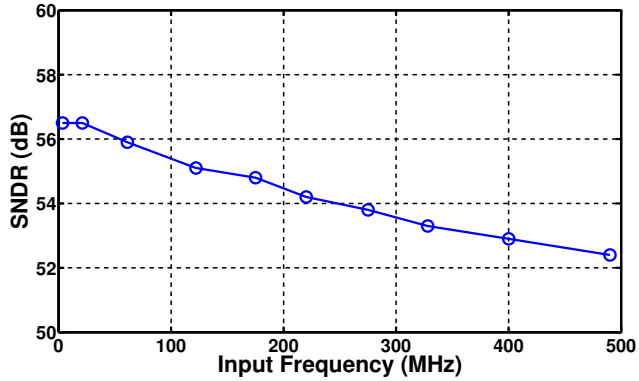

Fig. 5 Measured SNDR at a sampling rate of 1 GHz.

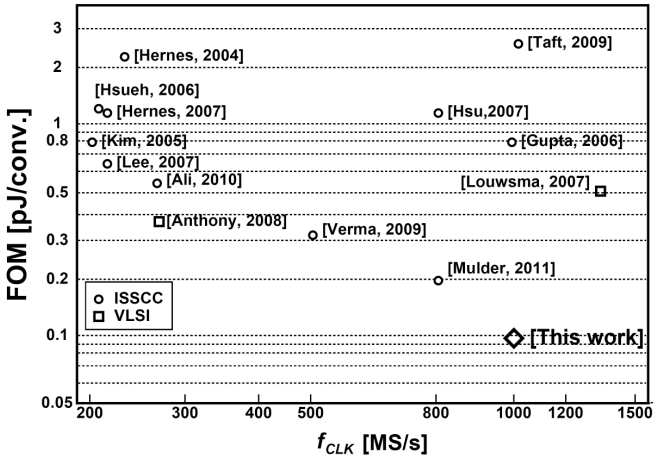

Fig. 6 FOM comparison.