A Low-Power CMOS Receiver for 5 GHz WLAN

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***Abstract*—Mobile devices demand low-power WiFi receivers for extended battery lifetime. This paper presents the design of an 11.6-mW receiver including baseband channel selection filtering that targets the IEEE802.11a standard. A 1-to-6 on-chip transformer serves as a low-noise amplifier with zero power dissipation and high linearity while providing ESD protection and differential outputs. The co-design of the transformer and the passive mixers leads to an efficient front end. Realized in 65-nm CMOS technology, the prototype exhibits a noise figure of 6 dB and a sensitivity of −66 dBm at a data rate of 54 Mb/s from 5 GHz to 5.9 GHz. A new analysis of fully-differential current-driven passive mixers is also presented to facilitate the design of the front end.**

***Index Terms*—Transformer, zero-power, 802.11a, passive mixer, analysis, input impedance, conversion gain, noise figure, harmonic balance, noninvasive filter.**

I. Introduction

THE widespread use of WiFi radios in mobile devices has accentuated their power consumption issues, especially in the case of multi-input multi-output (MIMO) transceivers defined by IEEE802.11n. Among the receiver (RX) building blocks, oscillators, frequency dividers, and analog-to-digital converters have seen dramatic improvements in the past 10 years, now operating with power levels in the milliwatt range [1]–[6]. The main receiver chain, however, still consumes a disproportionately high power, e.g., about 46 mW in [7].

This paper proposes a complete 5 GHz receiver design that meets the IEEE802.11a sensitivity, blocking, and filtering requirements. Several circuit techniques are presented that reduce the overall power to 11.6 mW. Realized in 65-nm CMOS technology, a prototype of the receiver exhibits an input sensitivity of −66 dBm at 54 Mb/s with a variable voltage gain from 5 to 48 dB.

Section II introduces the use of on-chip transformers in place of low-noise amplifiers (LNAs) and Section III describes the receiver architecture. Section IV discusses the properties of current-driven mixers and Section V deals with the transformer/mixer interface. Section VI is concerned with the LO generation circuit, and Sections VII and VIII present the baseband filters and the experimental results, respectively.

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II. Transformer-Based Amplification

Transformers have been utilized at the input of receivers for single-ended to differential conversion [8]–[10], but it appears that they have not been exploited as a means to replace LNAs. The principal role of an LNA in a receiver is to provide voltage gain and input matching with an acceptable noise figure. If a passive device can play this role, then the power consumption and nonlinearity associated with the LNA can be avoided. For example, [11] uses a resonant up-match along with a capacitive network to drive passive mixers directly. One is therefore compelled to consider transformers for this purpose, especially because they also offer ESD protection and differential outputs.

A 1-to-N transformer can, in principle, amplify the input voltage by a factor of N and transform the impedance seen by its secondary to a value necessary for matching (e.g., 50 Ω). However, imperfections such as power loss (and hence noise), limited magnetic coupling, and substantial capacitive coupling may degrade the performance so much as to defeat the purpose. The stacked structure shown in Fig. 1(a), for example, exhibits a high magnetic coupling factor but also a high power loss and capacitive coupling factor. By contrast, the planar geometry depicted in Fig. 1(b) [12] has less capacitive coupling but also lower magnetic coupling. We therefore surmise that the stacked structure in Fig. 1(c) may offer an acceptable compromise, providing a reasonable voltage gain, a lower power loss, and a high self-resonance frequency. In this geometry, the secondary is realized in metal 9 to reduce its capacitance to the substrate, and the primary in metal 8. While not quite symmetric, the secondary avoids bridges that would inevitably add resistance due to contacts and lower metal layers. Since the IP_2 required in 802.11a is fairly relaxed ($\approx$ 0 dBm [13]), this asymmetry is tolerable.

The design of the proposed 1-to-N transformer is dictated by some bounds. As the number of secondary turns increases, the voltage gain grows slowly beyond a point (because the new turns are farther from the primary) but the capacitance and loss rise significantly. Fig. 1(d) plots these trends as predicted by HFSS simulations for the 5 GHz band. Here, the line width and spacing are equal to 4 μm[1] and 2 μm, respectively, and the power loss is defined under matched conditions at both the primary and the secondary.[2] We observe that the voltage gain reaches diminishing returns as the number of secondary turns exceeds 7, and the loss grows beyond 2.5 dB. We have thus chosen six turns as a compromise. This transformer design exhibits an input resistance of 50 Ω (in the 5 GHz band) if the sec-

[1]Further improvement can be achieved if the width of turns is tapered such that the outer turns are wider than the inner turns.

[2]For the receiver input to be matched, the secondary of the transformer must also be matched.

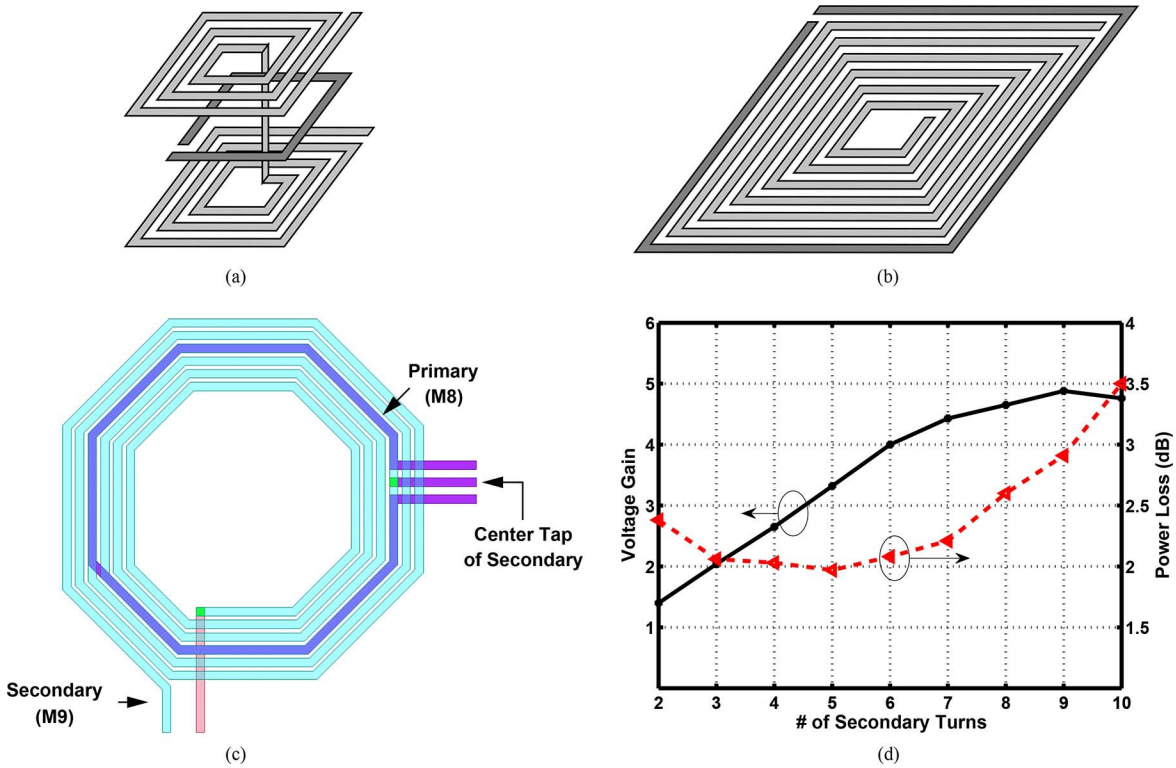


Fig. 1. Various transformer topologies, (a) stacked, (b) planar, and (c) the proposed geometry, and (d) voltage gain and power loss of the proposed transformer versus number of secondary turns.

ondary is terminated into 800 Ω. In other words, looking into the secondary, we see 800 Ω if the primary is driven by 50 Ω.

III. Receiver Architecture

Fig. 2 shows the receiver architecture. The transformer described in the previous section serves as the LNA and differentially drives two sets of passive mixers with 25% duty cycle local oscillator (LO) waveforms. The downconverted signals are then applied to fourth-order elliptic filters for channel selection. The LO frequency arrives at twice the carrier frequency, is divided by two, and creates four 25% duty cycle phases. As explained below, the transformer and the mixers are designed so as to provide input matching, an advantage over the LNA-less receiver in [14]. (The matching becomes necessary because it is difficult in practice to ensure a short connection between the antenna and the receiver input.)

The absence of an active LNA in the front end means that the passive mixers are driven by a low to moderate source impedance. Consequently, the on-resistance of the mixer switches can contribute significant noise, requiring wide transistors and hence a high power dissipation in the LO phase generation circuitry. This issue is revisited in the next section.

By virtue of its high turns ratio, the transformer in Fig. 1(c) exhibits a moderate output impedance. We may therefore view the mixers in Fig. 2 as current-driven[3] circuits and surmise that they contribute less noise than voltage-driven

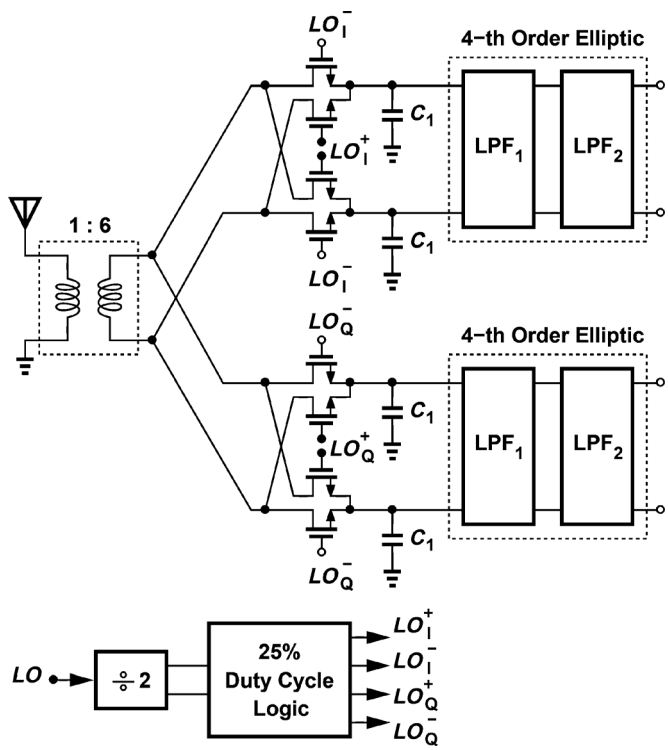


Fig. 2. Receiver architecture.

topologies [15]. Several important questions must be answered. First, how can the transformer and the mixers provide input matching with a reasonable noise figure? Second, how should the mixers' conversion gain be defined in the presence of a finite source impedance? Third, how is the noise figure of the cascade

[3]We use the term "current-driven" in this paper to refer to passive mixers using a time constant (the source resistance times the load capacitance) much longer than the LO period. This condition creates a harmonically-rich voltage waveform at the mixer input, allowing upconversion of the baseband impedance (though this upconversion is not directly exploited in this work).

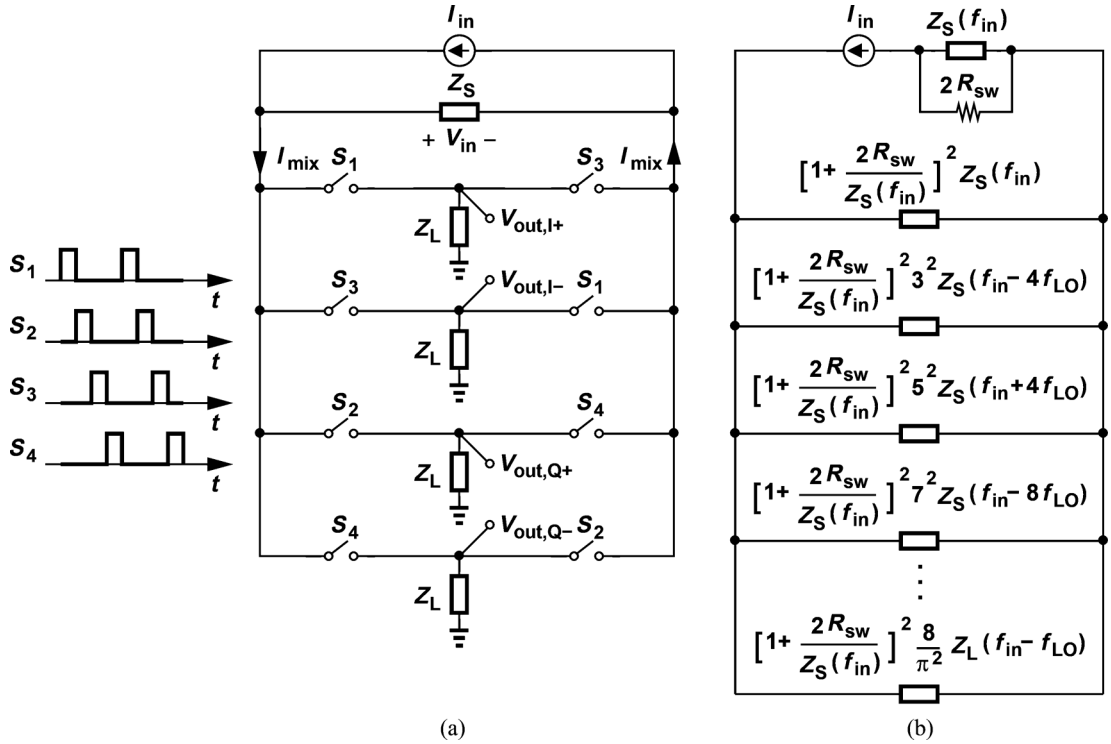


Fig. 3. Current-driven quadrature downconverter, and (b) its equivalent circuit.

calculated? These questions are addressed by the analysis in Appendix I.

IV. Properties of Current-Driven Passive Mixers

Current-driven passive mixers with 25% duty cycle have been analyzed in [16]–[23]. We provide an alternative analysis in Appendix I and utilize the results in this section.

Consider the quadrature downconverter shown in Fig. 3(a), where S_j denotes both a switch and the unity-height LO waveform controlling that switch. As shown in Appendix I, the circuit can be viewed as in Fig. 3(b), if only the load impedance translated to $\pm f_{\rm LO}$ is included. We make two observations. First, if Z_S is real and equal to R_S and if Z_L is capacitive, then the impedance seen by $I_{\rm in}$ simplifies to $(8/\pi^2)R_S^2/(R_S+2R_{sw})+R_S||(2R_{sw})$. This impedance varies from $0.81R_S$ to R_S as R_{sw} ranges from 0 to infinity. For input matching on the other hand, $I_{\rm in}$ must see $R_S/2$ (one R_S as the source impedance and another presented by the circuit). That is, such a topology cannot provide input matching.

Second, for a complex source impedance, the translated copies of Z_S in Fig. 3(b) can contribute resistance at $f=f_{\rm LO}$, allowing input matching. This point proves useful in our front-end design as the transformer's output impedance at harmonics of $f_{\rm LO}$ exhibits significant "tails" at $f_{\rm LO}$.

The noise properties of the quadrature downconverter also provide design guidelines. For a simple case of $Z_S=R_S$ and $Z_L=1/(C_LS)$, Appendix I yields NF $=(\pi^2/8)(1+2R_{sw}/R_S)$, implying that R_{sw} must be chosen small enough for a reasonable NF. However, the wide switches in this case would require substantial power dissipation in the LO network. Additionally, in the absence of gain preceding the downconverter, the first baseband stage must exhibit a very low input noise. Both of these issues are mitigated by the use of a step-up transformer.

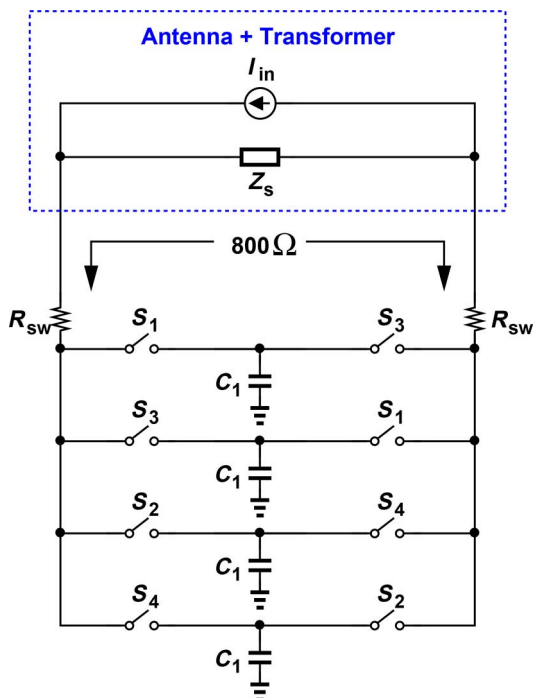


Fig. 4. Transformer-mixer interface.

V. Transformer-Mixer Codesign

Having analyzed 1-to-N transformers and passive mixers with 25% LO duty cycle in previous sections, we now deal with

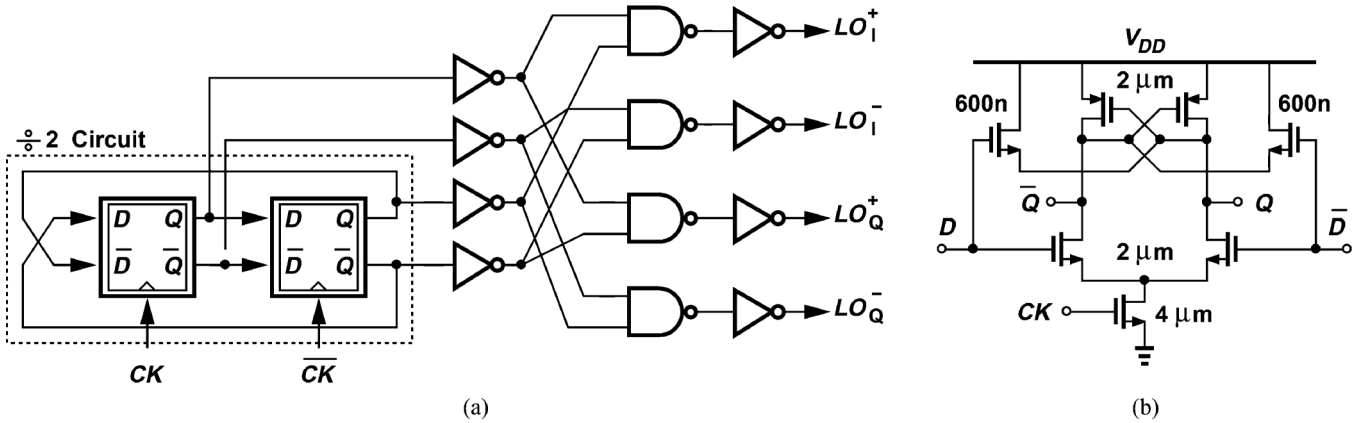


Fig. 5. (a) 25% duty cycle LO generation circuit, (b) latch curcuit used in the divide by 2 (L = 60 nm).

the design of the receiver front end. Our objective is to choose the transformer turns ratio, the mixer transistor widths, and the baseband load so as to achieve (a) proper input matching at the antenna, (b) an acceptable noise figure, and (c) a reasonable voltage gain from the antenna to the baseband outputs of the mixers so as to relax the required noise figure of the baseband chain and hence reduce its power consumption. Our approach consists of two steps: 1) design the transformer for maximum voltage gain with acceptable power loss and input matching when it is matched at the secondary, and 2) design the down-conversion I and Q mixers so as to present proper impedance to the transformer and hence establish this secondary matching.

The optimization of the inductor for loss limits the value of the primary and secondary inductances to about 0.42 nH and 2.9 nH, respectively, yielding a "native" resonance frequency above 10 GHz. Two lumped capacitors of values 950 fF and 55 fF have therefore been added to the primary and secondary, respectively, to allow operation in the 5 GHz range. Due to the distributed nature of the transformer and the high capacitive coupling between the primary and the secondary, it is neither easy nor accurate to model the structure as two mutually-coupled lumped inductors with lumped capacitances. For this reason, these optimizations use simulations with S-parameter models.

To create impedance matching, we model the antenna and the transformer by a Norton equivalent as shown in Fig. 4, where $Z_S = 800\ \Omega$ in the 5 GHz band. The mixers must present a resistance of 800 Ω to the secondary so as to match the receiver input to 50 Ω. However, since this resistance also depends on Z_S, it is more meaningful to ensure that $I_{\rm in}$ sees a resistance of 400 Ω. We therefore return to (13), equate it to this value, and seek the necessary R_{sw}. Due to the bandpass and relatively wideband nature of the transformer and hence Z_S, the summation over k was carried out for about 14 terms, i.e., for harmonic numbers up to 29. Solution of this equation yields $R_{sw} \approx 57\ \Omega$ and a switch aspect ratio of $W/L = 10\mu$m/60 nm.

The dependence of $Z_{\rm in}$ upon the source impedance suggests that the input matching remains relatively intact if the antenna impedance varies to some extent. However, two effects tend to keep the input impedance relatively constant: the resistive loss of the transformer, and the negligible variation of the transformer impedance at the LO harmonics as the antenna impedance varies. This is better understood if we use the simplified model of Fig. 18 for $R_{sw} = 0$. The loss of the transformer translates to a weaker dependence of $Z_s(f_{\rm in})$ upon the antenna impedance. Moreover, due to the bandpass nature of the transformer, $Z_s(f_{\rm in} \pm 4kf_{\rm LO})$ is almost independent of the antenna impedance for $k \neq 0$. Thus, the antenna/receiver matching in our design has about the same sensitivity to the antenna impedance as conventionally-matched systems.

Since the impedance is matched using physical resistances in the transformer and the switches, the receiver's noise figure exceeds 3 dB. Due to its loss, the transformer itself participates in input matching, i.e., the transformer loss of 2.4 dB is in fact part of this 3 dB limit. Similarly, the on-resistance of the switches at all harmonics also contributes to the input matching and to the 3 dB value. Simulations can reveal these effects to some extent: the front end (including the transformer and the mixers) exhibits a noise figure of 4.5 dB with a noisy transformer and 3.3 dB with a noiseless transformer. Simulations also predict a voltage gain of 12 dB, an input $P_{\rm 1dB}$ of -5.2 dBm, and $|S_{11}| > 12$ dB across the 5 GHz band.

For a target receiver NF of less than 6 dB, all of the subsequent stages must contribute no more than 1.5 dB, demanding additional circuit techniques so as to realize low-noise yet linear baseband filters with low power dissipation. The front end reported here does not include automatic gain control (AGC) to attenuate high input levels for the baseband chain, but the gain of the mixers can be readily reduced by inserting small MOSFETs between their differential outputs [24].

VI. LO Generation Circuit

In order to generate 25% duty cycle LO phases, we employ a divide-by-two circuit and some combinational logic. Fig. 5(a) shows the circuit implementation, where the latches used in the divider incorporate additional NMOS source followers so as to improve the speed and reduce the power consumption [Fig. 5(b)] [25]. The inverters and NAND gates are designed to drive 10 μm mixer switches and ensure nonoverlapping LO waveforms. At an LO frequency of 5.5 GHz, the divider, draws 430 μW and the remaining logic 980 μW, while exhibiting a phase noise of -150 dBc/Hz at 1 MHz offset.

VII. Baseband Filter Design

The baseband filters shown in Fig. 2(a) must suppress the blockers according to the 11a standard, present an input noise

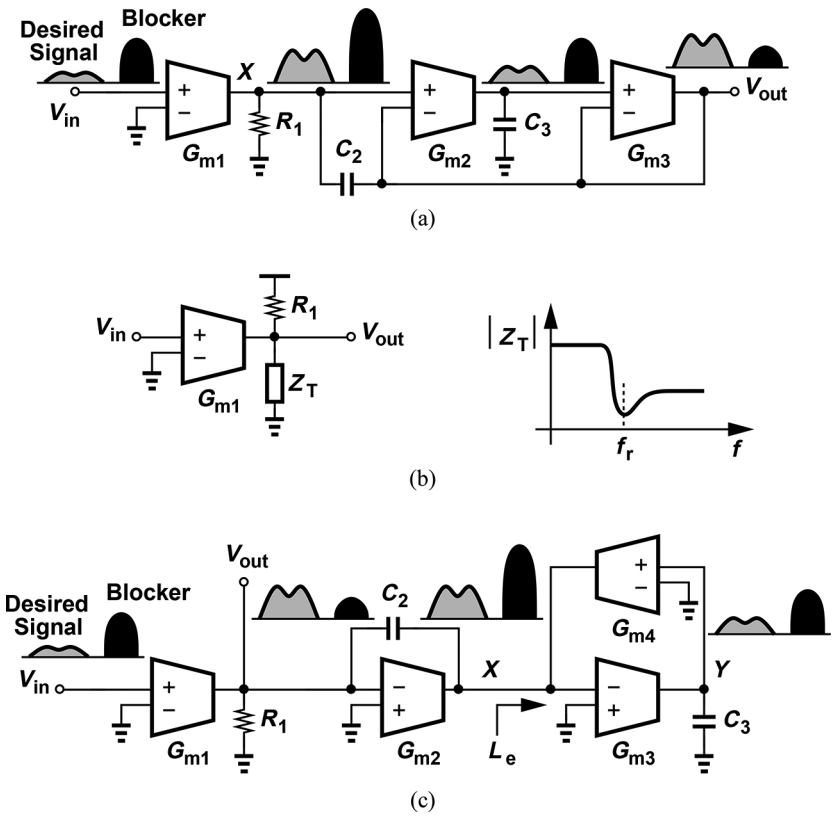


Fig. 6. (a) Conventional implementation of a biquad, (b) basic idea of noninvasive filtering, and (c) noninvasive implementation of a biquad.

much less than the amplified noise of the RF front end, and provide adequate voltage gain. For a data rate of 6 Mb/s, the adjacent and alternate channels can be 16 dB and 32 dB above the desired signal, dictating a high selectivity. The blocker specifications are relaxed by 17 dB for a data rate of 54 Mb/s, but the order of the filter is still determined by the former case. It is possible to defer some of the filtering to the digital domain if the baseband ADCs offer a dynamic range wide enough and a sampling rate high enough to handle the partially-attenuated blockers. In this work, we seek a self-sufficient system and design the filters for complete channel selection.

In OFDM systems, each subcarrier occupies a narrow bandwidth, across which the filter phase response can be assumed linear. Thus, the phase linearity of the baseband filters is not critical in 11a, allowing an elliptic implementation for sharp selectivity. A fifth-order filter satisfies the rejection required in the adjacent and alternate channels, but the challenge is to achieve low noise for signals near the sensitivity level and enough linearity so that the filtration does not degrade in the presence of large blockers. Specifically, a filter input-referred noise of about 4 nV/$\sqrt{\text{Hz}}$ raises the receiver NF from 4.5 dB to 6 dB.

A. Choice of Filter Topology

Let us first consider the G_m-C biquad section shown in Fig. 6(a) [26]. This circuit exhibits the following transfer functions: $V_{\text{out}}/V_{\text{in}} = G_{m1}R_1(s^2 + G_{m2}G_{m3}/C_2C_3)/D$ and $V_X/V_{\text{in}} = G_{m1}R_1[s^2 + (G_{m3}/C_2)s + G_{m2}G_{m3}/C_2C_3]/D$, where $D = (1+G_{m3}R_1)s^2 + (G_{m3}/C_2)s + G_{m2}G_{m3}/C_2C_3$, suggesting that the adjacent-channel blocker can be suppressed in V_{out} but not in V_X. That is, the blocker experiences voltage gain as it travels to X, potentially compressing G_{m1} at its output and G_{m2} at its input.

Two other issues plague the topology of Fig. 6(a). First, G_{m2} contributes noise within the desired channel according to the transfer function $k/(as^2 + bs + 1)$, posing severe noise-linearity-power trade-offs. Second, the differential implementation would require three four-input G_m cells, further exacerbating the noise problem.

The "noninvasive" filter topology introduced in [27] relaxes all of the issues mentioned above. Illustrated conceptually in Fig. 6(b), the idea is to create a notch at the output node by means of a "trap", Z_T, an emulated series LC tank. If the trap frequency, f_r, is placed in the middle of the adjacent channel, then the blocker is heavily suppressed and does not compress G_{m1} at the output. Moreover, since Z_T is nearly an open circuit within the desired channel, it contributes little noise.

Depicted in Fig. 6(c) [27], the actual implementation synthesizes the trap by resonating C_2 with an inductance L_e. This inductance is produced by "rotating" C_3 with the aid of a gyrator consisting of G_{m3} and G_{m4} and is equal to $C_3/(G_{m3}G_{m4})$. The transfer functions associated with this circuit are expressed as $V_{\text{out}}/V_{\text{in}} = G_{m1}R_1[s^2 + G_{m3}G_{m4}/C_2C_3]/E$, $V_X/V_{\text{in}} = G_{m1}R_1[s^2 - (G_{m2}/C_2)s]/E$, and $V_Y/V_{\text{in}} = -(G_{m1}R_1G_{m3}/C_3)(s - G_{m2}/C_2)/E$, where $E = (1+G_{m2}R_1)s^2 + (G_{m3}G_{m4}R_1/C_3)s + G_{m3}G_{m4}/C_2C_3$. Interestingly, the blocker experiences gain as it reaches node X because, roughly speaking, C_2 and L_e act as a series resonant network. This effect will be quantified for the design described below, but we should remark here that compression at node X simply shifts the trap notch frequency and does not affect

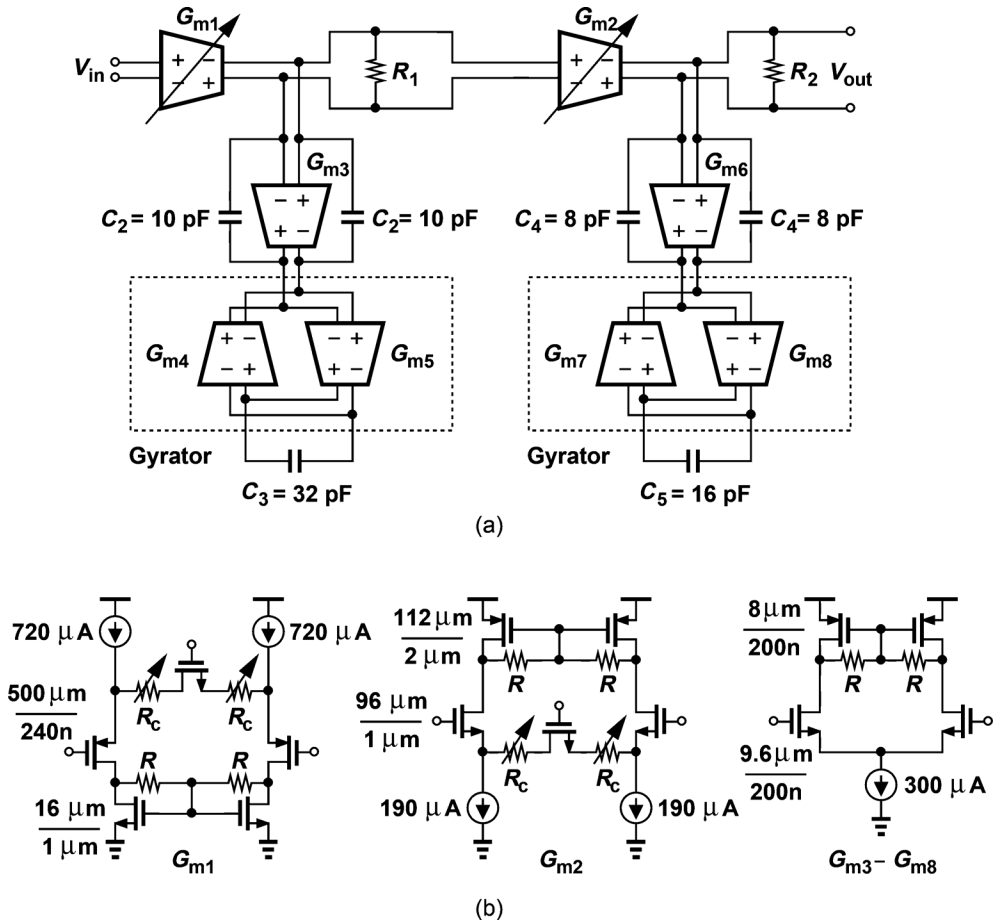


Fig. 7. (a) Fourth-order elliptic low-pass filter, and (b) G_m implementations.

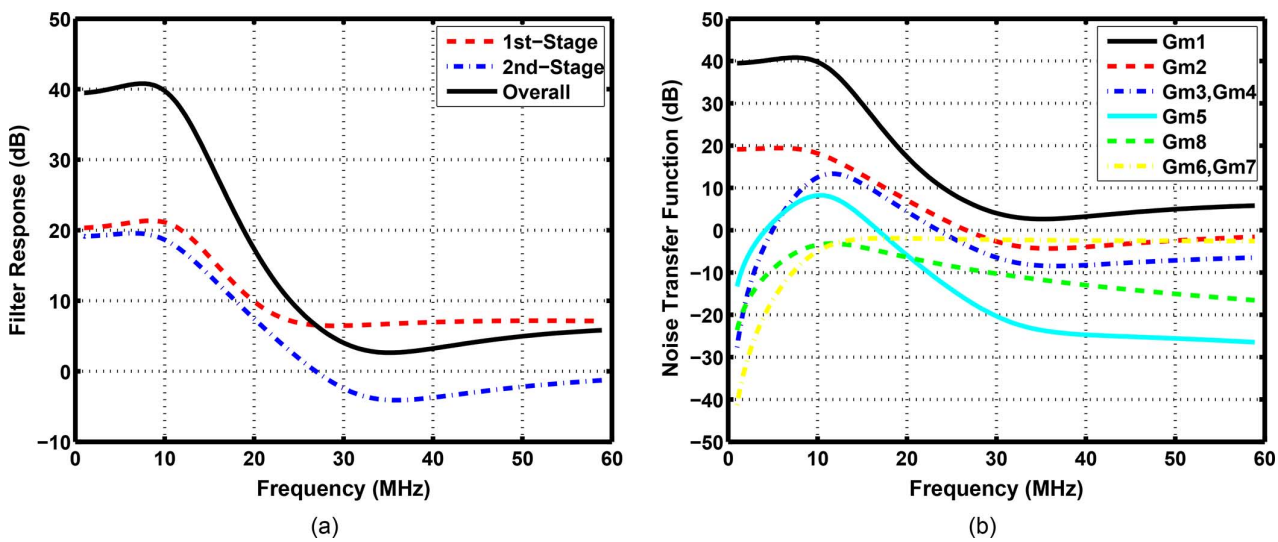


Fig. 8. (a) Transfer function of each stage in the filter and the overall response, and (b) noise transfer functions for all the G_m cells to the output.

the transfer function in the signal band. This can be seen from $L_e = C_3/(G_{m3}G_{m4})$ by noting that reduction of G_{m3} or G_{m4} translates to a greater inductance. We recognize that the noise of G_{m2} and G_{m4} sees a high-pass transfer to V_{out}, and that of G_{m3}, a band-pass transfer. Thus, the output noise principally arises from G_{m1} (and R_1).

B. Filter Implementation

Shown in Fig. 7(a), the overall filter incorporates two cascaded sections, which along with a passive first-order RC section (not shown), achieve the selectivity necessary for 11a. The implementation of the building blocks is depicted in Fig. 7(b).

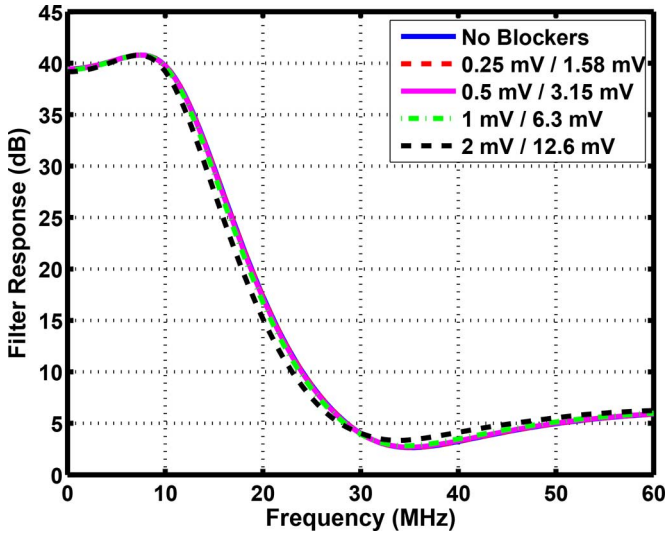


Fig. 9. Filter response in the presence of simultaneous 20 MHz and 40 MHz blockers, with their peak swings shown respectively as first and second values.

The G_{m1} and G_{m2} cells are programmable, allowing gain reduction for high input levels.

Fig. 8(b) plots the simulated noise transfers to the output from the inputs of G_{m1}–G_{m8}, indicating that G_{m3}–G_{m8} contribute negligibly.

Fig. 9 plots $|V_{\rm out}/V_{\rm in}|$ in the presence of several blocker levels in the adjacent and alternate channels. In this simulation, the alternate-channel blocker is 16 dB higher and the peak input voltage swings are shown.[4] We observe that for an alternate-channel blocker level of 12.6 $\rm mV_p$, which corresponds to -40 dBm at the receiver input (with 12 dB of front end gain), the response changes negligibly. This means that an alternate-channel blocker 25 dB higher than the desired signal is tolerable by virtue of noninvasive filtering. For a higher desired and blocker powers, the gain can be reduced.

According to simulations, the filter exhibits an input-referred noise voltage of 2 $\rm nV/\sqrt{Hz}$, an in-channel 1 dB compression point of 7.1 $\rm mV_{pp}$ (in the high-gain mode), and a voltage gain of 39 dB while drawing 4.3 mW. The filter's voltage gain is programmable in steps of 2 to 3 dB for a total range of 43 dB. The present design does not have the provision for frequency tuning, but this can be accomplished by adjusting C_2–C_5 in Fig. 7(a).

VIII. Experimental Results

The receiver of Fig. 2(a) has been fabricated in 65-nm digital CMOS technology. Fig. 10 shows the die photograph. The RF section occupies 350 μm $\times$ 240 μm and the baseband section 450 μm $\times$ 220 μm.[5] The circuit is bonded to a printed-circuit board and operates with a 1-V supply.

Fig. 11(a) plots the measured noise figure of the complete receiver as a function of the baseband frequency. The average noise figure is about 5.3 dB and the rise at low frequencies is due to the flicker noise of the baseband stages. The sensitivity of the receiver is measured with the aid of Agilent's N5182 MXG vector signal generator and N9020A MXA signal analyzer, which respectively apply a 64-QAM 802.11a signal and sense the baseband outputs to construct the signal constellation. Fig. 11(b) shows the results for a -65 dBm 5.7 GHz input at 54 MB/s. The error vector magnitude (EVM) is equal to -28 dB, exceeding the 11a specification by 5 dB, suggesting that the receiver sensitivity would be 5 dB better. As expected, the sensitivity was measured to be -70 dBm with an EVM of -23.4 dB.

Fig. 12(a) plots the S_{11} from 5 to 6 GHz, measured at each input frequency, while the mixers switch at the corresponding LO frequency. It is expected that a slightly larger transformer or adding more capacitance can yield $S_{11} < -10$ dB across the band. Fig. 12(b) shows the sensitivity of the receiver from 5 to 6 GHz. The sensitivity degrades slightly at lower frequencies because the transformer is mistuned. The receiver gain across the band in Fig. 12(c) also confirms the transformer's mistuning.

Fig. 13(a) plots the measured receiver transfer function, revealing a passband peaking of 1 dB and a rejection of 22 dB at 20 MHz and 43 dB at 40 MHz.[6] Owing to the finite output resistance of the G_m cells, the filter does not exhibit the deep notches that are characteristic of elliptic transfer functions. The performance of the baseband filter is ultimately tested when a large blocker accompanies a small desired signal. In such a case, the filter must remain sufficiently selective and linear so that the desired signal does not experience compression. Fig. 13(b) plots the measured passband gain as a function of the power of an RF blocker in the adjacent or alternate adjacent channel.

The filter nonlinearity resulting from a blocker may also corrupt the 11a 64-QAM OFDM signal by creating cross modulation among the sub-channels. This effect is characterized by setting the RF input signal level 3 dB above the sensitivity, applying a blocker, and raising its level until the EVM falls to -23 dB. Fig. 14(a) plots the relative blocker level in this test as a function of the frequency offset with respect to the desired signal center frequency. The non-monotonic behavior observed in these measurements is difficult to explain. One possibility is that it may arise from how the equipment measures the pilot channel in the presence of residual blocker.

Fig. 14(b) shows the measured EVM and the corresponding passband gain versus the input power. As the input level begins to rise from -70 dBm, the EVM is noise-limited and falls but, beyond -25 dBm, it is nonlinearity-limited and rises. The baseband variable gain guarantees an EVM of -23 dB for input levels as high as -17 dBm.

Table I summarizes the receiver performance and compares it to that of prior art. This work has reduced the power consumption by about a factor of 4 while demonstrating a sensitivity of -70 dBm for an 11a 64QAM OFDM signal at 54 Mbps with a code rate of 3/4. The sensitivity is measured at EVM $= -23$ dB, which corresponds to a BER of 10^{-3} [28].

IX. Conclusion

This paper suggests the use of transformers in place of active LNAs to save power and provide ESD protection. The "zero-power" front end consisting of a transformer and

[4]In the 11a specifications, an alternate-channel blocker of -50 dBm must be tolerated when the desired signal is at -65 dBm.

[5]Due to limited silicon area, the receiver layout is decomposed and placed within other unrelated circuits, but all of the connections are present on the chip.

[6]In this measurement a first-order RC section follows each output on the PCB.

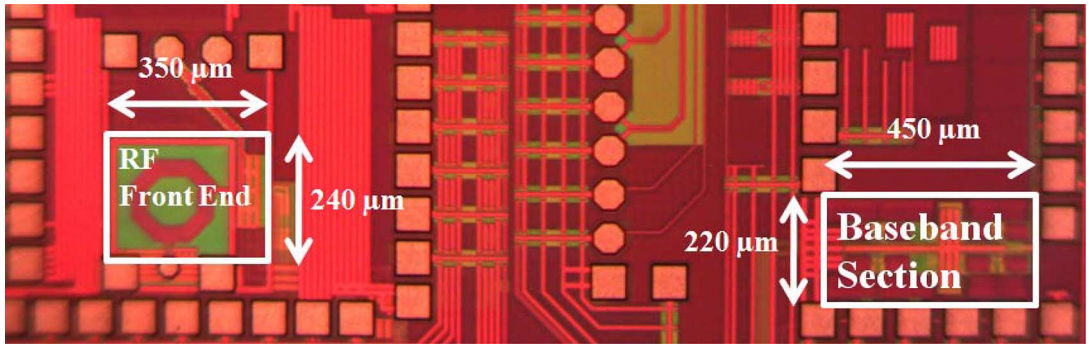
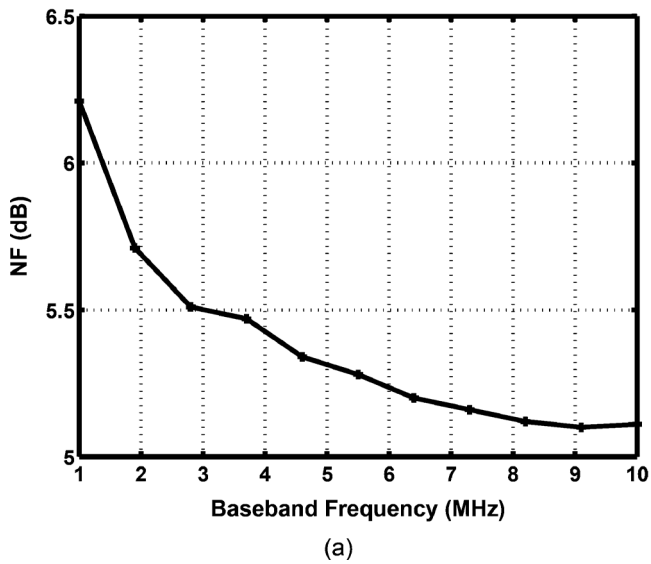


Fig. 10. Die photograph.



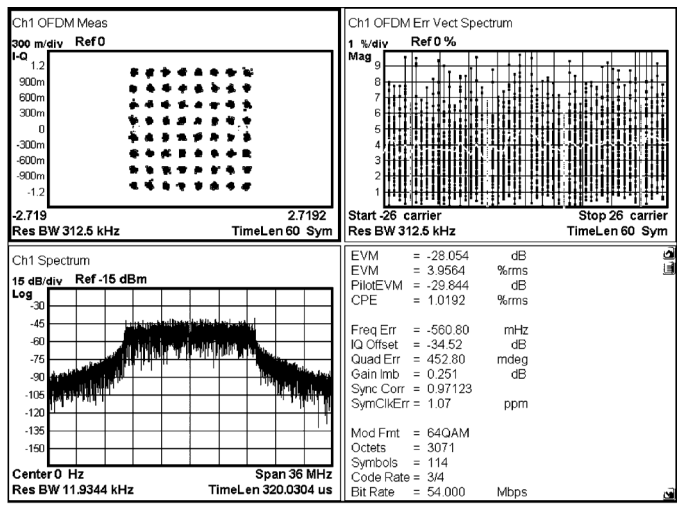


Fig. 11. (a) Measured noise figure, and (b) measured EVM at $P_{\rm in} = -65$ dBm.

passive mixers along with noninvasive filtering exceeds the 11a requirements while consuming 11.6 mW. An analysis of differential passive mixers with 25% duty cycle LO offers insights into their properties.

Appendix A
Analysis of Current-Driven Passive Mixers

We consider Fig. 3 and assume a zero switch resistance for now. The differential I and Q output voltages can be expressed as $V_{\rm out,I}(t) = [I_{\rm mix}(t) \times (S_1 - S_3)] * [2Z_L(t)]$ and $V_{\rm out,Q}(t) = [I_{\rm mix}(t) \times (S_2 - S_4)] * [2Z_L(t)]$, where $Z_L(\rm t)$ denotes the inverse Laplace transform of $Z_L(\rm s)$. The input voltage, $V_{\rm in}$, is equal to $+V_{\rm out,I}$ when S_1 is high, $-V_{\rm out,I}$ when S_3 is high, etc., assuming the form $V_{\rm in}(t) = V_{\rm out,I}(t) \times (S_1 - S_3) + V_{\rm out,Q}(t) \times (S_2 - S_4)$. Substituting for $V_{\rm out,I}$ and $V_{\rm out,Q}$ and taking the Fourier transform, we have

$$V_{\rm in}(f) = 2\{[I_{\rm mix} * (S_1 - S_3)] \times Z_L\} * (S_1 - S_3) + 2\{[I_{\rm mix} * (S_2 - S_4)] \times Z_L\} * (S_2 - S_4) \quad (1)$$

where the quantities on the right-hand side are frequency-domain representations. This equation is the differential form of that in [22] and plays a central role in our analysis, drawing upon the time-domain and frequency-domain characteristics of the $S_1 - S_3$ and $S_2 - S_4$ waveforms. As shown in Fig. 15, the spectra of these two functions contain odd harmonics with an envelope similar to that of a simple square wave. (The 90° time shift in $S_2 - S_4$ produces a factor of j in its spectrum.) More accurately,

$$S_1(f) - S_3(f) = \sum_{k=-\infty}^{\infty} \frac{2\sin[(2k+1)\pi/4]}{(2k+1)\pi} \times \delta[f - (2k+1)f_{\rm LO}], \quad (2)$$

$$S_2(f) - S_4(f) = -j \sum_{k=-\infty}^{\infty} \frac{(-1)^k 2\sin[(2k+1)\pi/4]}{(2k+1)\pi} \times \delta[f - (2k+1)f_{\rm LO}]. \quad (3)$$

The derivations have thus far considered general source and load impedances. A number of special cases are of particular interest for their simplicity or applicability: (1) Z_S can be infinite, a real value, or a band-pass impedance, and (2) Z_L can be a capacitor. In addition, the switches can have a zero or finite resistance. We first assume $Z_S = \infty$ and derive characteristics such as the input impedance and conversion gain and study the effect of switch resistance. Next, we assume $Z_S < \infty$ and extend the results.

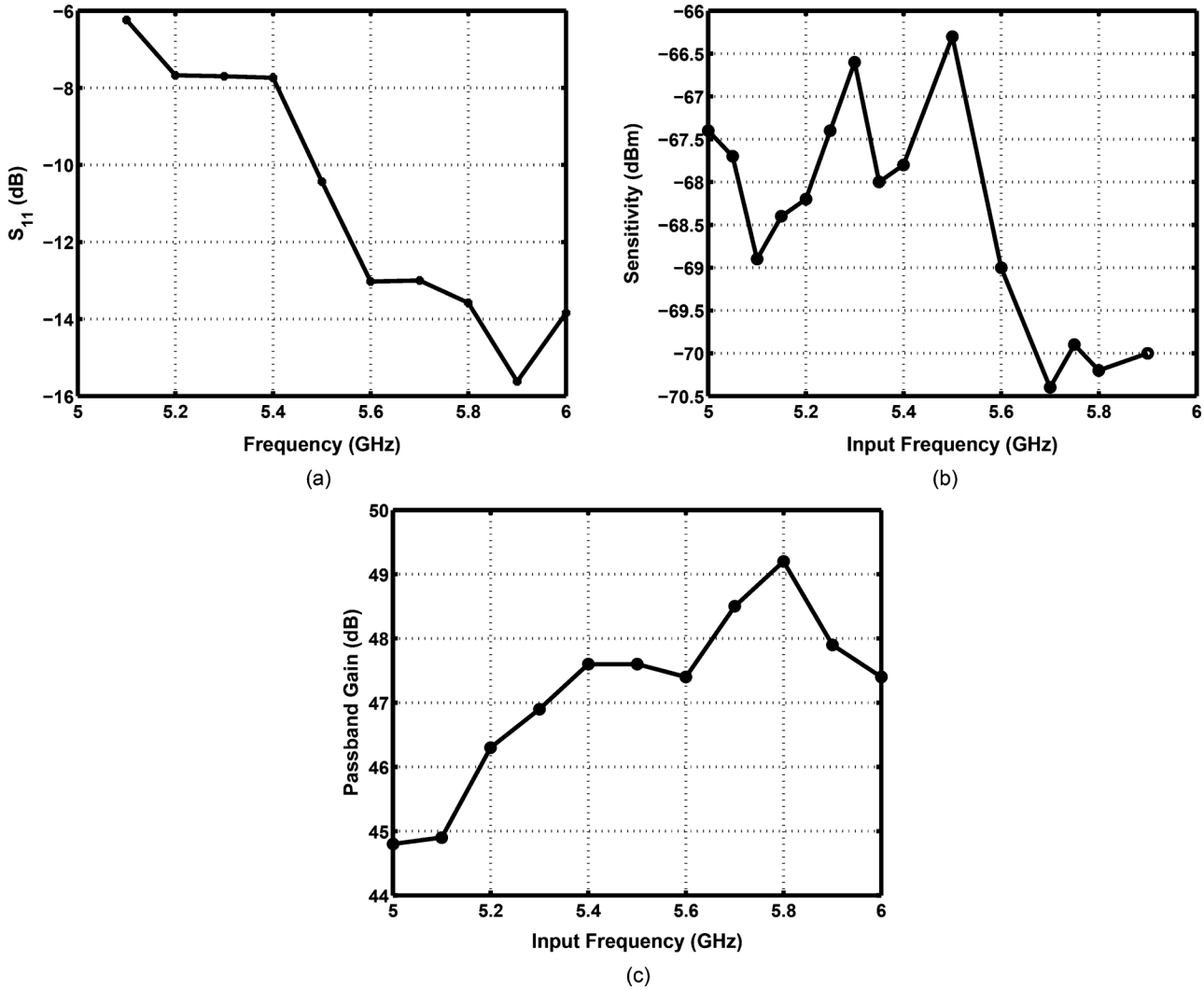


Fig. 12. Measured (a) input return loss, (b) sensitivity, and (c) passband gain.

Suppose $Z_S = \infty$ and the input current in Fig. 3(a) is a sinusoid at $f_{\rm in}$. Thus, $I_{\rm mix}(= I_{\rm in})$ is also a single tone, which, upon experiencing the operations in (1), shifts up and down in frequency. We seek all mechanisms that shift an input at $f_{\rm in}$ back to $f_{\rm in}$ after the two convolutions with $S_1 - S_3$ or $S_2 - S_4$ take effect. We first consider only the impulse at $+f_{\rm in}$, i.e., assume $I_{\rm mix} = \delta(f - f_{\rm in})$. It follows from (2) that

$$[I_{\rm mix} * (S_1 - S_3)] \times Z_L(f) = \frac{2}{\pi} \sum_{k=-\infty}^{\infty} \frac{\sin[(2k+1)\pi/4]}{(2k+1)} \delta[f - f_{\rm in} - (2k+1) f_{\rm LO}] Z_L[f_{\rm in} + (2k+1) f_{\rm LO}]. \quad (4)$$

Referring to (1), we multiply the result by 2 and convolve it with $S_1 - S_3$, and choose the frequency components that are equal to $f_{\rm in}$:

$$2\{[I_{\rm mix} * (S_1 - S_3)] \times Z_L\} * (S_1 - S_3)(f_{\rm in}) = \frac{4}{\pi^2} \sum_{k=-\infty}^{\infty} \frac{\delta(f - f_{\rm in})}{(2k+1)^2} Z_L[f_{\rm in} + (2k+1) f_{\rm LO}]. \quad (5)$$

The second term in (1) can be obtained in a similar manner, and the calculations can be repeated for $I_{\rm mix} = \delta(f + f_{\rm in})$. We thus obtain the input impedance in the vicinity of $f_{\rm in}$ as

$$Z_{\rm mix}(f_{\rm in}) = \frac{8}{\pi^2} \left[\frac{1}{1^2} Z_L(f_{\rm in} \pm f_{\rm LO}) + \frac{1}{3^2} Z_L(f_{\rm in} \pm 3 f_{\rm LO}) + \frac{1}{5^2} Z_L(f_{\rm in} \pm 5 f_{\rm LO}) + \cdots \right] \quad (6)$$

which is twice that reported in [22] and [23]. It is interesting to note that the input impedance consists of the *series* combination of translated copies of Z_L. This occurs because voltage components at $f_{\rm in}$, which are created by the *same* current source, add. In the special case of $Z_L(f) = R_L$, the infinite sum in (6) converges to $Z_{\rm mix}(f_{\rm in}) = 2R_L$, an expected result because the input source does not recognize that the resistors are switched when the circuit contains no memory.

The conversion gain can be defined as the intermediate-frequency (IF) voltage (at the I or Q output) divided by the RF input current or by the RF input voltage. We compute the LO fundamental amplitude in $S_1 - S_3$ as $\sqrt{2}/\pi$ and write the transimpedance gain as $A_R = 2\sqrt{2}/\pi Z_L(f_{\rm in} - f_{\rm LO})$. To obtain the

TABLE I
COMPARISON WITH STATE-OF-THE-ART

	This Work	[7]	[29]	[30]
Frequency (GHz)	5.1 – 5.9	5.15 – 5.35	4.9 – 5.95	5.1 – 5.9
NF (dB)	5.3	8.0	4.4	5.5
IIP_3 (dBm)	+ 2.6	−11.2	+ 5	+ 16
Gain (dB)	5 – 48	14 – 94.5	8 – 74	19 – 89
Sensitivity (dBm) at 54 Mb/s	−70	NA	NA	−75.5
LO Leakage (dBm) at 5.5 GHz	−60	NA	NA	NA
Power (mW)	11.6	46	108*	72.7**
LNA	0	11.7		
Mixers	0	9.8		
LO Buffers	0.4	10.8		
Filters, VGAs	10	13.7		
Divider/ 25% Logic	1.2			
CMOS Process	65 nm	0.18 μm	0.18 μm	0.13 μm
Area (mm^2)	0.183	NA	NA	NA

* Including ADC.

** Without LO Buffer.

voltage conversion gain, we divide A_R by the input impedance at $f = f_{\rm in}$:

$$A_V = \frac{\sqrt{2}\pi}{4} \cdot \frac{Z_L(f_{\rm in}-f_{\rm LO})}{Z_L(f_{\rm in}\pm f_{\rm LO})+\frac{1}{3^2}Z_L(f_{\rm in}\pm 3f_{\rm LO})+\frac{1}{5^2}Z_L(f_{\rm in}\pm 5f_{\rm LO})+\cdots}. \tag{7}$$

This voltage gain reduces to $\sqrt{2}\pi/4$ (≈0.9 dB) [15] and $\sqrt{2}/\pi$ (≈ −6.9 dB) for capacitive and resistive loads, respectively. Note that passive mixers with capacitive loads provide positive conversion gain.

The effect of the switch resistance, R_{sw}, can be included with the aid of Fig. 16, where R_{sw} is "factored out" and placed in series with the input source [31]. In other words, the input impedance is now equal to that given by (6) plus $2R_{sw}$. The transimpedance gain remains the same, but the voltage conversion gain is revised to (8), shown at the bottom of the page. With $Z_S < \infty$ in Fig. 3(a), $I_{\rm mix} = I_{\rm in} - V_{\rm in}/Z_S$, complicating the derivations because $V_{\rm in}$ contains components around odd harmonics of $f_{\rm LO}$ and so does $I_{\rm mix}$. We begin with $R_{sw} = 0$ and observe that (1) still holds. Fig. 17 illustrates the problem that we must solve. A unit input current near $\pm f_{\rm LO}$ is shifted up and down by multiples of $4f_{\rm LO}$, generating new components in $I_{\rm mix}(f)$ and $V_{\rm in}(f)$. Using (1), we wish to compute a_j and b_j and hence express the input impedance as $Z_{\rm in}(f_{\rm in}) = V_{\rm in}(f_{\rm in})/I_{\rm in}(f_{\rm in}) = b_1$. This task is pursued in Appendix II, yielding

$$Z_{\rm in}(f_{\rm in}) = \frac{\frac{8}{\pi^2}Z_L(f_{\rm in}-f_{\rm LO})}{1+\frac{8}{\pi^2}Z_L(f_{\rm in}-f_{\rm LO})\sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2 Z_S(f_{\rm in}+4kf_{\rm LO})}} \tag{9}$$

which is the same as those in [22] and [23]. Here, we have assumed $Z_L(f)$ is band-limited and neglected its translated copies.

Equation (9) can be rewritten as

$$\frac{1}{Z_{\rm in}(f_{\rm in})} = \frac{1}{\frac{8}{\pi^2}Z_L(f_{\rm in}-f_{\rm LO})} + \cdots + \frac{1}{7^2 Z_S(f_{\rm in}-8f_{\rm LO})} + \frac{1}{3^2 Z_S(f_{\rm in}-4f_{\rm LO})} + \frac{1}{Z_S(f_{\rm in})} + \frac{1}{5^2 Z_S(f_{\rm in}+4f_{\rm LO})} + \frac{1}{9^2 Z_S(f_{\rm in}+8f_{\rm LO})} + \cdots. \tag{10}$$

Illustrated in Fig. 18, $Z_{\rm in}$ is equal to $(8/\pi^2)Z_L(f_{\rm in} - f_{\rm LO})$ *in parallel* with $Z_S(f_{\rm in})$ and its translated and scaled copies [19].

To include the effect of switch resistance, we replace $I_{\rm in}$, Z_S, and the two R_{sw}'s with their Norton equivalent, arriving at an input current equal to $I_{\rm in}Z_S/(Z_S + 2R_{sw})$ and a source impedance equal to $Z_S + 2R_{sw}$. We therefore replace Z_S in (9) with $Z_S + 2R_{sw}$ and write the result as shown in (11) at the bottom of the page. In the original circuit, $V_{\rm in} = V_{\rm mix} + 2R_{sw}I_{\rm mix}$ and $I_{\rm mix} = I_{\rm in} - V_{\rm in}/Z_S$, yielding $V_{\rm in}/I_{\rm in}$ as shown in (12) at the bottom of the next page, which agrees with those in [22] and [23]. Fig. 3(b) shows the equivalent impedance in

$$A_V = \frac{(2\sqrt{2}/\pi)Z_L(f_{\rm in}-f_{\rm LO})}{2R_{sw}+(8/\pi^2)\left[Z_L(f_{\rm in}\pm f_{\rm LO})+\frac{1}{3^2}Z_L(f_{\rm in}\pm 3f_{\rm LO})+\frac{1}{5^2}Z_L(f_{\rm in}\pm 5f_{\rm LO})+\cdots\right]}. \tag{8}$$

$$V_{\rm mix}(f) = I_{\rm in}\frac{Z_S}{Z_S+2R_{sw}} \times \frac{\frac{8}{\pi^2}Z_L(f_{\rm in}-f_{\rm LO})}{1+\frac{8}{\pi^2}Z_L(f_{\rm in}-f_{\rm LO})\sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2[Z_S(f_{\rm in}+4kf_{\rm LO})+2R_{sw}]}} \tag{11}$$

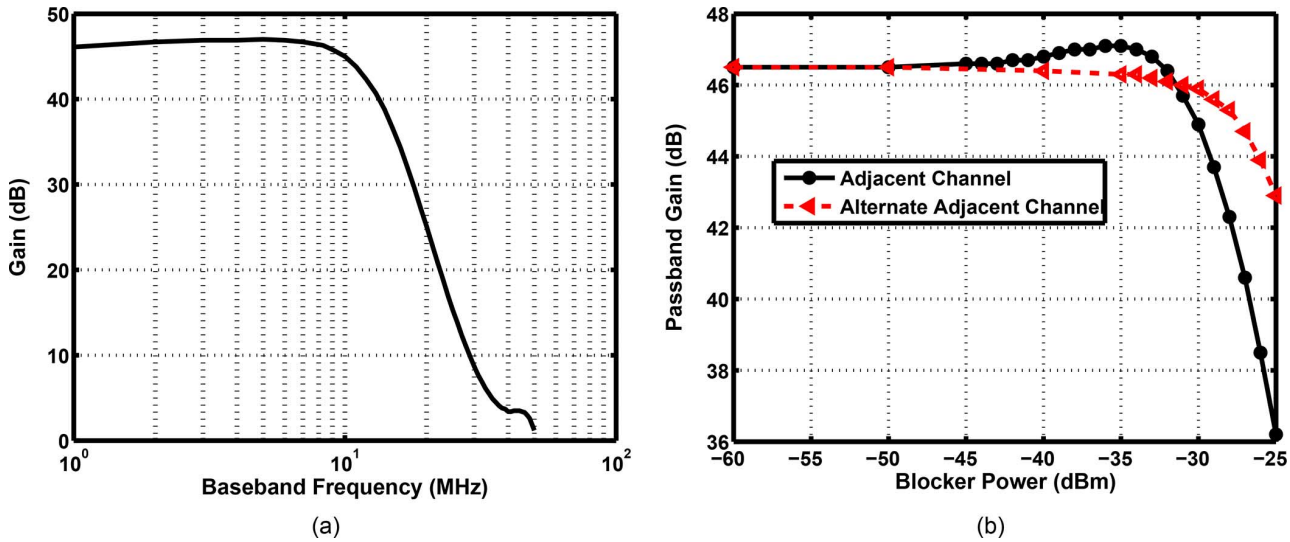


Fig. 13. Measured (a) receiver transfer function, and (b) passband gain in the presence of a blocker.

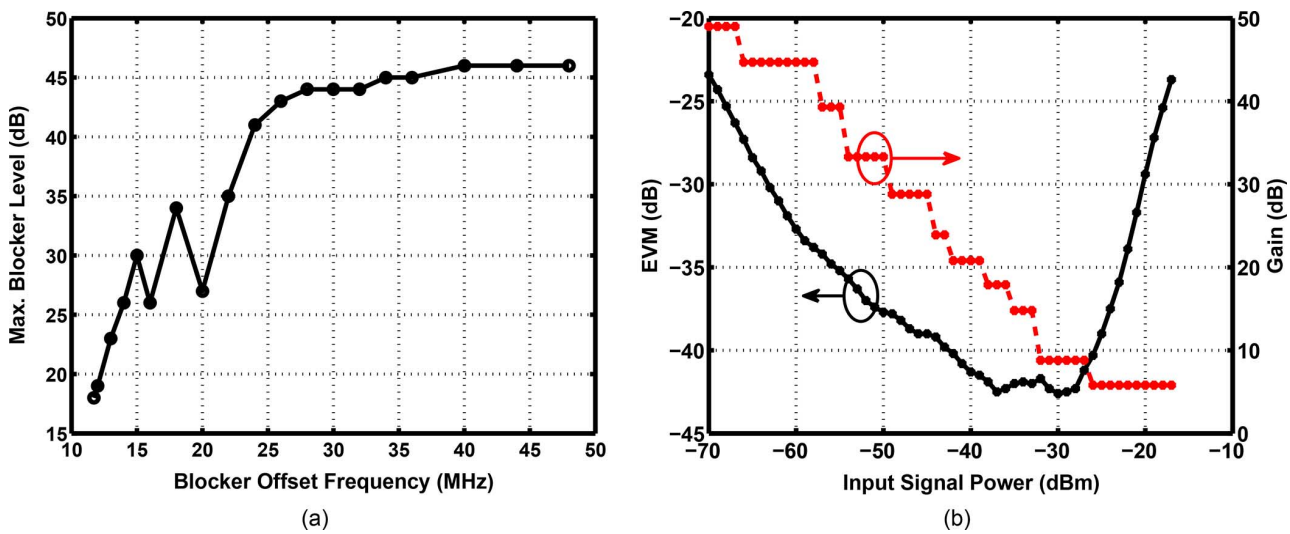


Fig. 14. Measured (a) maximum blocker level for EVM $= -23$ dB, (b) EVM and passband gain versus input power.

this case. For a capacitive load, $Z_L(f_{\rm in}-f_{\rm LO})$ is large and the second term in the denominator of (12) is dominant, yielding

$$Z_{\rm in}(f_{\rm in}) = Z_S(f_{\rm in})\|(2R_{sw}) + \left[\frac{Z_S(f_{\rm in})}{Z_S(f_{\rm in})+2R_{sw}}\right]^2 \div \sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2[Z_S(f_{\rm in}+4kf_{\rm LO})+2R_{sw}]}. \quad (13)$$

The transimpedance and voltage gains for a capacitive load and $R_{sw}\neq 0$ can be calculated as follows. In Fig. 3(a), $I_{\rm mix}=V_{\rm in}(Z_S-Z_{\rm in})/Z_SZ_{\rm in}$. Also, the low-frequency output in Fig. 16, $V_{{\rm out},I}$, is upconverted with a gain of $2\sqrt{2}/\pi$ and added to $2R_{sw}I_{\rm mix}$ to generate $V_{\rm in}$ in the vicinity of $f_{\rm LO}$. We thus have $A_{V,{\rm cap}}=(\sqrt{2}\pi/4)(1+2R_{sw}/Z_S-2R_{sw}/Z_{\rm in})$. The transimpedance gain, A_R, is equal to $A_{V,cap}\times Z_{\rm in}$, where $Z_{\rm in}$ is expressed in (13).

We now compute the noise figure of the circuit shown in Fig. 3, assuming that Z_S is a resistor, R_S, and Z_L a capacitor, C_L.

Suppose $R_{sw}=0$ for now. If $I_{\rm in}$ denotes the rms value of the input current, the signal-to-noise ratio at the input is given by ${\rm SNR}_{\rm in}=I_{\rm in}^2/(4kT/R_S)$. The signal and the noise around $f_{\rm LO}$ are downconverted with the same transimpedance gain, A_R. However, the noise around the nth harmonic of $f_{\rm LO}$ (n is an odd

$$Z_{\rm in}(f_{\rm in}) = Z_S(f_{\rm in})\|(2R_{sw})+\left[\frac{Z_S(f_{\rm in})}{Z_S(f_{\rm in})+2R_{sw}}\right]^2\times\frac{\frac{8}{\pi^2}Z_L(f_{\rm in}-f_{\rm LO})}{1+\frac{8}{\pi^2}Z_L(f_{\rm in}-f_{\rm LO})\sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2[Z_S(f_{\rm in}+4kf_{\rm LO})+2R_{sw}]}} \quad (12)$$

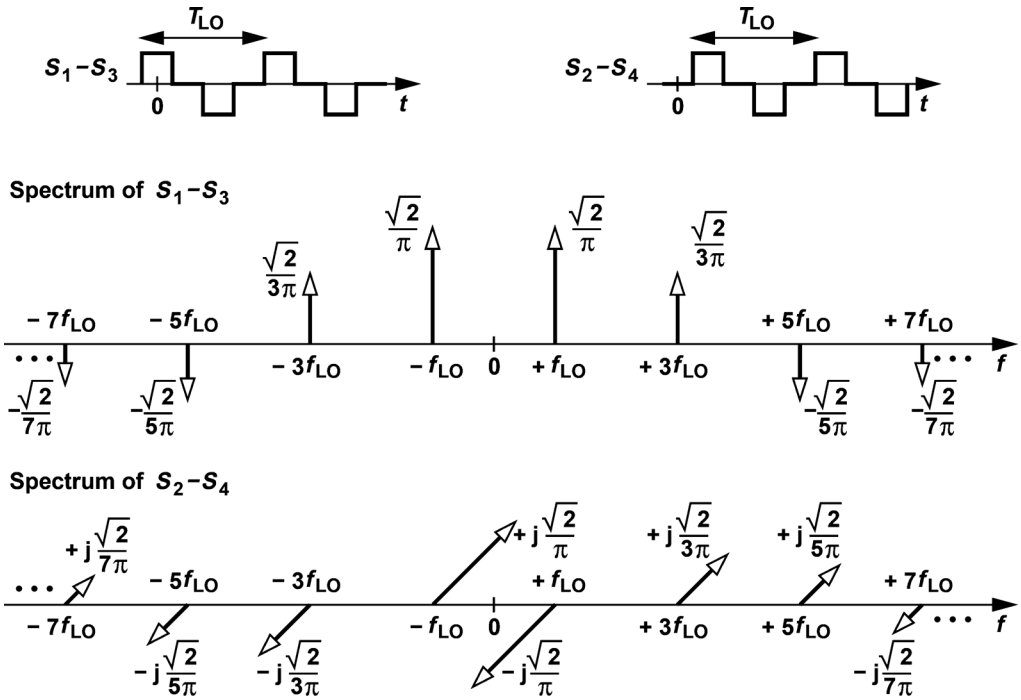


Fig. 15. Switching functions $S_1 - S_3$ and $S_2 - S_4$ in time and frequency domains.

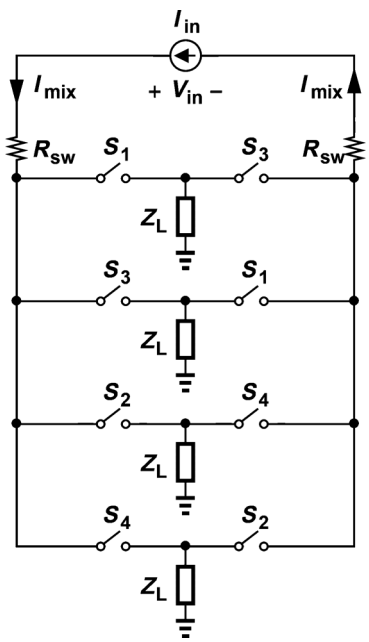


Fig. 16. Moving the switch resistance to the main path.

integer) also folds down with a gain of A_R/n [11]. The output SNR is thus equal to $\text{SNR}_{\text{out}} = I_{\text{in}}^2 A_R^2/[(4kT/R_S)A_R^2(1 + 1/3^2 + 1/5^2 + \cdots)]$, where we have assumed direct conversion and hence a double-sideband (DSB) signal. It follows that the DSB NF is $\text{NF} = \pi^2/8 \approx 0.9$ dB. This is the lower bound on the noise figure of a current-driven quadrature downconverter with 25% duty cycle, simply arising from the aliasing of the broadband noise of R_S. If $R_{sw} > 0$, then I_{in}^2 is scaled by a factor of $R_S^2/(R_S + R_{sw})^2$ while the total noise current is $4kT/(R_S + 2R_{sw})$, yielding $\text{NF} = (\pi^2/8)(1 + 2R_{sw}/R_S)$. This result is similar to that in [11] (for a single-ended input) except for the factor of 2 that appears before R_{sw}.

Finally, we determine the NF with a band-pass source impedance that reduces to R_S in the vicinity of f_{LO}. For a narrow-band input channel around f_{LO}, the input SNR and the output signal power remain the same as before, but the downconverted noise changes to

$$\begin{aligned}\overline{V_{n,out}^2} &= \left\{\frac{4kTR_S^2}{R_S(R_S+2R_{sw})^2} + \frac{4kT(2R_{sw})}{(R_S+2R_{sw})^2}\right\}A_R^2 \\ &+ \left\{\frac{4kT|Z_S(3f_{\text{LO}})|^2}{R_S|Z_S(3f_{\text{LO}})+2R_{sw}|^2} + \frac{4kT(2R_{sw})}{|Z_S(3f_{\text{LO}})+2R_{sw}|^2}\right\}\frac{A_R^2}{9} \\ &+ \left\{\frac{4kT|Z_S(5f_{\text{LO}})|^2}{R_S|Z_S(5f_{\text{LO}})+2R_{sw}|^2} + \frac{4kT(2R_{sw})}{|Z_S(5f_{\text{LO}})+2R_{sw}|^2}\right\} \\ &\times \frac{A_R^2}{25} + \cdots. \end{aligned} \tag{14}$$

The noise figure is expressed as

$$\begin{aligned}\text{NF} &= \left(1 + \frac{2R_{sw}}{R_S}\right)^2 \\ &\times \sum_{k=0}^{+\infty} \frac{1}{(2k+1)^2} \frac{\left|Z_S^2[(2k+1)f_{\text{LO}}]\right| + 2R_{sw}R_S}{\left|Z_S[(2k+1)f_{\text{LO}}] + 2R_{sw}\right|^2}. \end{aligned} \tag{15}$$

As a special case, suppose Z_S is a parallel RLC tank resonating at f_{LO} and with a sufficiently high Q that $Z_S[(2k+1)f_{\text{LO}}]$ can be neglected in (15) for $k > 0$. The NF then simplifies to

$$\text{NF}_{\text{RLC}} = 1 + \frac{2R_{sw}}{R_S} + \left(\frac{\pi^2}{8} - 1\right)\left(2 + \frac{2R_{sw}}{R_S} + \frac{R_S}{2R_{sw}}\right). \tag{16}$$

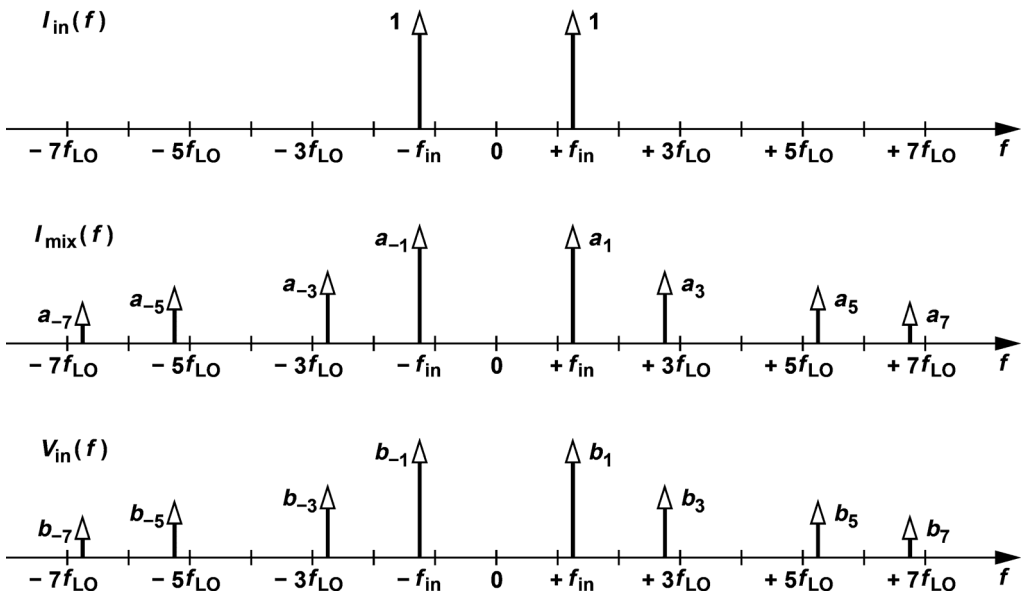


Fig. 17. A single-tone current applied at the input and the resultant spectrum of the mixer input current and voltage.

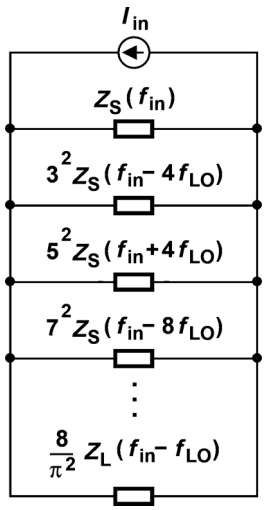


Fig. 18. Input impedance illustration for $R_{sw} = 0$.

The minimum NF occurs for $R_{sw} = \sqrt{\pi^2 - 8}/(2\pi)R_S \approx 0.218R_S$. In this case, $\mathrm{NF}_{\min} = 2.54 \approx 4.05$ dB, which agrees with [19].

Appendix B
Input Impedance With Finite Z_S

Two equations govern the circuit of Fig. 3(a): (1) and $I_{\mathrm{mix}} = I_{\mathrm{in}} - V_{\mathrm{in}}/Z_S$. The former allows us to express the b coefficients in Fig. 17 in terms of the a coefficients. We have

$$b_1 = 2\left(\frac{\sqrt{2}}{\pi}\right)^2 \times 2Z_L(f - f_{\mathrm{LO}}) \times \left[a_1 + \frac{a_{-3}}{3} + \frac{a_5}{-5} + \frac{a_{-7}}{-7} + \frac{a_9}{9} + \cdots\right]. \quad (17)$$

Note that b_1 is in fact the input impedance in the vicinity of f_{LO}. Similarly, $b_{-3} = b_1/3$, $b_5 = b_1/(-5)$, $b_{-7} = b_1/(-7)$, etc. Moreover, $I_{\mathrm{mix}} = I_{\mathrm{in}} - V_{\mathrm{in}}/Z_S$ yields $a_1 = 1 - b_1/Z_s(f)$, $a_{-3} = -b_{-3}/Z_s(f - 4f_{\mathrm{LO}})$, $a_5 = -b_5/Z_s(f + 4f_{\mathrm{LO}})$, etc. Substituting for the b values, we have $a_{-3} = (a_1 - 1)Z_S(f)/[3Z_S(f - 4f_{\mathrm{LO}}]$, $a_5 = (a_1 - 1)Z_S(f)/[-5Z_S(f - 4f_{\mathrm{LO}}]$, etc.

Next, we write $a_1 = 1 - b_1/Z_s(f)$ and substitute for b_1 from (17) and a_{-3} and a_5 from the above, arriving at

$$a_1 = 1 - \frac{1}{Z_s(f)}\frac{8}{\pi^2}Z_L(f - f_{\mathrm{LO}}) \times \left[1 + (a_1 - 1)\frac{Z_s(f)}{Z_s(f)} + (a_1 - 1)\frac{Z_s(f)}{9Z_s(f - 4f_{\mathrm{LO}})} + (a_1 - 1)\frac{Z_s(f)}{25Z_s(f + 4f_{\mathrm{LO}})} + \cdots\right]. \quad (18)$$

It follows that

$$(a_1 - 1)\left[1 + \frac{8}{\pi^2}Z_L(f - f_{\mathrm{LO}}) \times \sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2 Z_s(f + 4kf_{\mathrm{LO}})}\right] = -\frac{8}{\pi^2}\frac{Z_L(f - f_{\mathrm{LO}})}{Z_s(f)}. \quad (19)$$

Since $Z_{\mathrm{in}} = b_1 = -(a_1 - 1)Z_s(f)$, we have

$$Z_{\mathrm{in}}(f) = \frac{\frac{8}{\pi^2}Z_L(f - f_{\mathrm{LO}})}{1 + \frac{8}{\pi^2}Z_L(f - f_{\mathrm{LO}})\sum_{k=-\infty}^{\infty}\frac{1}{(4k+1)^2 Z_s(f + 4kf_{\mathrm{LO}})}}. \quad (20)$$

Acknowledgment

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References

[1] S. Levantino *et al.*, "Suppression of flicker noise upconversion in a 65 nm CMOS VCO in the 3.0-to-3.6 GHz band," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 50–51.

[2] L. Fanori, T. Mattsson, and P. Andreani, "A 2.4-to-5.3 GHz dual-core CMOS VCO with concentric 8-shaped coils," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2014, pp. 370–371.
[3] S. Rong, A. W. L. Ng, and H. C. Luong, "0.9 mW 7 GHz and 1.6 mW 60 GHz frequency dividers with locking-range enhancement in 0.13 μm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 96–97.
[4] S. Cheng *et al.*, "A fully differential low-power divide-by-8 injection-locked frequency divider up to 18 GHz," *IEEE J. Solid-State Circuits*, vol. 42, no. 3, pp. 583–591, Mar. 2007.
[5] Y. Zhu *et al.*, "A 50-fJ 10-b 160-MS/s pipelined-SAR ADC decoupled flip-around MDAC and self-embedded offset cancellation," *IEEE J. Solid-State Circuits*, vol. 47, no. 11, pp. 2614–2626, Nov. 2012.
[6] S. Hashemi and B. Razavi, "A 7.1 mW 1-GS/s ADC with 48-dB SNDR at Nyquist rate," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2013.
[7] L. L. L. Kan *et al.*, "A 1-V 86 mW RX 53 mW TX single-chip CMOS transceiver for WLAN IEEE 802.11a," *IEEE J. Solid-State Circuits*, vol. 42, no. 9, pp. 1986–1998, Sep. 2007.
[8] N.-Y. Wang *et al.*, "A 60 dB gain and 4 dB noise figure CMOS V-band receiver based on two-dimensional passive Gm-enhancement," in *IEEE RFIC Symp.*, Jun. 2011, pp. 65–68.
[9] H. Wu *et al.*, "A current-mode mm-wave direct-conversion receiver with 7.5 GHz Bandwidth, 3.8 dB minimum noise-figure and +1 dBm P1 dB, out linearity for high data rate communications," in *IEEE RFIC Symp. Dig.*, Jun. 2013, pp. 89–92.
[10] A. Mirzaei *et al.*, "A 65 nm CMOS quad-band SAW-less receiver SoC for GSM/GPRS/EDGE," *IEEE J. Solid-State Circuits*, vol. 46, no. 4, pp. 950–964, Apr. 2011.
[11] B. W. Cook *et al.*, "Low-power 2.4 GHz transceiver with passive RX front-end and 400-mV supply," *IEEE J. Solid-State Circuits*, vol. 41, no. 12, pp. 2757–2766, Dec. 2006.
[12] J. R. Long, "Monolithic transformers for silicon RF IC design," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1368–1383, Sep. 2000.
[13] K. Cai and P. Zhang, "The effects of IP2 impairment on an 802.11a OFDM direct conversion radio system," *Microwave J.*, vol. 47, pp. 22–35, Feb. 2004.
[14] M. Soer *et al.*, "A 0.2-to-2.0 GHz 65 nm CMOS receiver without LNA achieving $>$11 dBm IIP3 and $<$6.5 dB NF," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2009, pp. 222–223.
[15] D. Kaczman *et al.*, "A single-chip 10-band WCDMA/HSDPA 4-band GSM/EDGE SAW-less CMOS receiver with DigRF 3 G interface and +90 dBm IIP2," *IEEE J. Solid-State Circuits*, vol. 44, no. 3, pp. 718–739, Mar. 2009.
[16] A. Mirzaei and H. Darabi, "Analysis of imperfections on performance of 4-phase passive-mixer-based high-Q bandpass filters in SAW-less receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 879–892, May 2011.
[17] A. Mirzaei *et al.*, "Analysis and optimization of direct-conversion receivers with 25% duty-cycle current-driven passive mixers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 9, pp. 2353–2366, Sep. 2010.
[18] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable RF interface," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2696–2708, Dec. 2010.
[19] C. Andrews and A. C. Molnar, "Implications of passive mixer transparency for impedance matching and noise figure in passive mixer-first receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 12, pp. 3092–3103, Dec. 2010.
[20] A. Molnar and C. Andrews, "Impedance, filtering and noise in n-phase passive CMOS mixers," in *Proc. IEEE Custom Integrated Circuits Conf. (CICC)*, Sep. 2012.
[21] M. Soer *et al.*, "Unified frequency-domain analysis of switched-series-RC passive mixers and samplers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 10, pp. 2618–2631, Oct. 2010.
[22] A. Mirzaei, H. Darabi, and D. Murphy, "Architectural evolution of integrated M-phase high-Q bandpass filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 59, no. 1, pp. 52–65, Jan. 2012.
[23] H. Darabi and A. Mirzaei, *Integration of Passive RF Front End Components in SoCs*. Cambridge, U.K.: Cambridge, 2013.
[24] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice-Hall, 2011.
[25] J. W. Jung and B. Razavi, "A 25-Gb/s 5 mW CMOS CDR/deserializer," *IEEE J. Solid-State Circuits*, vol. 48, no. 3, pp. 684–697, Mar. 2013.
[26] R. L. Geiger and E. Sanchez-Sinencio, "Active filter design using operational transconductance amplifiers: A tutorial," *IEEE Circuits Devices Mag.*, vol. 1, no. 2, pp. 20–32, Mar. 1985.
[27] A. Zolfaghari and B. Razavi, "A low-power 2.4 GHz transmitter/receiver CMOS IC," *IEEE J. Solid-State Circuits*, vol. 38, no. 2, pp. 176–183, Feb. 2003.
[28] R. A. Shafik, S. Rahman, and R. Islam, "On the extended relationships among EVM, BER and SNR as performance metrics," in *Proc. IEEE ICECE*, Dec. 2006, pp. 408–411.
[29] T. Maeda *et al.*, "Low-power-consumption direct-conversion CMOS transceiver for multi-standard 5 GHz wireless LAN systems with channel bandwidths of 5–20 MHz," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 375–383, Feb. 2006.
[30] K. Lim *et al.*, "A 2×2 MIMO tri-band dual-mode direct-conversion CMOS transceiver for worldwide WiMAX/WLAN applications," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1648–1658, Jul. 2011.
[31] H. Khatri, P. S. Gudem, and L. E. Larson, "Distortion in current commutating passive CMOS downconversion mixers," *IEEE Trans. Microw. Theory Tech.*, vol. 57, no. 11, pp. 2671–2681, Nov. 2009.

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