ABSTRACT

This article describes recent activities in the area of RF integrated circuits. First, transceiver architectures developed for cellular and cordless telephone standards are presented. Next, the choice of device technology is discussed, and the design of building blocks such as low-noise amplifiers and mixers, oscillators, and power amplifiers is described. Last, some of the emerging applications of RF circuits and their implications for the design are considered.

Recent Advances in RF Integrated Circuits

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The recent explosion in the radio frequency (RF) and wireless market has caught the semiconductor industry by surprise. The increasing demand for affordable mobile communications has introduced numerous challenges in the design of cellular and cordless telephones and pagers, and new prospects for wireless technology have motivated dramatic changes in the thought process behind deploying a communication system.

Affordability and portability are the two principal requirements — and features — of wireless communications. In fact, many developing countries have concluded that it is less expensive to equip people with mobile phones than to develop the infrastructure of a wired telephone network, an observation that may have seemed implausible 10 years ago. Translated into cost, battery life, and form factor, these requirements are met through innovations at all levels of abstraction: networking and communications, transceiver architectures, circuit design, and device technology. The overall design procedure is augmented by concurrent engineering, that is, iteration between these levels to approach an optimal system.

This article describes recent developments in the design of RF transceivers and circuits, with an emphasis on integrated solutions. The second section presents examples of cellular and cordless phone architectures, and the third section discusses the choice of integrated circuit (IC) technologies. The fourth section describes the design of a number of RF building blocks, and the fifth section provides a brief overview of emerging RF applications.

TRANSCEIVER ARCHITECTURES

Among various receiver architectures, the heterodyne approach has been the most widely accepted technique for robust operation, but alternative topologies that more easily lend themselves to integration are also under investigation [1–3]. Similarly, two types of transmitters, one-step and two-step architectures, are commonly used, although they too require many off-chip devices.

In this section, we study four transceivers designed for the Global System for Mobile Communication (GSM) and Digital European Cordless Telephone (DECT). GSM and DECT have proven to be robust and versatile solutions to cellular and cordless communications, respectively. As a result, substantial research has been expended on RF circuit integration for these two standards.

Lucent Microelectronics (formerly AT&T Microelectronics) offers a single-chip solution that, along with a low-noise amplifier (LNA) and a power amplifier, can form a complete GSM transceiver (up to the baseband interface). Figure 1 depicts the overall system [4]. The receive path translates the 900 MHz input to an intermediate frequency (IF) of 71 MHz, performs partial channel selection by means of a surface acoustic wave (SAW) filter, amplifies the signal by a programmable gain, and downconverts the result to quadrature baseband components. This architecture requires only two external filters in the receive path (excluding the duplexer), but the IF SAW device tends to have higher loss (and higher cost) if it must filter adjacent channels to sufficiently low levels.

The transmit path upconverts the baseband Gaussian-shaped data directly to 900 MHz. To minimize the effect of noise coupling from the PA to the voltage-controlled oscillators (VCOs), the required carrier signal is produced by adding the frequencies of VCO_1 and VCO_2, allowing each to operate at a frequency far from the PA output frequency. A buffer following the modulator delivers 0 dBm of power to a 50 Ω load.

The three VCOs employed in this architecture are embedded in synthesizer loops. The quadrature phases required of VCO_3 and the transmit carrier signal are generated using different circuit techniques commensurate with the frequency of operation and complexity.

Fabricated in a 12 GHz bipolar technology, the GSM chip draws approximately 60 mA from a 2.7 V supply.

Philips Semiconductor offers a pair of RF and IF chips for GSM transceivers. Figure 2 shows the overall system [5]. The receive path includes two LNAs to allow the use of two low-cost, lossy image-reject filters. The gain of each LNA can be digitally programmed, covering a range of +21 dB to –38 dB. The amplified signal is translated to an IF of 400 MHz by mixing with the output of a 1.3 GHz VCO. With the image

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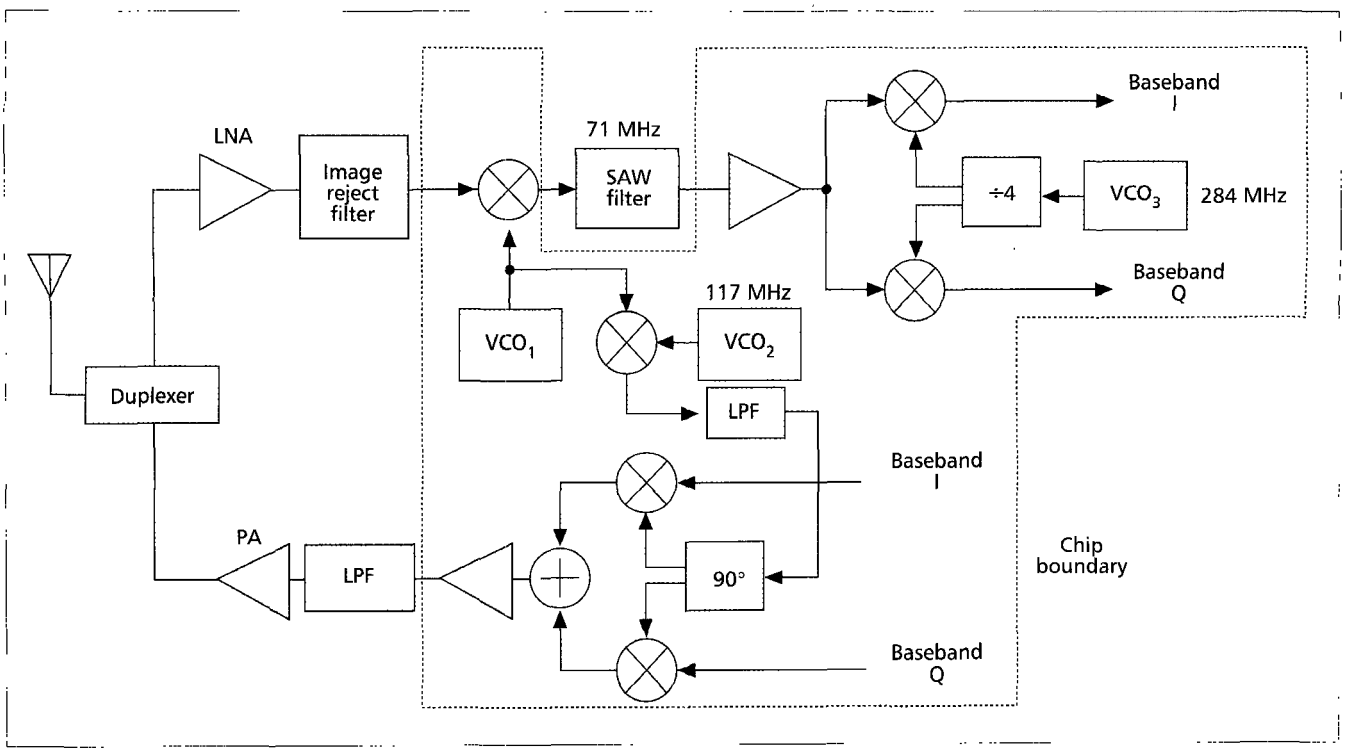


Figure 1. *Lucent Technologies GSM transceiver.*

lying at 1.7 GHz, the LNAs and the input stage of the mixer are designed so that their cumulative gain drops by approximately 30 dB at the image frequency, thus relaxing the stopband suppression required of the filters. The IF signal is then filtered and downconverted to baseband quadrature channels. Since most channel selection is performed in the baseband by means of integrated fifth-order low-pass filters, the IF SAW filter has relaxed requirements.

The transmit path incorporates two steps of upconversion. In the first step, the Gaussian-shaped baseband data is modulated on a 400 MHz carrier and subsequently filtered by a link control (LC) circuit. In the second step, the signal is split into quadrature phases and applied to a single-sideband (SSB) mixer that is driven by a 1.3 GHz oscillator. Suppressing the unwanted sideband by 20 dB, this mixer relaxes the rejection required of the preceding filter. The 900 MHz signal is then buffered and fed to the power amplifier.

The architecture of Fig. 2 incorporates only two oscillators to perform all the frequency translations in both the receive and transmit paths, thereby simplifying the prediction of various spurs that may result from coupling and intermodulation. This strategy is feasible here because the system is time-division (and frequency-division) duplexed, making it possible to share the oscillators between the two paths. (The transmit and receive time slots in GSM are offset by three time slots.)

Since both oscillators are external, the leakage of their out-

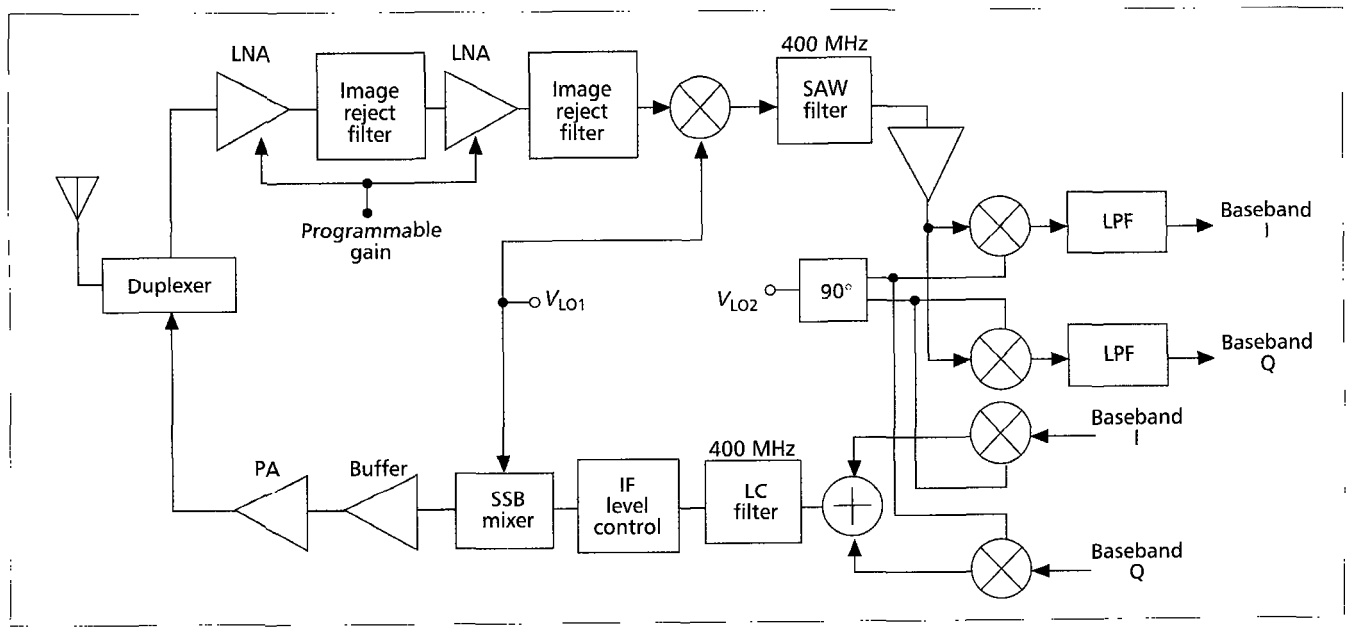


Figure 2. *The Philips GSM transceiver.*

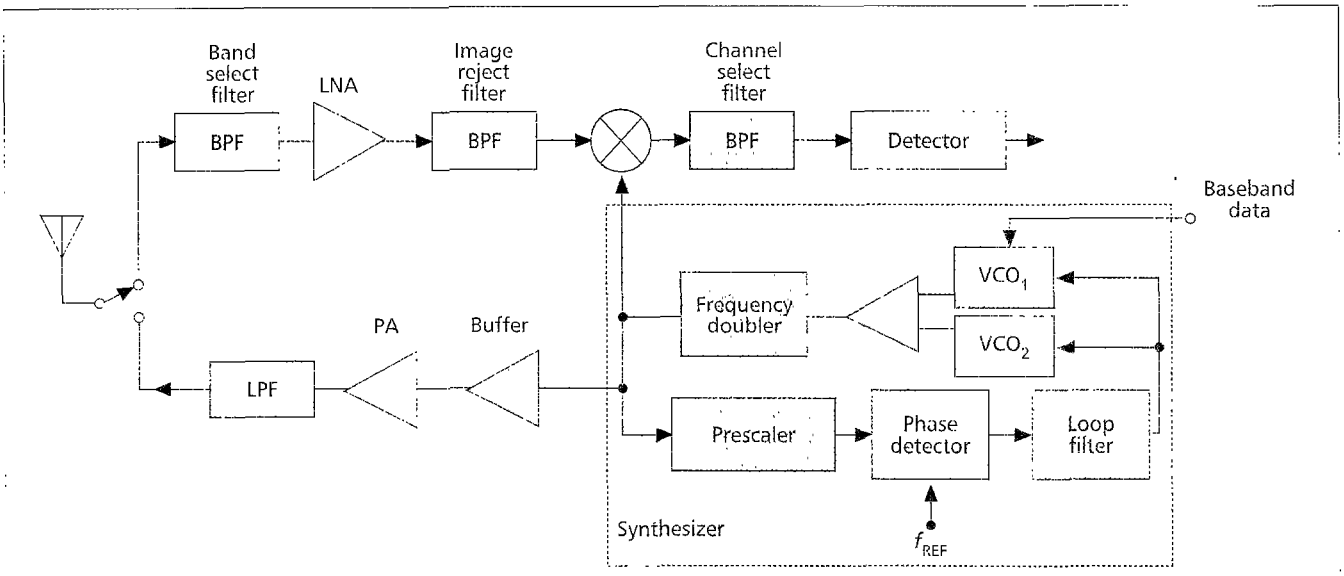


Figure 3. *Transceiver architecture for digital frequency modulation systems.*

puts to other parts of the circuit becomes problematic. In particular, if V_{LO2} were at 400 MHz, then, similar to the case of homodyne downconversion, self-mixing would corrupt the baseband signals by DC offsets [6, 7]. For this reason, V_{LO2} is generated at 800 MHz, and the frequency is divided by two on the IF chip. This also provides the quadrature phases required for driving the downconversion and upconversion mixers.

An interesting provision in the transceiver of Fig. 2 is partial compatibility with another standard, Digital Communications System at 1800 MHz (DCS1800) [5]. This standard is similar to GSM, but operates around 1.8 GHz. The frequency of V_{LO1} is chosen to be midway between the GSM and DCS1800 bands, allowing use of a 400 MHz IF for both but requiring high-side injection in the former and low-side injection in the latter. Thus, in principle, the two standards can share all sections of the transceiver except for the LNAs, image-reject filters, and power amplifier.

Fabricated in a 13 GHz bipolar complementary metal oxide semiconductor (BiCMOS) technology, the GSM transceiver draws a current of 50 mA in receive mode and 105 mA in transmit mode while operating from a 2.7 V supply.

Figure 3 shows a transceiver designed for wireless systems employing digital frequency modulation with time-division duplexing (TDD) [8], such as Digital European Cordless Telecommunications (DECT), wireless local area networks (WLANs), and wireless local loop (WLL). Following front-end filtering, amplification, and image rejection, the receiver translates the signal to an IF of 110 MHz. A SAW filter then performs channel selection, applying the frequency-modulated waveform directly to a detector.

The transmitter comprises a synthesizer loop with direct modulation of the VCO, several stages of isolation buffering, and a power amplifier. Note that the LO signal required for the receiver downconversion mixer is provided by the same synthesizer. This is possible because in a TDD system the receive and transmit paths do not operate simultaneously.

Direct modulation of VCO_1 is accomplished by first closing the synthesizer loop to establish the proper carrier frequency and subsequently opening the loop and applying the baseband data to the control line of the oscillator. Since the VCO is not phase-locked during the actual transmission, great care must be taken to minimize variations in the supply voltage and the load impedance so as to maintain the carrier frequency with an error less than 50 kHz. Thus, the transmitter incorporates several voltage regulators and isolation buffers. A provision is also made for utilizing a separate oscillator, VCO_2, for the receive operation in systems where the receive and transmit bands are different.

Fabricated in a 25 GHz silicon bipolar process and employing an external LNA, the receiver of Fig. 3 achieves a sensitivity of –95 dBm with an input IP_3 of –17 dBm. The transmitter delivers an adjustable output power of up to +5.5 dBm.

Figure 4 shows a 1.9 GHz dual-conversion receiver implemented in CMOS technology for DECT applications [9]. Based on the Weaver image-reject architecture [10], the circuit consists of a front-end LNA, a quadrature downconversion to an IF of approximately 200 MHz, a second downconversion to zero frequency, and baseband channel select filters and analog-to-digital (A/D) converters. In this architecture, the first LO has a fixed frequency while the sec-

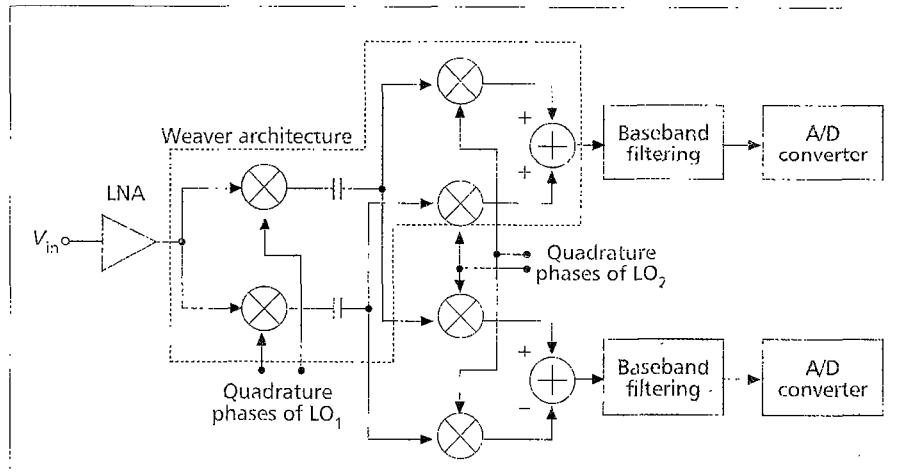


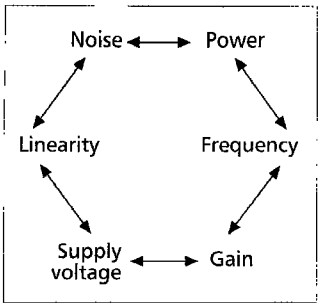
Figure 4. *The DECT image-reject receiver.*

ond selects the desired channel. Thus, the first LO close-in phase noise can be suppressed by employing a wide loop bandwidth in its associated synthesizer [9].

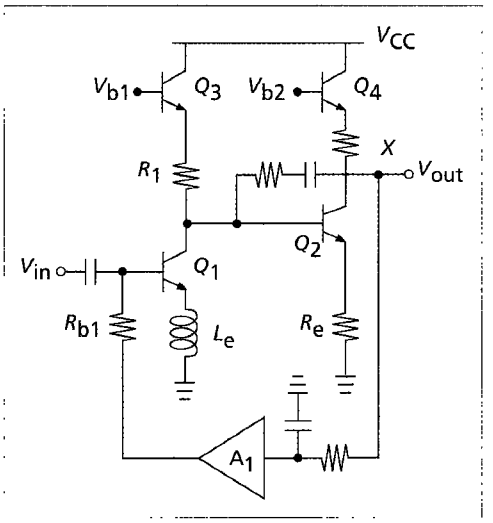
The image rejection of the Weaver topology is limited by phase and gain mismatches in LO and signal paths [10]. Nevertheless, in the receiver of Fig. 4 the image is approximately 400 MHz away from the signal, thereby experiencing suppression in the front-end filter and the tuned LNA.

The receiver baseband processing consists of a second-order Sallen and Key anti-aliasing filter, an eighth-order switched-capacitor channel-select filter, and a 10-bit A/D converter. In addition, to cancel dc offsets due to self-mixing of the second LO, two current-steering D/A converters that can be controlled externally are employed.

Fabricated in a 0.6 μm CMOS technology, the receiver of Fig. 4 achieves a sensitivity of –90 dBm with an input IP_3 of –7 dBm while consuming approximately 200 mW from a 3.3 V supply.



■ **Figure 5.** *RF design hexagon.*



■ **Figure 6.** *Two-stage bipolar LNA.*

IC Technologies

The viable IC technology for RF circuits continues to change. Performance, cost, and time to market are three critical factors influencing the choice of technologies in the competitive RF industry. In addition, issues such as level of integration, form factor, and prior (successful) experience play an important role in the decisions made by designers.

At present, GaAs and silicon bipolar and BiCMOS technologies constitute the major section of the RF market. Usually viewed as a low-yield high-power high-cost option, GaAs field-effect and heterojunction devices nonetheless have maintained a strong presence in RF products [12], especially in power amplifiers and front-end switches.

While GaAs processes offer useful features such as higher (breakdown voltage)(cut-off frequency) product, semi-insulating substrate, and high-quality inductors and capacitors, silicon devices in a very large-scale integration (VLSI) technology can potentially provide both higher levels of integration and lower overall cost, as demonstrated in complex circuits such as frequency synthesizers. In fact, all building blocks of typical transceivers are available in silicon bipolar technologies from many manufacturers.

Market predictions indicate that GaAs and silicon bipolar and BiCMOS technologies will sustain their strong presence in the RF market for many years. However, a third contender is CMOS technology. Supported by the enormous momentum of the digital market, CMOS devices have achieved high transit frequencies (e.g., tens of gigahertz in the 0.35 µm generation), and "RF CMOS" has suddenly become the topic of active research. CMOS technology must nevertheless resolve a number of practical issues: substrate coupling of signals that differ in amplitude by 100 dB, parameter variation with temperature and process, and device modeling for RF operation.

Building Blocks

The design of an RF transceiver heavily depends on the performance of its constituent subcircuits. LNAs, mixers, oscillators, frequency synthesizers, modulators, and power amplifiers are the principal RF building blocks in a typical system, each exhibiting trade-offs that can be summarized in the "RF design hexagon" of Fig. 5. Almost every two parameters in Fig. 5 trade with each other to some extent.

In this section, we present recent work in the design of some of these building blocks.

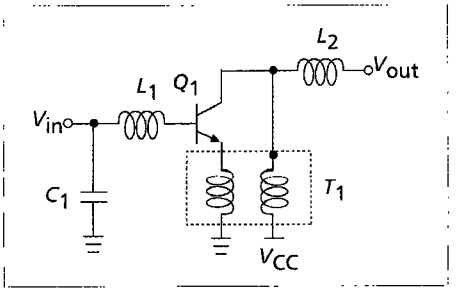
Low-Noise Amplifiers and Mixers

As the first stages in the receive path, LNAs and mixers must process the signal with minimal noise and interference. In addition to the noise figure (NF) and third intercept point (IP_3), the gain, port-to-port isolation, and power dissipation of these circuits impact the performance of a transceiver. The very low noise required of LNAs usually mandates the use of only one active device at the input without any (high-frequency) resistive feedback. In order to provide sufficient gain while driving 50 Ω, some LNAs employ more than one stage.

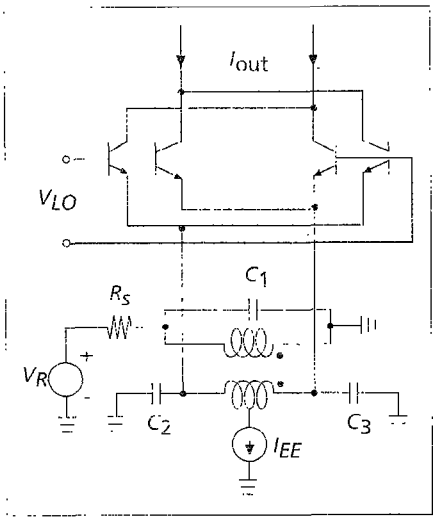
A bipolar LNA is shown in Fig. 6 [13], where the first stage utilizes a bond wire inductance L_e = 1.5 nH to degenerate the common-emitter amplifier, Q_1, without introducing additional noise. This technique both linearizes the LNA and makes it possible to achieve a 50 Ω input impedance. Bias voltages V_{b1} and V_{b2} and the low-frequency feedback amplifier A_1 are chosen to stabilize the gain against temperature and supply variations. The resistive feedback in the second stage improves the linearity and lowers the output impedance. The circuit exhibits a noise figure of 2.2 dB, an IP_3 of –10 dBm, and a gain of 16 dB at 900 MHz.

Another bipolar LNA designed to drive a 50 Ω load is depicted in Fig. 7 [14]. Employing negative feedback through a monolithic transformer to linearize the circuit, the LNA can operate with supply voltages as low as one V_{BE}. Interestingly, the transformer reduces the amplifier gain at both low and high frequencies, helping to stabilize the circuit. The external inductor L_1 and capacitor C_1 provide conjugate matching at the input.

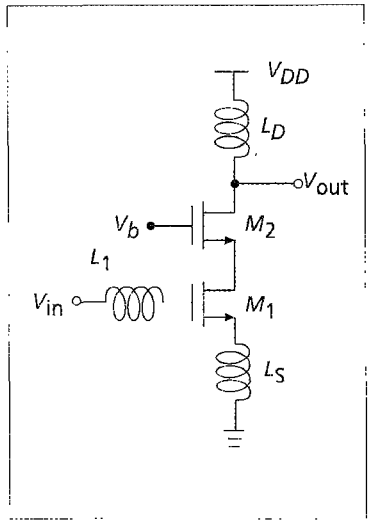
Drawing 2 mA from a 1.9 V supply, the circuit of Fig. 7 achieves a noise figure of 2.8 dB and a gain of 9.6 dB at 1.9 GHz in an 11 GHz BiCMOS



■ **Figure 7.** *Bipolar LNA using transformer feedback.*



■ **Figure 8.** *Double-balanced bipolar mixer with transformer coupling.*



■ **Figure 9.** *CMOS cascode LNA.*

technology. The transformer feedback boosts the input IP_3 to –3 dBm.

A double-balanced bipolar mixer designed in conjunction with the above LNA is shown in Fig. 8 [14]. Here, an on-chip transformer both operates as a single-ended to differential converter and provides input matching. The bias current of the switching quad is established by IEE, and capacitors $C_1 - C_3$ effect resonance at the primary and secondary transformers.

A 1.9 GHz implementation of this configuration in an 11 GHz bipolar technology exhibits an NF of 10.9 dB with an IP_3 of +2.3 dBm while dissipating 5 mW from a 1.9 V supply [14].

Shown in Fig. 9 is a 1.5 GHz CMOS LNA employing on-chip and off-chip inductors [15]. In a manner similar to that described for the circuit of Fig. 6, this LNA incorporates L_S and L_1 to create conjugate matching at the input. At 1.5 GHz, the on-chip inductor L_D provides significant voltage gain even though its Q is less than 4. By contrast, a load resistor would require a large voltage drop to provide a comparable gain.

The common-gate transistor, M_2, plays two important roles by increasing the reverse isolation of the LNA:

1) It lowers the LO leakage produced by the following mixer.
2) It improves the stability of the circuit by minimizing the feedback from the output to the input.

Note that the same circuit with no cascode device would be prone to oscillation.

The LNA of Fig. 9 is followed by another cascode stage to drive a 50 Ω load, with each stage drawing 10 mA. Fabricated in a 0.6 μm CMOS technology and operating from a 1.5 V supply, the circuit achieves a noise figure of 3 dB, a gain of 20 dB, and an input IP_3 of –10 dBm.

Figure 10 shows the simplified circuits of an LNA and a mixer designed for a 900 MHz direct-conversion receiver [16]. Requiring no image-reject filtering due to the zero IF, the receiver allows direct cascading of the two circuits, obviating the need for a 50 Ω interface between the LNA and the mixer. The LNA is configured as a differential common-gate topology, exhibiting an input impedance of 50 Ω (on each side) by proper sizing and biasing of M_1 and M_2. However, since the transconductance of each transistor is roughly equal to 1/(50 Ω), the noise figure cannot drop below a certain bound (2.2 dB with long-channel approximations).

The mixer resembles a Gilbert cell except that the sources of M_1 and M_2 are grounded. For square-law devices, this configuration does not produce third-order distortion, whereas a differential pair biased at a constant tail current does. Thus, "grounded-source" MOS pairs potentially achieve a higher IP_3 than do regular differential pairs. The load of the mixer consists of self-biased current sources M_3 and M_4 and gain-setting resistors R_1 and R_2.

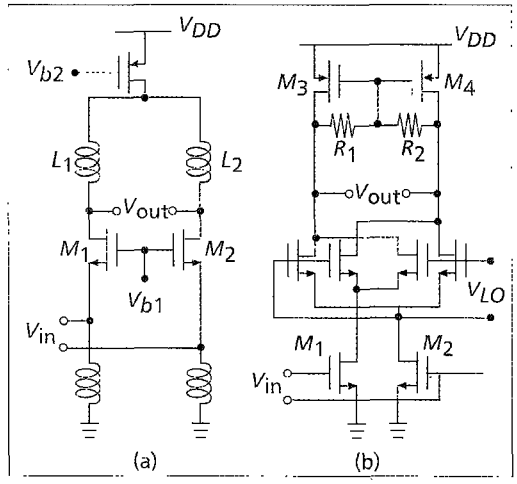
The LNA/mixer combination has been fabricated in a 1mm CMOS technology. Consuming 27 mW from a 3 V supply, the circuit exhibits an overall noise figure of 3.2 dB and an IP_3 of +8 dBm.

Other examples of LNAs and mixers can be found in [9, 17, 18].

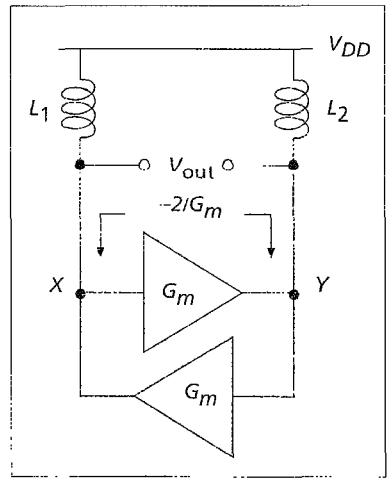
Oscillators

The local oscillators used to drive downconversion and upconversion mixers are embedded in a synthesizer loop to achieve a precise frequency definition. Phase noise, sidebands (spurs), tuning range, and settling behavior of synthesizers are critical parameters in RF applications, creating severe trade-offs as the number of external components is reduced.

Most integrated RF oscillators are configured as a negative-G_m stage with inductive load, as exemplified by Fig. 11. The idea is that an active circuit provides a negative resistance that cancels the finite loss in the inductors (and capacitors), thereby sustaining oscillation. While on-chip spiral inductors are attractive for higher levels of integration, various loss mechanisms limit the quality factor (Q) to approximately 4 in typical CMOS technologies. As depicted in Fig. 12, wire resistance and electric and magnetic coupling to the substrate contribute loss. Another important issue, particularly in CMOS circuits, is the upconversion of $1/f$ noise to the vicinity of the carrier frequency [19].



■ **Figure 10.** *a) Common-gate CMOS LNA; b) CMOS mixer with grounded-source input pair.*



■ **Figure 11.** *Oscillator using negative-G_m topology*

In bipolar technologies, spiral inductors exhibit slightly higher Qs because the substrate is lightly doped, that is, electric and magnetic coupling of the inductor to the substrate is less pronounced. Figure 13 shows a bipolar implementation incorporating monolithic inductors with a Q of approximately 9 [20]. Using emitter followers in the loop to allow larger voltage swings at X and Y, the oscillator exhibits a phase noise of –105 dBc/Hz at 100 kHz offset. The CMOS version (with no followers) has also been studied [21–23].

Figure 14 shows a CMOS VCO topology designed for 900 MHz and 1.8 GHz [24]. Here, the transconductance amplifier incorporates both n-type MOS (NMOS) and p-type MOS (PMOS) devices to achieve a higher transconductance for a given bias current. However, the additional capacitance contributed by the PMOS transistors limits the tuning range further. Drawing approximately 10 mW from a 3 V supply, the 900 MHz version of the oscillator exhibits a phase noise of –108 dBc/Hz at 100 kHz offset and a tuning range of 190 MHz [24].

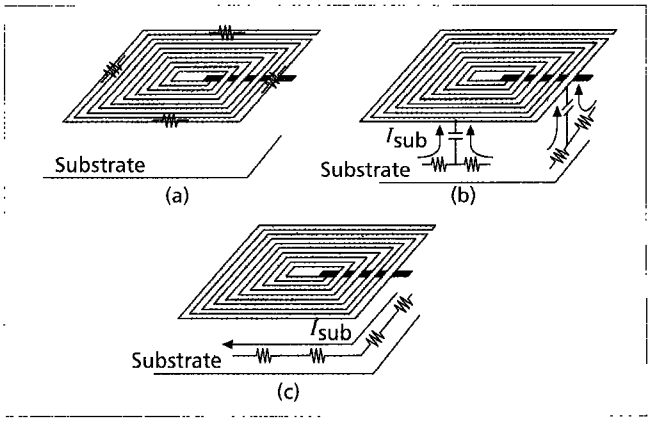
An important issue in fully monolithic LC oscillators is the trade-off between the phase noise and the tuning range [23]. For a given power dissipation, the relative phase noise decreases as the value of the tank inductance increases, but at the cost of making the capacitance of the transistors and the inductor a significant part of the tank. As a result, the *variable* component of the tank capacitance drops. Also, at low supply voltages, the variation obtained from a varactor diode becomes more limited.

At present, oscillators used in demanding applications such as cellular telephones still incorporate external resonators (inductors, microstrip lines, or filters) to achieve an acceptably low phase noise and an adequate tuning range. Nonetheless, the properties of inductors built on silicon substrates are under vigorous study.

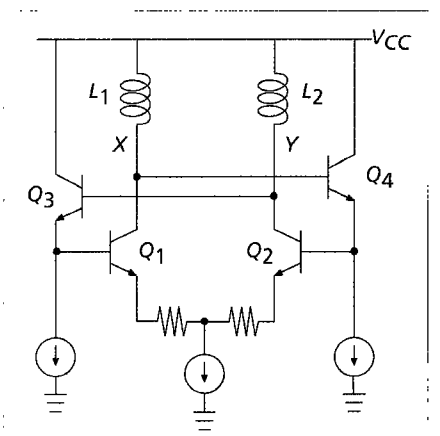
Power Amplifiers

Power amplifiers are among the most power-hungry building blocks of RF transceivers, challenging designers by supply-efficiency-linearity trade-offs. The enormous current levels and high slew rates are the principal difficulty in the design of power amplifiers and especially the package. For example, with a peak current of several amperes through the output transistor, the slew rate at 900 MHz is on the order of 10 A/ns. Thus, even parasitic resistances on the order of tens of milliohms and inductances on the order of tens of picohenries may result in considerable loss of efficiency. For these reasons, many layout and packaging issues that are usually unimportant in other analog and RF circuits become crucial in power amplifiers.

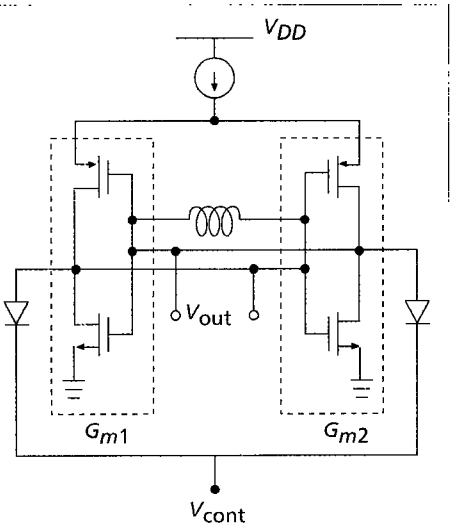
Shown in Fig. 15 is the simplified circuit of a nonlinear MESFET power amplifier operating at 835 MHz [25]. The first stage incorporates two tanks in series, one tuned to the first harmonic and the other to the third, to provide an approximation of a square wave at node X. This technique reduces the transition times at the gate of M_2, minimizing the power loss in the output transistor. The output stage is configured as a class E amplifier [26], achieving a high efficiency by creating nonoverlapping voltage and current waveforms and hence minimizing the loss in the output device. Fabricated in an 0.8 μm metal-semiconductor field-effect transistor (MESFET) technology and operating from a 2.5 V supply, the circuit delivers 250 mW with 50 percent efficiency. Note that the low substrate loss in MESFET technologies makes it possible to integrate the entire PA on one chip.



■ **Figure 12** *Loss mechanism in monolithic inductors: a) wire resistance; b) electric coupling to substrate; c) magnetic coupling to substrate.*



■ **Figure 13.** *Bipolar negative-G_m oscillator.*



■ **Figure 14.** *CMOS negative-G_m VCO.*

Figure 16 depicts a 900 MHz CMOS power amplifier [27]. The circuit consists of an input matching network, several tuned gain stages, an output stage, and an output matching network. The gain stages serve to both amplify the voltage swings and provide high drive capability for the output transistor, which is 8400 μm wide.

Designed to amplify constant-envelope modulated waveforms, the PA of Fig. 16 does not require linearity in the stages. However, with the specified input level (+5 dBm), the cascode stage operates in class A and the second stage in class AB. The last two stages are designed as "switching" circuits to deliver substantial power with relatively high efficiency. This is in contrast to class C stages, which achieve a high efficiency only at small output power levels.

The PA is fabricated in an 0.8 μm CMOS technology and operates with a 2.5 V supply. With an output power of 1 W, the circuit exhibits a power-added efficiency of 42 percent.

Emerging Applications

In addition to familiar wireless products such as pagers and cellular phones, RF technology has created many other markets that display a

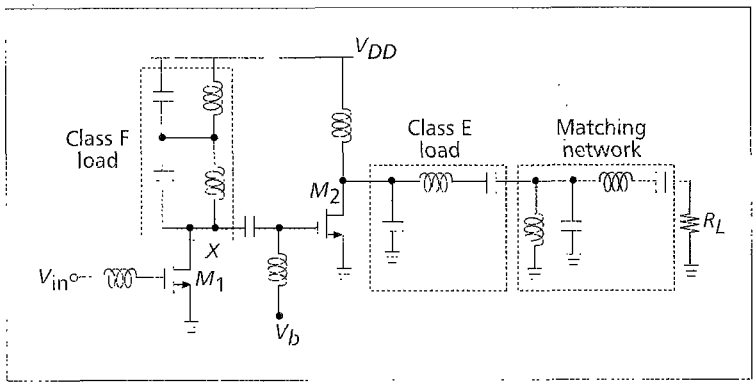


Figure 15. *MESFET power amplifier.*

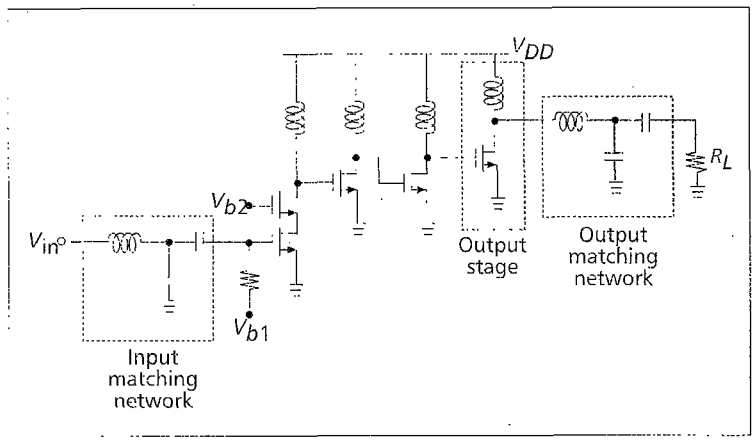


Figure 16. *CMOS power amplifier.*

great potential for rapid growth, each presenting its own set of challenges to RF designers.

WLANs

Communication among people or pieces of equipment in a crowded area can be realized through a wireless local area network. WLAN transceivers can provide mobile connectivity in offices, hospitals, factories, etc., obviating the need for cumbersome wired networks. Portability and reconfigurability are prominent features of such systems.

WLANs constitute a rapidly growing sector of the RF industry. At present, the unlicensed 2.4 GHz band is exploited for such applications [28] to provide data rates around 2 Mb/s. However, the higher rates required in exchanging digitized video and eventually establishing a wireless multimedia environment make it desirable to employ wideband standards. One such standard is the High Performance Local Area Network (HIPERLAN), operating around 5.2 GHz and allocating a bandwidth of 23.5 MHz to each user [29].

HIPERLAN presents many challenges in the design of both the RF section and the baseband section of transceivers. The high carrier frequency makes it difficult to design RF amplifiers, mixers, and oscillators in mainstream VLSI technologies. Furthermore, for a 23.5 MHz bandwidth, functions such as channel selection filtering and A/D conversion with low noise and high linearity entail severe trade-offs.

Digital baseband processing for HIPERLAN involves its own challenges. Equalization at 23.5 Mb/s with reasonable power dissipation and silicon area demands a great deal of work in high-speed low-power digital design.

GPS

The use of the Global Positioning System (GPS) to determine one's location as well as obtain directions becomes attractive to the consumer market as the cost and power dissipation of GPS receivers drop. Operating in the 1.5 GHz range, such systems are under consideration by automobile manufacturers, but they may be available as low-cost handheld products sometime in the near future. High sensitivity and low power drain are the main challenges in the design of GPS receivers.

RF IDs

RF identification systems, simply called "RF IDs," are small wireless tags that can be attached to objects or persons to track their position. Applications range from luggage in airports to troops in military operations. Low power consumption is especially critical here since the tag's lifetime may be determined by that of a single small battery. RF ID products in the 900 MHz and 2.4 GHz range have recently appeared in the market.

Multistandard Transceivers

The existence of various wireless standards within the United States and around the world has created a demand for transceivers that can operate in more than one mode. In the simplest case, two different receive and transmit frequency bands must be supported while other properties of the system remain unchanged. For example, the two European standards, GSM and DCS1800, differ primarily by their frequency bands. In a more sophisticated scenario, the transceiver can operate with two vastly different standards, such as IS-54 (time-division multiple access) and IS-95 (code-division multiple access).

Accommodating two or more standards in one transceiver generally requires substantial added complexity in both the RF and baseband sections, leading to high cost. Thus, the system must be designed to maximize the shared hardware.

Cable Modem

RF design finds application in *wired* systems as well. An important example is "cable modem," a standard that allows data communication over the cable TV network [30].

The principal challenge in cable modem RF design is that the system must interfere negligibly with the cable TV channels. Thus, unwanted noise, spurs, and harmonics, especially in the transmit path, must be predicted and controlled accurately. Furthermore, unlike typical wireless applications, cable modem operates across more than one decade of frequencies, requiring a wide range in some of the filters and oscillators.

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