A Study of Phase Noise in CMOS Oscillators

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***Abstract*— This paper presents a study of phase noise in two inductorless CMOS oscillators. First-order analysis of a linear oscillatory system leads to a noise shaping function and a new definition of Q. A linear model of CMOS ring oscillators is used to calculate their phase noise, and three phase noise phenomena, namely, additive noise, high-frequency multiplicative noise, and low-frequency multiplicative noise, are identified and formulated. Based on the same concepts, a CMOS relaxation oscillator is also analyzed. Issues and techniques related to simulation of noise in the time domain are described, and two prototypes fabricated in a 0.5-μm CMOS technology are used to investigate the accuracy of the theoretical predictions. Compared with the measured results, the calculated phase noise values of a 2-GHz ring oscillator and a 900-MHz relaxation oscillator at 5 MHz offset have an error of approximately 4 dB.**

I. Introduction

VOLTAGE-CONTROLLED oscillators (VCO's) are an integral part of phase-locked loops, clock recovery circuits, and frequency synthesizers. Random fluctuations in the output frequency of VCO's, expressed in terms of jitter and phase noise, have a direct impact on the timing accuracy where phase alignment is required and on the signal-to-noise ratio where frequency translation is performed. In particular, RF oscillators employed in wireless tranceivers must meet stringent phase noise requirements, typically mandating the use of passive LC tanks with a high quality factor (Q). However, the trend toward large-scale integration and low cost makes it desirable to implement oscillators monolithically. The paucity of literature on noise in such oscillators together with a lack of experimental verification of underlying theories has motivated this work.

This paper provides a study of phase noise in two inductorless CMOS VCO's. Following a first-order analysis of a linear oscillatory system and introducing a new definition of Q, we employ a linearized model of ring oscillators to obtain an estimate of their noise behavior. We also describe the limitations of the model, identify three mechanisms leading to phase noise, and use the same concepts to analyze a CMOS relaxation oscillator. In contrast to previous studies where time-domain jitter has been investigated [1], [2], our analysis is performed in the frequency domain to directly determine the phase noise. Experimental results obtained from a 2-GHz ring oscillator and a 900-MHz relaxation oscillator indicate that, despite many simplifying approximations, lack of accurate MOS models for RF operation, and the use of simple noise models, the analytical approach can predict the phase noise with approximately 4 to 6 dB of error.

The next section of this paper describes the effect of phase noise in wireless communications. In Section III, the concept of Q is investigated and in Section IV it is generalized through the analysis of a feedback oscillatory system. The resulting equations are then used in Section V to formulate the phase noise of ring oscillators with the aid of a linearized model. In Section VI, nonlinear effects are considered and three mechanisms of noise generation are described, and in Section VII, a CMOS relaxation oscillator is analyzed. In Section VIII, simulation issues and techniques are presented, and in Section IX the experimental results measured on the two prototypes are summarized.

II. Phase Noise in Wireless Communications

Phase noise is usually characterized in the frequency domain. For an ideal oscillator operating at ω_0, the spectrum assumes the shape of an impulse, whereas for an actual oscillator, the spectrum exhibits "skirts" around the center or "carrier" frequency (Fig. 1). To quantify phase noise, we consider a unit bandwidth at an offset $\Delta\omega$ with respect to ω_0, calculate the noise power in this bandwidth, and divide the result by the carrier power.

To understand the importance of phase noise in wireless communications, consider a generic transceiver as depicted in Fig. 2, where the receiver consists of a low-noise amplifier, a band-pass filter, and a downconversion mixer, and the transmitter comprises an upconversion mixer, a band-pass filter, and a power amplifier. The local oscillator (LO) providing the carrier signal for both mixers is embedded in a frequency synthesizer. If the LO output contains phase noise, both the downconverted and upconverted signals are corrupted. This is illustrated in Fig. 3(a) and (b) for the receive and transmit paths, respectively.

Referring to Fig. 3(a), we note that in the ideal case, the signal band of interest is convolved with an impulse and thus translated to a lower (and a higher) frequency with no change in its shape. In reality, however, the wanted signal may be accompanied by a large interferer in an adjacent channel, and the local oscillator exhibits finite phase noise. When the two signals are mixed with the LO output, the downconverted band consists of two overlapping spectra, with the wanted signal suffering from significant noise due to tail of the interferer. This effect is called "reciprocal mixing."

Shown in Fig. 3(b), the effect of phase noise on the transmit path is slightly different. Suppose a noiseless receiver is to

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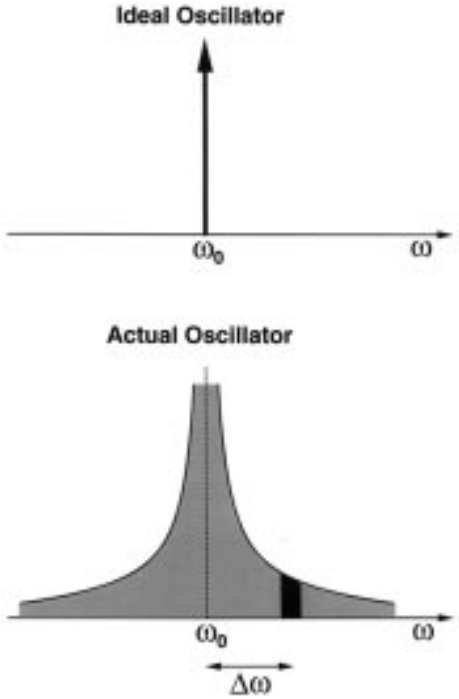


Fig. 1. Phase noise in an oscillator.

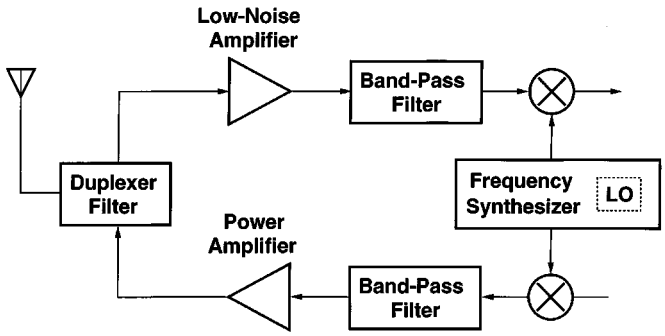


Fig. 2. Generic wireless transceiver.

detect a weak signal at ω_2 while a powerful, nearby tranmitter generates a signal at ω_1 with substantial phase noise. Then, the wanted signal is corrupted by the phase noise tail of the transmitter.

The important point here is that the difference between ω_1 and ω_2 can be as small as a few tens of kilohertz while each of these frequencies is around 900 MHz or 1.9 GHz. Therefore, the output spectrum of the LO must be extremely sharp. In the North American Digital Cellular (NADC) IS54 system, the phase noise power per unit bandwidth must be about 115 dB below the carrier power (i.e., -115 dBc/Hz) at an offset of 60 kHz.

Such stringent requirements can be met through the use of LC oscillators. Fig. 4 shows an example where a transconductance amplifier (G_m) with positive feedback establishes a negative resistance to cancel the loss in the tank and a varactor diode provides frequency tuning capability. This circuit has a number of drawbacks for monolithic implementation. First, both the control and the output signals are single-ended,

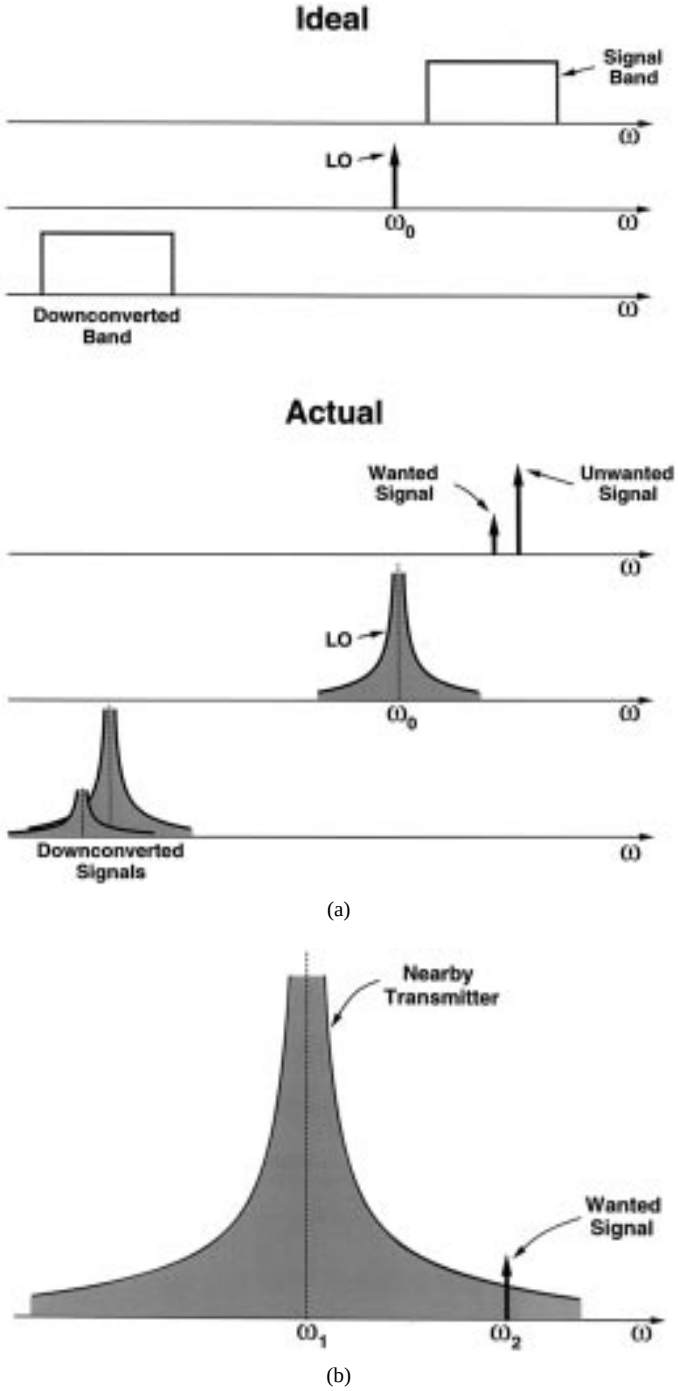


Fig. 3. Effect of phase noise on (a) receive and (b) transmit paths.

making the circuit sensitive to supply and substrate noise. Second, the required inductor (and varactor) Q is typically greater than 20, prohibiting the use of low-Q integrated inductors. Third, monolithic varactors also suffer from large series resistance and hence a low Q. Fourth, since the LO signal inevitably appears on bond wires connecting to (or operating as) the inductor, there may be significant coupling of this signal to the front end ("LO leakage"), an undesirable effect especially in homodyne architectures [3].

Ring oscillators, on the other hand, require no external components and can be realized in fully differential form, but

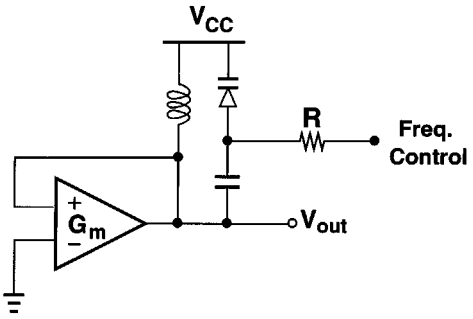


Fig. 4. LC oscillator.

their phase noise tends to be high because they lack passive resonant elements.

III. Definitions of Q

The quality factor, Q, is usually defined within the context of second-order systems with (damped) oscillatory behavior. Illustrated in Fig. 5 are three common definitions of Q. For an RLC circuit, Q is defined as the ratio of the center frequency and the two-sided -3-dB bandwidth. However, if the inductor is removed, this definition cannot be applied. A more general definition is: 2π times the ratio of the stored energy and the dissipated energy per cycle, and can be measured by applying a step input and observing the decay of oscillations at the output. Again, if the circuit has no oscillatory behavior (e.g., contains no inductors), it is difficult to define "the energy dissipated per cycle." In a third definition, an LC oscillator is considered as a feedback system and the phase of the *open-loop* transfer function is examined at resonance. For a simple LC circuit such as that in Fig. 4, it can be easily shown that the Q of the tank is equal to $0.5\omega_0\, d\Phi/d\omega$, where ω_0 is the resonance frequency and $d\Phi/d\omega$ denotes the slope of the phase of the transfer function with respect to frequency. Called the "open-loop Q" herein, this definition has an interesting interpretation if we recall that for steady oscillations, the total phase shift around the loop must be precisely 360°. Now, suppose the oscillation frequency slightly deviates from ω_0. Then, if the phase slope is large, a significant change in the phase shift arises, violating the condition of oscillation and forcing the frequency to return to ω_0. In other words, the *open-loop* Q is a measure of how much the *closed-loop* system opposes variations in the frequency of oscillation. This concept proves useful in our subsequent analyses.

While the third definition of Q seems particularlly well-suited to oscillators, it does fail in certain cases. As an example, consider the two-integrator oscillator of Fig. 6, where the open-loop transfer function is simply

$$H(s) = -\left(\frac{\omega_0}{s}\right)^2 \tag{1}$$

yielding $\Phi = \angle H(s = j\omega) = 0$, and $Q = 0$. Since this circuit does indeed oscillate, this definition of Q is not useful here.

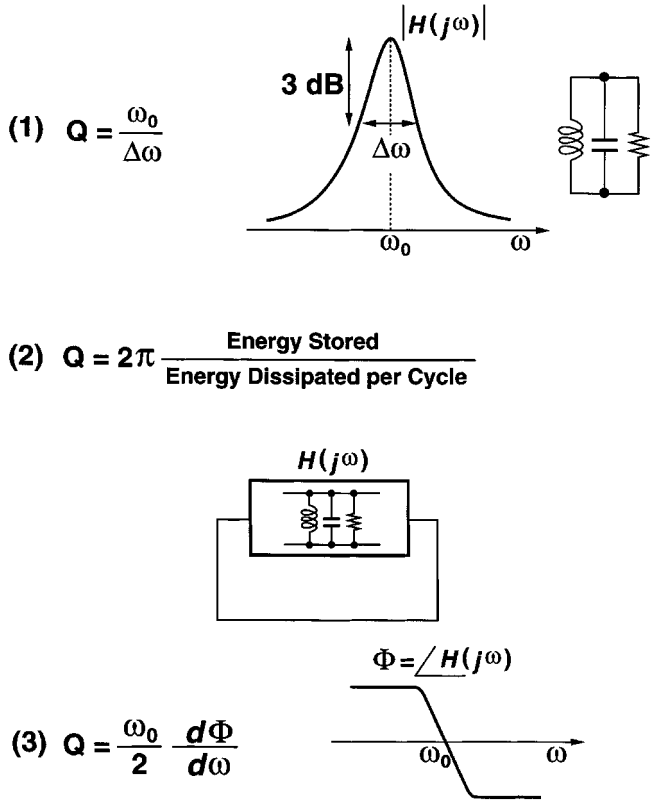


Fig. 5. Common definitions of Q.

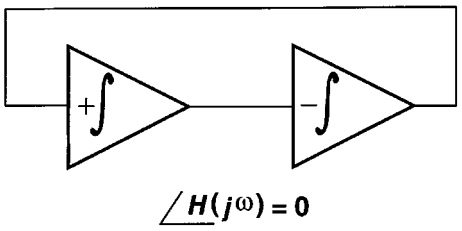


Fig. 6. Two-integrator oscillator.

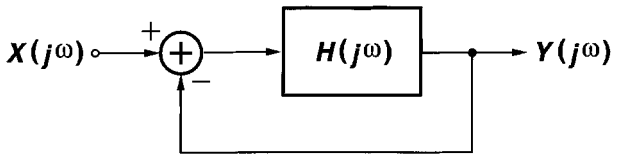


Fig. 7. Linear oscillatory system.

IV. Linear Oscillatory System

Oscillator circuits in general entail "compressive" nonlinearity, fundamentally because the oscillation amplitude is not defined in a linear system. When a circuit begins to oscillate, the amplitude continues to grow until it is limited by some other mechanism. In typical configurations, the open-loop gain of the circuit drops at sufficiently large signal swings, thereby preventing further growth of the amplitude.

In this paper, we begin the analysis with a linear model. This approach is justified as follows. Suppose an oscillator employs strong automatic level control (ALC) such that its oscillation amplitude remains small, making the linear approximation

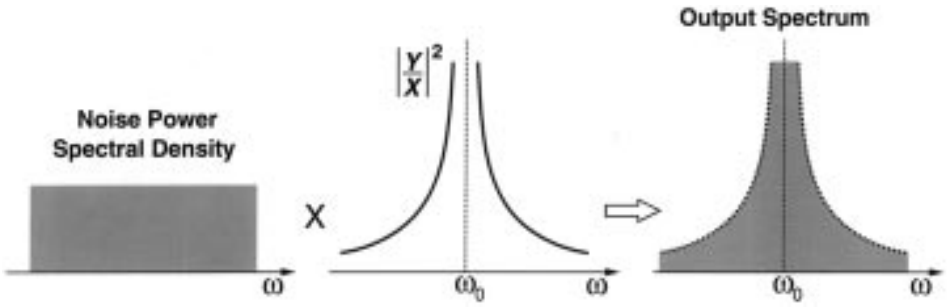


Fig. 8. Noise shaping in oscillators.

valid. Since the ALC can be relatively slow, the circuit parameters can be considered time-invariant for a large number of cycles. Now, let us gradually weaken the effect of ALC so that the oscillator experiences increasingly more "self-limiting." Intuitively, we expect that the linear model yields reasonable accuracy for soft amplitude limiting and becomes gradually less accurate as the ALC is removed. Thus, the choice of this model depends on the *error* that it entails in predicting the response of the actual oscillator to various sources of noise, an issue that can be checked by simulation (Section VIII). While adequate for the cases considered here, this approximation must be carefully examined for other types of oscillators.

To analyze phase noise, we treat an oscillator as a feedback system and consider each noise source as an input (Fig. 7). The phase noise observed at the output is a function of: 1) sources of noise in the circuit and 2) how much the feedback system rejects (or amplifies) various noise components. The system oscillates at $\omega = \omega_0$ if the transfer function

$$\frac{Y}{X}(j\omega) = \frac{H(j\omega)}{1 + H(j\omega)} \tag{2}$$

goes to infinity at this frequency, i.e., if $H(j\omega_0) = -1$. For frequencies close to the carrier, $\omega = \omega_0 + \Delta\omega$, the open-loop transfer function can be approximated as

$$H(j\omega) \approx H(j\omega_0) + \Delta\omega \frac{dH}{d\omega} \tag{3}$$

and the noise tranfer function is

$$\frac{Y}{X}[j(\omega_0 + \Delta\omega)] = \frac{H(j\omega_0) + \Delta\omega \dfrac{dH}{d\omega}}{1 + H(j\omega_0) + \Delta\omega \dfrac{dH}{d\omega}}. \tag{4}$$

Since $H(j\omega_0) = -1$ and for most practical cases $|\Delta\omega\ dH/d\omega| \ll 1$, (4) reduces to

$$\frac{Y}{X}[j(\omega_0 + \Delta\omega)] \approx \frac{-1}{\Delta\omega \dfrac{dH}{d\omega}}. \tag{5}$$

This equation indicates that a noise component at $\omega = \omega_0 + \Delta\omega$ is multiplied by $-(\Delta\omega\ dH/d\omega)^{-1}$ when it appears at the output of the oscillator. In other words, the noise power spectral density is shaped by

$$\left|\frac{Y}{X}[j(\omega_0 + \Delta\omega)]\right|^2 = \frac{1}{(\Delta\omega)^2 \left|\dfrac{dH}{d\omega}\right|^2}. \tag{6}$$

This is illustrated in Fig. 8. As we will see later, (6) assumes a simple form for ring oscillators.

To gain more insight, let $H(j\omega) = A(\omega)\exp[j\Phi(\omega)]$, and hence

$$\frac{dH}{d\omega} = \left(\frac{dA}{d\omega} + jA\frac{d\Phi}{d\omega}\right)\exp(j\Phi). \tag{7}$$

Since for $\omega \approx \omega_0, A \approx 1$, (6) can be written as

$$\left|\frac{Y}{X}[j(\omega_0 + \Delta\omega)]\right|^2 = \frac{1}{(\Delta\omega)^2\left[\left(\dfrac{dA}{d\omega}\right)^2 + \left(\dfrac{d\Phi}{d\omega}\right)^2\right]}. \tag{8}$$

We define the open-loop Q as

$$Q = \frac{\omega_0}{2}\sqrt{\left(\frac{dA}{d\omega}\right)^2 + \left(\frac{d\Phi}{d\omega}\right)^2}. \tag{9}$$

Combining (8) and (9) yields

$$\left|\frac{Y}{X}[j(\omega_0 + \Delta\omega)]\right|^2 = \frac{1}{4Q^2}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \tag{10}$$

a familiar form previously derived for simple LC oscillators [4]. It is interesting to note that in an LC tank at resonance, $dA/d\omega = 0$ and (9) reduces to the third definition of Q given in Section III. In the two-integrator oscillator, on the other hand, $dA/d\omega = 2/\omega_0, d\Phi/d\omega = 0$, and $Q = 1$. Thus, the proposed definition of Q applies to most cases of interest.

To complete the discussion, we also consider the case shown in Fig. 9, where $H_1(j\omega)H_2(j\omega) = H(j\omega)$. Therefore, $Y(j\omega)/X(j\omega)$ is given by (5). For, $Y_1(j\omega)/X(j\omega)$, we have

$$\frac{Y_1}{X}(j\omega) = \frac{H_1(j\omega)}{1 + H(j\omega)} \tag{11}$$

giving the following noise shaping function:

$$\left|\frac{Y_1}{X}[j(\omega_0 + \Delta\omega)]\right|^2 = \frac{|H_1|^2}{(\Delta\omega)^2\left|\dfrac{dH}{d\omega}\right|^2}. \tag{12}$$

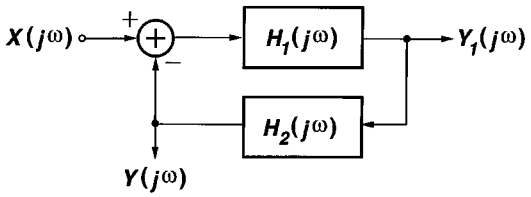


Fig. 9. Oscillatory system with nonunity-gain feedback.

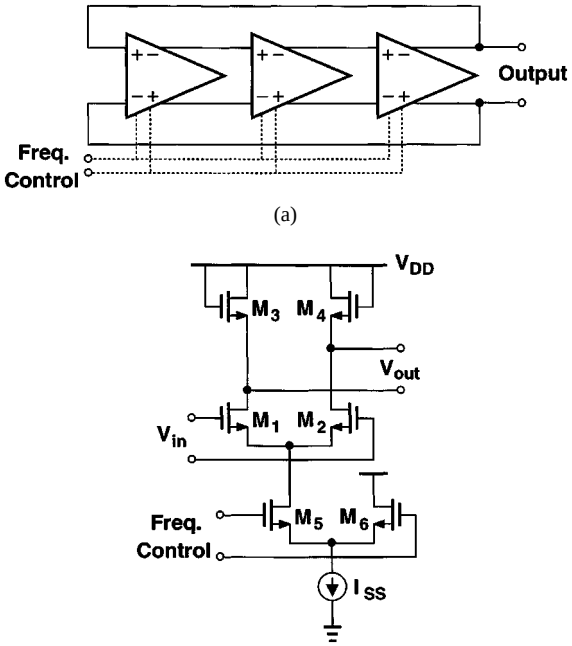


Fig. 10. CMOS VCO: (a) block diagram and (b) implementation of one stage.

V. CMOS Ring Oscillator

Submicron CMOS technologies have demonstrated potential for high-speed phase-locked systems [5], raising the possibility of designing fully integrated RF CMOS frequency synthesizers. Fig. 10 shows a three-stage ring oscillator wherein both the signal path and the control path are differential to achieve high common-mode rejection.

To calculate the phase noise, we model the signal path in the VCO with a linearized (single-ended) circuit (Fig. 11). As mentioned in Section IV, the linear approximation allows a first-order analysis of the topologies considered in this paper, but its accuracy must be checked if other oscillators are of interest. In Fig. 11, R and C represent the output resistance and the load capacitance of each stage, respectively, ($R \approx 1/g_{m3} = 1/g_{m4}$), and G_mR is the gain required for steady oscillations. The noise of each differential pair and its load devices are modeled as current sources I_{n1}–I_{n3}, injected onto nodes 1–3, respectively. Before calculating the noise transfer function, we note that the circuit of Fig. 11 oscillates if, at ω_0, each stage has unity voltage gain and 120° of phase shift. Writing the open-loop transfer function and imposing these two conditions, we have $\omega_0 = \sqrt{3}/(RC)$ and $G_mR = 2$. The

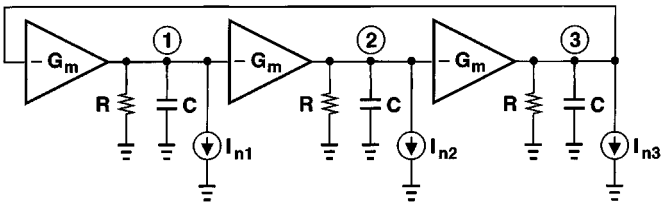


Fig. 11. Linearized model of CMOS VCO.

open-loop transfer function is thus given by

$$H(j\omega) = \frac{-8}{\left(1 + j\sqrt{3}\,\dfrac{\omega}{\omega_0}\right)^3}. \tag{13}$$

Therefore, $|dA/d\omega| = 9/(4\omega_0)$ and $|d\Phi/d\omega| = 3\sqrt{3}/(4\omega_0)$. It follows from (6) or (10) that if a noise current I_{n1} is injected onto node 1 in the oscillator of Fig. 11, then its power spectrum is shaped by

$$\left|\frac{V_1}{I_{n1}}[j(\omega_0 + \Delta\omega)]\right|^2 = \frac{R^2}{27}\left(\frac{\omega_0}{\Delta\omega}\right)^2. \tag{14}$$

This equation is the key to predicting various phase noise components in the ring oscillator.

VI. Additive and Multiplicative Noise

Modeling the ring oscillator of Fig. 10 with the linearized circuit of Fig. 11 entails a number of issues. First, while the stages in Fig. 10 turn off for part of the period, the linearized model exhibits no such behavior, presenting constant values for the components in Fig. 11. Second, the model does not predict mixing or modulation effects that result from nonlinearities. Third, the noise of the devices in the signal path has a "cyclostationary" behavior, i.e., periodically varying statistics, because the bias conditions are periodic functions of time. In this section, we address these issues, first identifying three types of noise: additive, high-frequency multiplicative, and low-frequency multiplicative.

A. Additive Noise

Additive noise consists of components that are directly added to the output as shown in Fig. 7 and formulated by (6) and (14).

To calculate the additive phase noise in Fig. 10 with the aid of (14), we note that for $\omega \approx \omega_0$ the voltage gain in each stage is close to unity. (Simulations of the actual CMOS oscillator indicate that for $\omega_0 = 2\pi \times 970$ MHz and noise injected at $\omega - \omega_0 = 2\pi \times 10$ MHz onto one node, the components observed at the three nodes differ in magnitude by less than 0.1 dB.) Therefore, the total output phase noise power density due to I_{n1}-I_{n3} is

$$|V_{1\text{tot}}[j(\omega_0 + \Delta\omega)]|^2 = \frac{R^2}{9}\left(\frac{\omega_0}{\Delta\omega}\right)^2 \overline{I_n^2} \tag{15}$$

where it is assumed $\overline{I_{n1}^2} = \overline{I_{n2}^2} = \overline{I_{n3}^2} = \overline{I_n^2}$. For the differential stage of Fig. 10, the thermal noise current per unit bandwidth

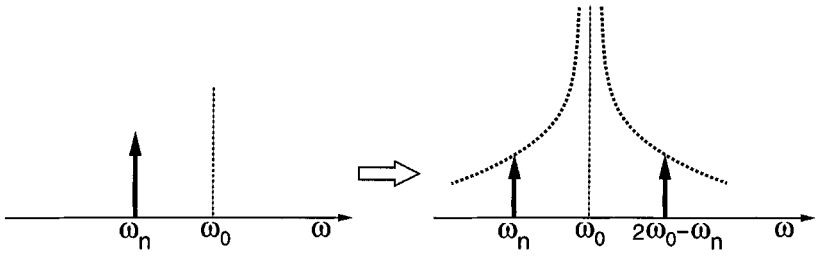


Fig. 12. High-frequency multiplicative noise.

is equal to $\overline{I_n^2} = 8kT(g_{m1} + g_{m3})/3 \approx 8kT/R$. Thus,

$$|V_{1\text{tot}}[j(\omega_0 + \Delta\omega)]|^2 = 8kT\frac{R}{9}\left(\frac{\omega_0}{\Delta\omega}\right)^2. \tag{16}$$

In this derivation, the thermal drain noise current of MOS devices is assumed equal to $\overline{i_n^2} = 4kT(2g_m/3)$. For short-channel devices, however, the noise may be higher [6]. Using a charge-based model in our simulation tool, we estimate the factor to be 0.873 rather than 2/3. In reality, hot-electron effects further raise this value.

Additive phase noise is predicted by the linearized model with high accuracy if the stages in the ring operate linearly for most of the period. In a three-stage CMOS oscillator designed for the RF range, the differential stages are in the linear region for about 90% of the period. Therefore, the linearized model emulates the CMOS oscillator with reasonable accuracy. However, as the number of stages increases or if each stage entails more nonlinearity, the error in the linear approximation may increase.

Since additive noise is shaped according to (16), its effect is significant only for components close to the carrier frequency.

B. High-Frequency Multiplicative Noise

The nonlinearity in the differential stages of Fig. 10, especially as they turn off, causes noise components to be multiplied by the carrier (and by each other). If the input/output characteristic of each stage is expressed as $V_{\text{out}} = \alpha_1 V_{\text{in}} + \alpha_2 V_{\text{in}}^2 + \alpha_3 V_{\text{in}}^3$, then for an input consisting of the carrier and a noise component, e.g., $V_{\text{in}}(t) = A_0 \cos\omega_0 t + A_n \cos\omega_n t$, the output exhibits the following important terms:

$$V_{\text{out}1}(t) \propto \alpha_2 A_0 A_n \cos(\omega_0 \pm \omega_n)t$$
$$V_{\text{out}2}(t) \propto \alpha_3 A_0 A_n^2 \cos(\omega_0 - 2\omega_n)t$$
$$V_{\text{out}3}(t) \propto \alpha_3 A_0^2 A_n \cos(2\omega_0 - \omega_n)t.$$

Note that $V_{\text{out}1}(t)$ appears in band if ω_n is small, i.e., if it is a *low-frequency* component, but in a fully differential configuration, $V_{\text{out}1}(t) = 0$ because $\alpha_2 = 0$. Also, $V_{\text{out}2}(t)$ is negligible because $A_n \ll A_0$, leaving $V_{\text{out}3}(t)$ as the only significant cross-product.

This simplified one-stage analysis predicts the *frequency* of the components in response to injected noise, but not their *magnitude*. When noise is injected into the oscillator, the magnitude of the observed response at ω_n and $2\omega_0 - \omega_n$ depends on the noise shaping properties of the feedback oscillatory system. Simulations indicate that for the oscillator topologies considered here, these two components have approximately equal magnitudes. Thus, the nonlinearity folds all the noise components below ω_0 to the region above and vice versa, effectively doubling the noise power predicted by (6). Such components are significant if they are close to ω_0 and are herein called high-frequency multiplicative noise. This phenomenon is illustrated in Fig. 12. (Note that a component at $3\omega_0 + \Delta\omega$ is also translated to $\omega_0 + \Delta\omega$, but its magnitude is negligible.)

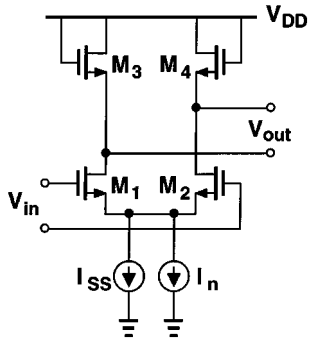


Fig. 13. Frequency modulation due to tail current noise.

This effect can also be viewed as sampling of the noise by the differential pairs, especially if each stage experiences hard switching. As each differential pair switches twice in every period, a noise component at ω_n is translated to $2\omega_0 \pm \omega_n$. Note that for highly nonlinear stages, the Taylor expansion considered above may need to include higher order terms.

C. Low-Frequency Multiplicative Noise

Since the frequency of oscillation in Fig. 10 is a function of the tail current in each differential pair, noise components in this current modulate the frequency, thereby contributing phase noise [classical frequency modulation (FM)]. Depicted in Fig. 13, this effect can be significant because, in CMOS oscillators, ω_0 must be adjustable by more than $\pm 20\%$ to compensate for process variations, thus making the frequency quite sensitive to noise in the tail current. This mechanism is illustrated in Fig. 14.

To quantify this phenomenon, we find the sensitivity or "gain" of the VCO, defined as $K_{\text{VCO}} = d\omega_{\text{out}}/dI_{SS}$ in Fig. 13, and use a simple approximation. If the noise per unit bandwidth in I_{SS} is represented as a sinusoid with the same

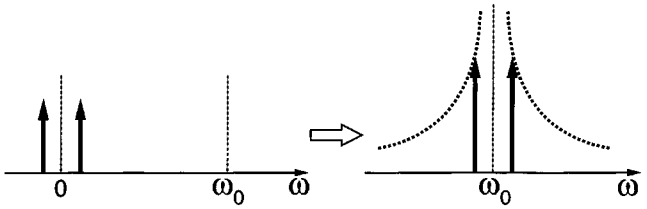


Fig. 14. Low-frequency multiplicative noise.

power: $I_m \cos \omega_m t$, then the output signal of the oscillator can be written as

$$v_{\text{out}}(t) = A_0 \cos\left(\omega_0 t + K_{\text{VCO}} \int I_m \cos \omega_m t \, dt\right) \quad (17)$$

$$= A_0 \cos\left(\omega_0 t + \frac{K_{\text{VCO}}}{\omega_m} I_m \sin \omega_m t\right). \quad (18)$$

For $K_{\text{VCO}} I_m / \omega_m \ll 1$ radian ("narrowband FM")

$$v_{\text{out}}(t) \approx A_0 \cos \omega_0 t + \frac{A_0 I_m K_{\text{VCO}}}{2\omega_m} \cdot [\cos(\omega_0 + \omega_m)t - \cos(\omega_0 - \omega_m)t]. \quad (19)$$

Thus, the ratio of each sideband amplitude to the carrier amplitude is equal to $I_m K_{\text{VCO}}/(2\omega_m)$, i.e.,

$$|V_n|^2(\text{with respect to carrier}) = \frac{1}{4}\left(\frac{K_{\text{VCO}}}{\omega_m}\right)^2 I_m^2. \quad (20)$$

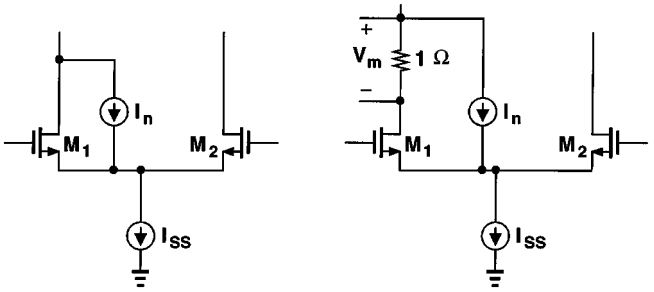
Since K_{VCO} can be easily evaluated in simulation or measurement, (20) is readily calculated.

It is seen that modulation of the carrier brings the low frequency noise components of the tail current to the band around ω_0. Thus, flicker noise in I_n becomes particularly important.

In the differential stage of Fig. 3(b), two sources of low-frequency multiplicative noise can be identified: noise in I_{SS} and noise in M_5 and M_6. For comparable device size, these two sources are of the same order and must be both taken into account.

D. Cyclostationary Noise Sources

As mentioned previously, the devices in the signal path exhibit cyclostationary noise behavior, requiring the use of periodically varying noise statistics in analysis and simulations. To check the accuracy of the stationary noise approximation, we perform a simple, first-order simulation on the two cases depicted in Fig. 15. In Fig. 15(a), a sinusoidal current source with an amplitude of 2 nA is connected between the drain and source of M_1 to represent its noise with the assumption that M_1 carries half of I_{SS}. In Fig. 15(b), the current source is also a sinusoid, but its amplitude is a function of the drain current of M_1. Since MOS thermal noise current (in the saturation region) is proportional to $\sqrt{g_m}$, we use a nonlinear dependent source in SPICE [7] as $I_n(t) = \alpha \sqrt[4]{V_m(t)} \sin \omega_n t$, where $\omega_n = 2\pi \times 980$ MHz. The factor α is chosen such that $I_n(t) = 2\ \text{nA} \times \sin \omega_n t$ when $V_m(t) = 1\ \Omega \times I_{SS}/2$ (balanced



(a) (b)

Fig. 15. Gain stage with (a) stationary and (b) cyclostationary noise.

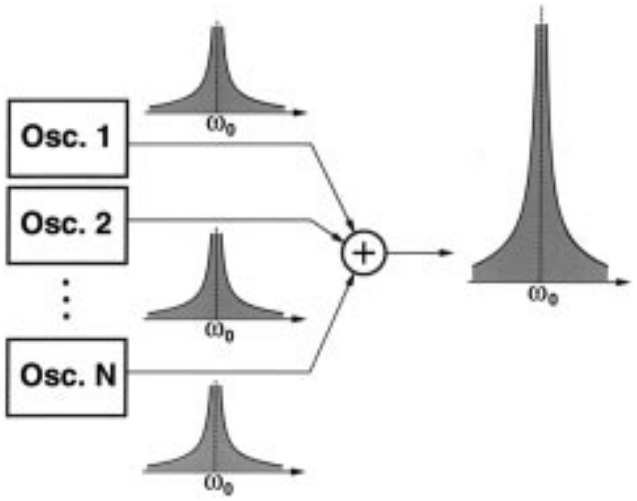


Fig. 16. Addition of output voltages of N oscillators.

condition). Simulations indicate that the sideband magnitudes in the two cases differ by less than 0.5 dB.

It is important to note that this result may not be accurate for other types of oscillators.

E. Power-Noise Trade-Off

As with other analog circuits, oscillators exhibit a trade-off between power dissipation and noise. Intuitively, we note that if the output voltages of N identical oscillators are added in phase (Fig. 16), then the total carrier power is multiplied by N^2, whereas the noise power increases by N (assuming noise sources of different oscillators are uncorrelated). Thus, the phase noise (relative to the carrier) decreases by a factor N at the cost of a proportional increase in power dissipation.

Using the equations developed above, we can also formulate this trade-off. For example, from (16), since $G_m R \approx 2$, we have

$$|V_{n\text{tot}}|^2 = 8kT \frac{2}{9G_m}\left(\frac{\omega_0}{\Delta\omega}\right)^2. \quad (21)$$

To reduce the total noise power by N, G_m must increase by the same factor. For any active device, this can be accomplished by increasing the width and the bias current by N. (To maintain the same frequency of oscillation, the load resistor is reduced by N.) Therefore, for a constant supply voltage, the power dissipation scales up by N.

TABLE I
COMPARISON OF THREE-STAGE AND FOUR-STAGE RING OSCILLATORS

	3-Stage VCO	4-Stage VCO
Minimum Required DC Gain	2	$\sqrt{2}$
Noise Shaping Function	$\frac{R^2}{27}(\frac{\omega_0}{\Delta\omega})^2$	$\frac{R^2}{16}(\frac{\omega_0}{\Delta\omega})^2$
Open-Loop Q	$\frac{3\sqrt{3}}{4}$ (≈ 1.3)	$\sqrt{2}$ (≈ 1.4)
Total Additive Noise	$8kT\frac{R}{9}(\frac{\omega_0}{\Delta\omega})^2$	$8kT\frac{R(1+\sqrt{2})}{12}(\frac{\omega_0}{\Delta\omega})^2$
Power Dissipation	1.8 mW	3.6 mW

F. Three-Stage Versus Four-Stage Oscillators

The choice of number of stages in a ring oscillator to minimize the phase noise has often been disputed. With the above formulations, it is possible to compare rings with different number of stages (so long as the approximations remain valid). For the cases of interest in RF applications, we consider three-stage and four-stage oscillators designed to operate at the same frequency. Thus, the four-stage oscillator incorporates smaller impedance levels and dissipates more power. Table I compares various aspects of the two circuits. We make three important observations. 1) Simulations show that if the four-stage oscillator is to operate at the same speed as the three-stage VCO, the value of R in the former must be approximately 60% of that in the latter. 2) The Q's of the two VCO's (10) are roughly equal. 3) The total additive thermal noise of the two VCO's is about the same, because the four-stage topology has more sources of noise, but with lower magnitudes.

From these rough calculations, we draw two conclusions. First, the phase noise depends on not only the Q, but the number and magnitude of sources of noise in the circuit. Second, four-stage VCO's have no significant advantage over three-stage VCO's, except for providing quadrature outputs.

G. Supply and Substrate Noise

Even though the gain stage of Fig. 10 is designed as a differential circuit, it nonetheless suffers from some sensitivity to supply and substrate noise (Fig. 17). Two phenomena account for this. First, device mismatches degrade the symmetry of the circuit. Second, the total capacitance at the common source of the differential pair (i.e., the source junction capacitance of M_1 and M_2 and the capacitance associated with the tail current source) converts the supply and substrate noise to current, thereby modulating the delay of the gain stage. Simulations indicate that even if the tail current source has a high dc output impedance, a 1-mV_{pp} supply noise component at 10 MHz generates sidebands 60 dB below the carrier at $\omega_0 \pm (2\pi \times 10$ MHz).

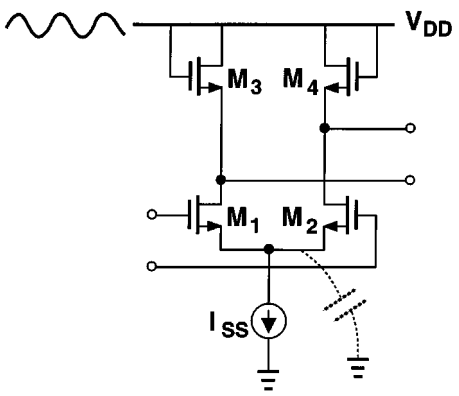


Fig. 17. Substrate and supply noise in gain stage.

VII. CMOS RELAXATION OSCILLATOR

In this section, we apply the analysis methodology described thus far to a CMOS relaxation oscillator [Fig. 18(a)]. When designed to operate at 900 MHz, this circuit hardly "relaxes" and the signals at the drain and source of M_1 and M_2 are close to sinusoids. Thus, the linear model of Fig. 7 is a plausible choice. To utilize our previous results, we assume the signals at the sources of M_1 and M_2 are fully differential[1] and redraw the circuit as in Fig. 18(b), identifying it as a two-stage ring with capacitive degeneration ($C_A = 2C$). The total capacitance seen at the drain of M_1 and M_2 is modeled with C_1 and C_2, respectively. (This is also an approximation because the input impedance of each stage is not purely capacitive.) It can be easily shown that the open-loop transfer function is

$$H(s) = \left[\frac{-g_m R C_A s}{(g_m + C_A s)(RC_D s + 1)}\right]^2 \tag{22}$$

where $C_1 = C_2 = C_D$ and g_m denotes the transconductance of each transistor. For the circuit to oscillate at $\omega_0, H(j\omega_0) = 1$, and each stage must have a phase shift of 180°, with 90° contributed by each zero and the remaining 90° by the two poles at $-g_m/C_A$ and $-1/(RC_D)$. It follows from the second condition that

$$\omega_0^2 = \frac{g_m}{RC_A C_D} \tag{23}$$

i.e., ω_0 is the geometric mean of the poles at the drain and source of each transistor. Combining this result with the first condition, we obtain

$$g_m R = \frac{C_A}{C_A - C_D}. \tag{24}$$

After lengthy calculations, we have

$$\left|\frac{dH}{d\omega}\right| = \frac{4}{RC_A\omega_0^2} \tag{25}$$

and

$$Q^2 = 4\left(1 - \frac{C_D}{C_A}\right)\frac{C_D}{C_A}. \tag{26}$$

[1]This assumption is justified by decomposing C into two series capacitors, each one of value $2C$, and monitoring the midpoint voltage. The common-mode swing at this node is approximatley 18 dB below the differential swings at the source of M_1 and M_2.

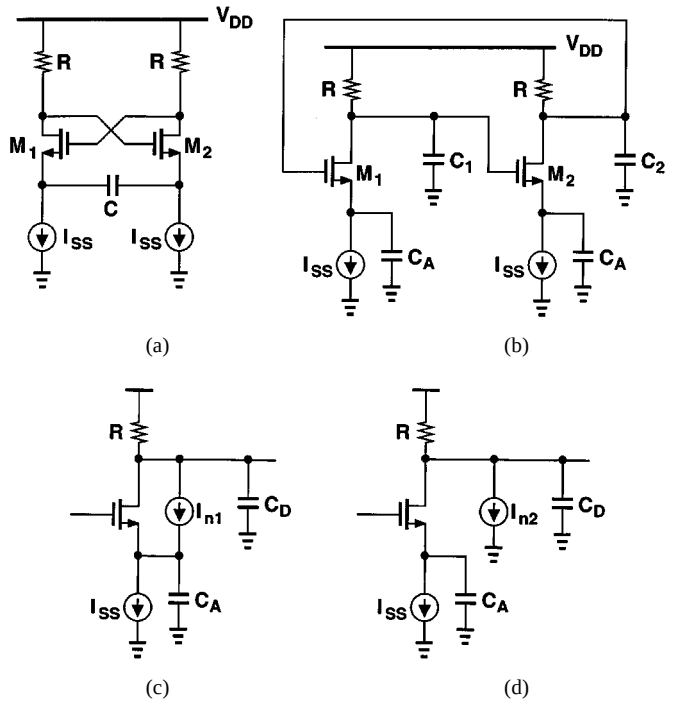


Fig. 18. (a) CMOS relaxation oscillator, (b) circuit of (a) redrawn, (c) noise current of one transistor, and (d) transformed noise current.

For $C_D = 0.5C_A, Q$ reaches its maximum value—unity. In other words, the maximum Q occurs if the (floating) timing capacitor is equal to the load capacitance. The noise shaping function is therefore equal to $(\omega_0/\Delta\omega)^2/4$.

Since the drain-source noise current of M_1 and M_2 appears between two internal nodes of the circuit [Fig. 18(c)], the transformation shown in Fig. 18(d) can be applied to allow the use of our previous derivations. It can be shown that

$$I_{n2} = \frac{C_A s}{g_m + C_A s} I_{n1} \tag{27}$$

and the total additive thermal noise observed at each drain is

$$\overline{V_n^2} = \frac{10}{3} kTR\left(\frac{\omega_0}{\Delta\omega}\right)^2. \tag{28}$$

This power must be doubled to account for high-frequency multiplicative noise.

VIII. Simulation Results

A. Simulation Issues

The time-varying nature of oscillators prohibits the use of the standard small-signal ac analysis available in SPICE and other similar programs. Therefore, simulations must be performed in the time domain. As a first attempt, one may generate a pseudo-random noise with known distribution, introduce it into the circuit as a SPICE piecewise linear waveform, run a transient analysis for a relatively large number of oscillation periods, write the output as a series of points equally spaced in time, and compute the fast Fourier transform (FFT) of the output. The result of one such attempt is shown in Fig. 19. It is important to note that 1) many coherent sidebands

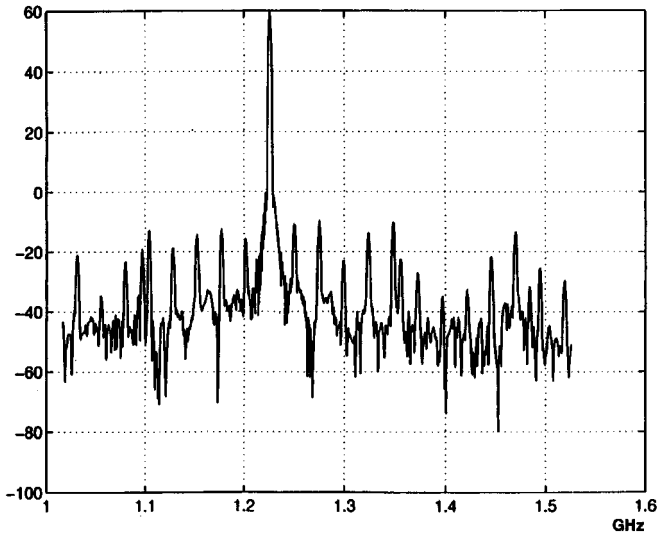


Fig. 19. Simulated oscillator spectrum with injected white noise.

appear in the spectrum even though the injected noise is white, and 2) the magnitude of the sidebands does not directly scale with the magnitude of the injected noise!

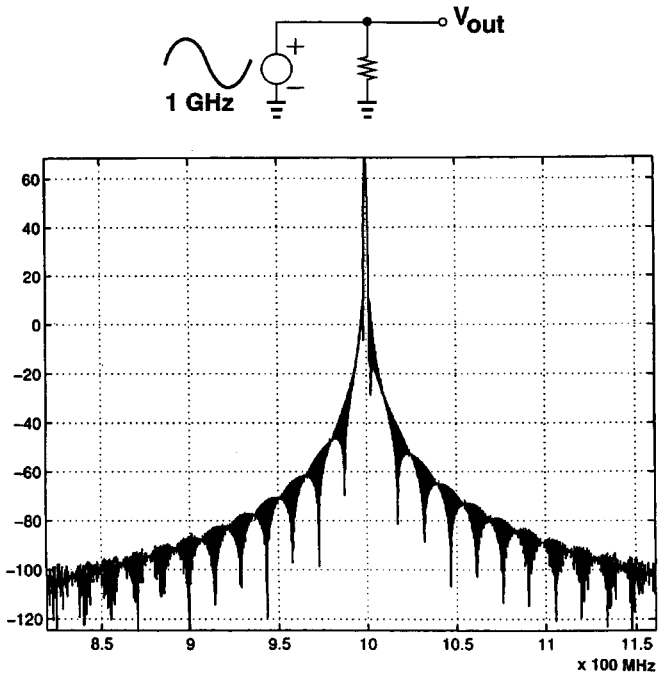
To understand the cause of this behavior, consider a much simpler case, illustrated in Fig. 20. In Fig. 20(a), a sinusoid at 1 GHz is applied across a 1-kΩ resistor, and a long transient simulation followed by interpolation and FFT is used to obtain the depicted spectrum. (The finite width results from the finite length of the data record and the "arches" are attributed to windowing effects.) Now, as shown in Fig. 20(b), we add a 30-MHz squarewave with 2 ns transition time and proceed as before. Note that the two circuits share only the ground node. In this case, however, the spectrum of the 1-GHz sinusoid exhibits coherent sidebands with 15 MHz spacing! Observed in AT&T's internal simulator (ADVICE), HSPICE, and Cadence SPICE, this effect is attributed to the additional points that the program must calculate at each edge of the squarewave, leading to errors in subsequent interpolation.

Fortunately, this phenomenon does not occur if only sinusoids are used in simulations.

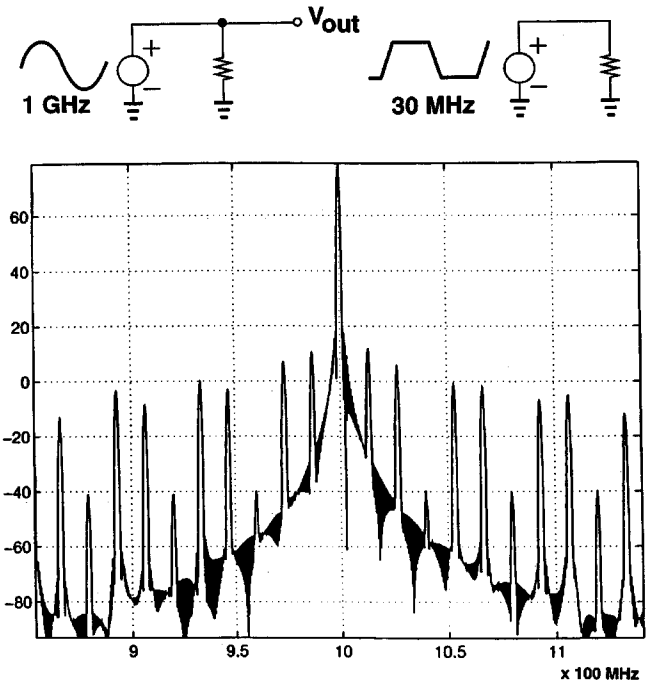
B. Oscillator Simulations

In order to compute the response of oscillators to each noise source, we approximate the noise per unit bandwidth at frequency ω_n with an impulse (a sinusoid) of the same power at that frequency. As shown in Fig. 21, the "sinusoidal noise" is injected at various points in the circuit and the output spectrum is observed. This approach is justified by the fact that random Gaussian noise can be expressed as a Fourier series of sinusoids with random phase [8], [9]. Since only one sinusoid is injected in each simulation, the interaction among noise components themselves is assumed negligible, a reasonable approximation because if two noise components at, say, -60 dB are multiplied, the product is at -120 dB.

In the simulations, the oscillators were designed for a center frequency of approximately 970 MHz. Each circuit and its linearized models were simulated in the time domain in steps



(a)



(b)

Fig. 20. Simple simulation revealing effect of pulse waveforms, (a) single sinusoidal source and (b) sinusoidal source along with a square wave generator.

of 30 ps for 8 μs, and the output was processed in MATLAB to obtain the spectrum. Since simulations of the linear model yield identical results to the equations derived above, we will not distinguish between the two hereafter.

Shown in Fig. 22 are the output spectra of the linear model and actual circuit of a three-stage oscillator in 0.5-μm CMOS technology with a 2-nA_p 980-MHz sinusoidal current injected into the signal path (the drain of one of the differential pairs).

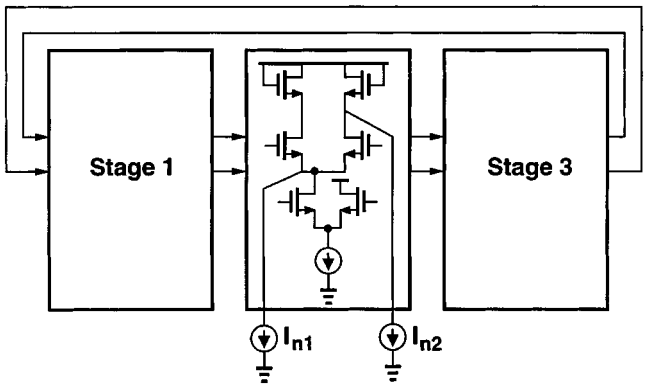


Fig. 21. Simulated configuration.

The vertical axis represents $10 \log V_{\mathrm{rms}}^2$. Note that the observed magnitude of the 980-MHz component differs by less than 0.2 dB in the two cases, indicating that the linearized model is indeed an accurate representation. As explained in Section VI-B, the 960-MHz component originates from third-order mixing of the carrier and the 980-MHz component and essentially doubles the phase noise.

In order to investigate the limitation of the linear model, the oscillator was made progressively more nonlinear. Shown in Fig. 23 is the output spectra of a four-stage CMOS oscillator, revealing approximately 1 dB of error in the prediction by the linear model. The error gradually increases with the number of stages in the ring and reaches nearly 6 dB for an eight-stage oscillator.

For bipolar ring oscillators (differential pairs with no emitter followers), simulations reveal an error of approximately 2 dB for three stages and 7 dB for four stages in the ring.

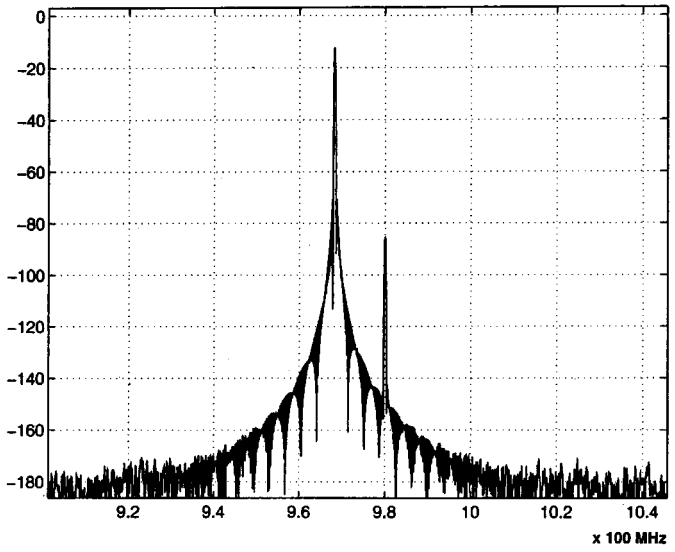
IX. Experimental Results

A. Measurements

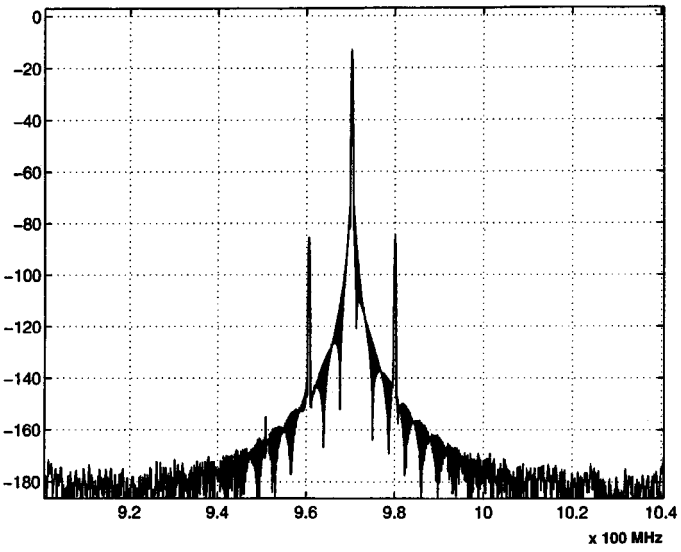
Two different oscillator configurations have been fabricated in a 0.5-μm CMOS technology to compare the predictions in this paper with measured results. Note that there are three sets of results: theoretical calculations based on linear models but including multiplicative noise, simulated predictions based on the actual CMOS oscillators, and measured values.

The first circuit is a 2.2-GHz three-stage ring oscillator. Fig. 24 shows one stage of the circuit along with the measured device parameters. The sensitivity of the output frequency to the tail current of each stage is about 0.43 MHz/μA. The measured spectrum is depicted in Fig. 25(a) and (b) with two different horizontal scales. Due to lack of data on the flicker noise of the process, we consider only thermal noise at relatively large frequency offsets, namely, 1 MHz and 5 MHz.

It is important to note that low-frequency flicker noise causes the center of the spectrum to fluctuate constantly. Thus, as the resolution bandwidth (RBW) of the spectrum analyzer is reduced [from 1 MHz in Fig. 25(a) to 100 kHz in Fig. 25(b)], the carrier power is subject to more averaging and appears to decrease. To maintain consistency with calculations, in which

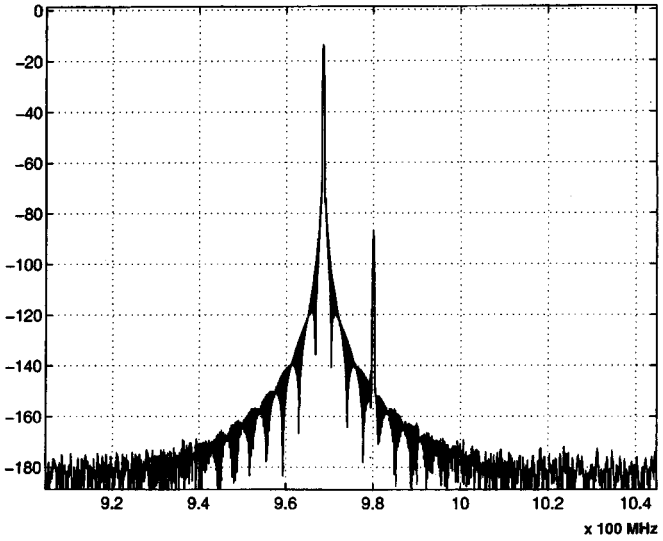


(a)

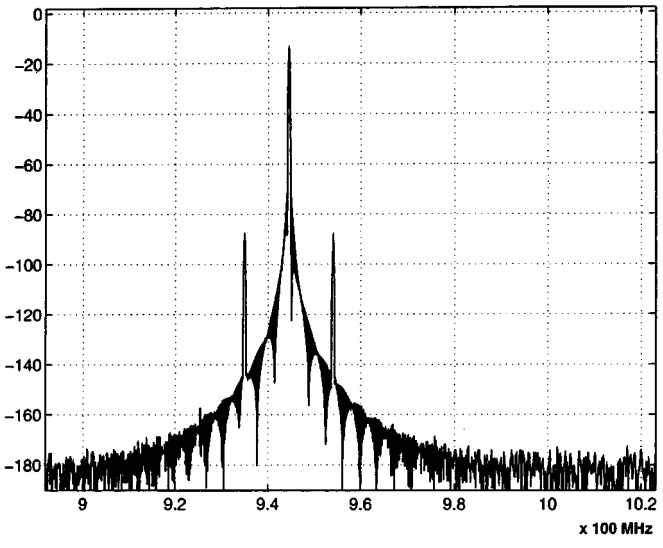


(b)

Fig. 22. Simulated output spectra of (a) linear model and (b) actual circuit of a three-stage CMOS oscillator.



(a)



(b)

Fig. 23. Simulated output spectra of (a) linear model and (b) actual circuit of a four-stage CMOS oscillator.

the phase noise is normalized to a *constant* carrier power, this power (i.e., the output amplitude) is measured using an oscilloscope.

The noise calculation proceeds as follows. First, find the additive noise power in (16), and double the result to account for third-order mixing (high-frequency multiplicative noise). Next, calculate the low-frequency multiplicative noise from (20) for one stage and multiply the result by three. We assume (from simulations) that the internal differential voltage swing is equal to 1 V_{pp} (0.353 V_{rms}) and the drain noise current of MOSFET's is given by $\overline{i_n^2} = 4kT(0.863g_m)$. For $\Delta\omega = 2\pi \times 1$ MHz, calculations yield

$$\text{high-frequency multiplicative noise} = -100.1 \text{ dBc/Hz} \quad (29)$$

$$\text{low-frequency multiplicative noise} = -106.3 \text{ dBc/Hz} \quad (30)$$

$$\text{total normalized phase noise} = -99.2 \text{ dBc/Hz}. \quad (31)$$

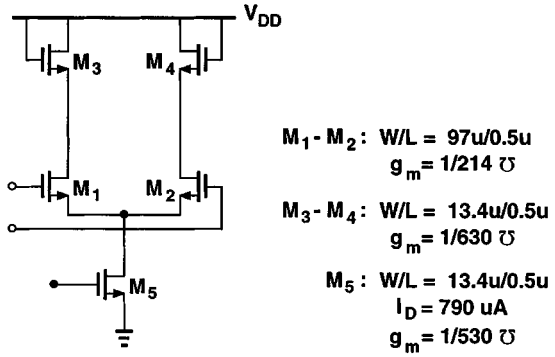
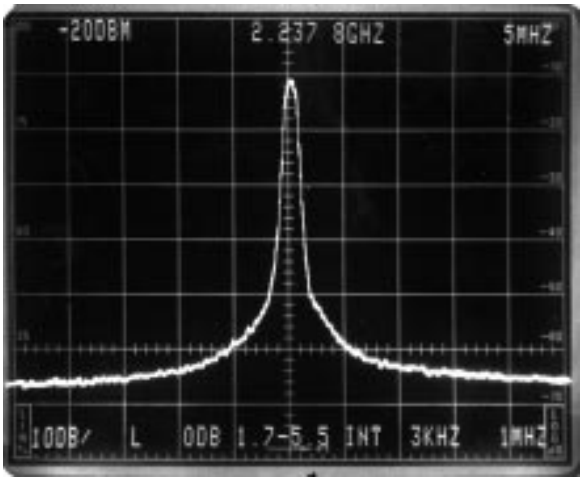
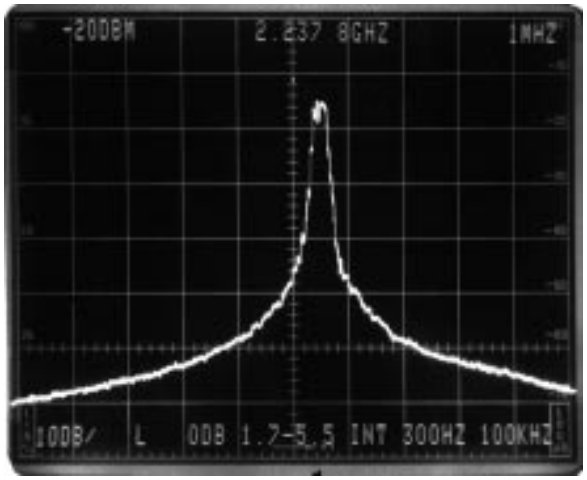


Fig. 24. Gain stage used in 2-GHz CMOS oscillator.

Simulations of the actual CMOS oscillator predict the total noise to be −98.1 dBc/Hz. From Fig. 25(b), with the carrier power of Fig. 25(a), the phase noise is approximately equal to −94 dBc/Hz.



(a)



(b)

Fig. 25. Measured output spectrum of ring oscillator (10 dB/div. vertical scale). (a) 5 MHz/div. horizontal scale and 1 MHz resolution bandwidth, (b) 1 MHz horizontal scale and 100 kHz resolution bandwidth.

Similarly, for $\Delta\omega = 2\pi \times 5$ MHz, calculations yield

$$\text{high-frequency multiplicative noise} = -114.0 \text{ dBc/Hz} \quad (32)$$

$$\text{low-frequency multiplicative noise} = -120.2 \text{ dBc/Hz} \quad (33)$$

$$\text{total normalized phase noise} = -113.1 \text{ dBc/Hz} \quad (34)$$

and simulations predict -112.4 dBc/Hz, while Fig. 25(a) indicates a phase noise of -109 dBc/Hz. Note that these values correspond to a center frequency of 2.2 GHz and should be lowered by approximately 8 dB for 900 MHz operation, as shown in (9).

The second circuit is a 920-MHz relaxation oscillator, depicted in Fig. 26. The measured spectra are shown in Fig. 27. Since simulations indicate that the low-frequency multiplicative noise is negligible in this implementation, we consider only the thermal noise in the signal path. For $\Delta\omega = 2\pi \times 1$ MHz, calculations yield a relative phase noise of -105 dBc/Hz, simulations predict -98 dB, and the spectrum in Fig. 27 gives -102 dBc/Hz. For $\Delta\omega = 2\pi \times 5$ MHz, the calculated and simulated results are -119 dBc/Hz and

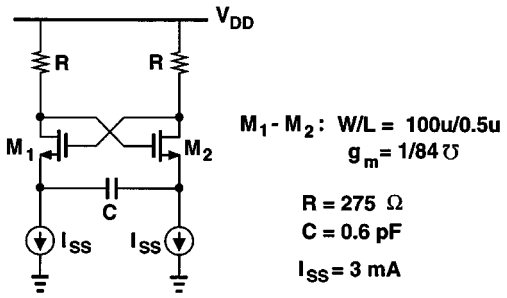
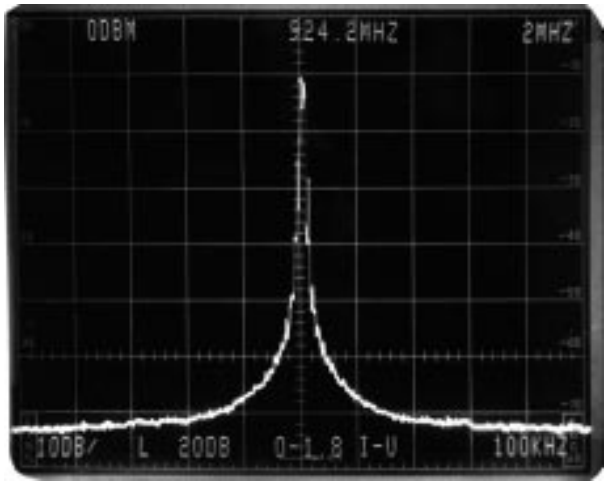
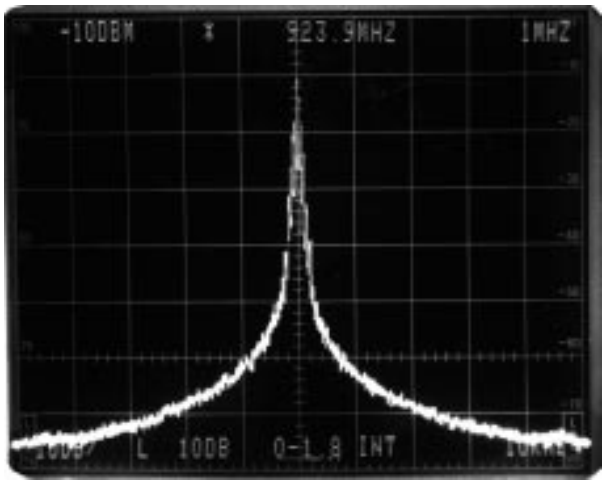


Fig. 26. Relaxation oscillator parameters.



(a)



(b)

Fig. 27. Measured output spectrum of relaxation oscillator (10 dB/div. vertical scale). (a) 2 MHz/div. horizontal scale and 100 kHz resolution bandwidth and (b) 1 MHz horizontal scale and 10 kHz resolution bandwidth.

-120 dBc/Hz, respectively, while the measured value is -115 dBc/Hz.

B. Discussion

Using the above measured data points and assuming a noise shaping function as in (10) with a linear noise-power trade-off (Fig. 16), we can make a number of observations.

How much can the phase noise be lowered by scaling device dimensions? If the gate oxide of MOSFET's is reduced indefinitely, their transconductance becomes relatively independent of their dimensions, approaching roughly that of bipolar transistors. Thus, in the gain stage of Fig. 24 the transconductance of M_1 and M_2 (for $I_{D1} = I_{D2} = 395\ \mu\text{A}$) would go from $(214\ \Omega)^{-1}$ to $(66\ \Omega)^{-1}$. Scaling down the load resistance proportionally and assuming a constant oscillation frequency, we can therefore lower the phase noise by $10\log(214/66) \approx 5$ dB. For the relaxation oscillator, on the other hand, the improvement is about 10 dB. These are, of course, greatly simplified calculations, but they provide an estimate of the maximum improvement expected from technology scaling. In reality, short-channel effects, finite thickness of the inversion layer, and velocity saturation further limit the transconductance that can be achieved for a given bias current.

It is also instructive to compare the measured phase noise of the above ring oscillator with that of a 900-MHz three-stage CMOS ring oscillator reported in [10]. The latter employs single-ended CMOS inverters with rail-to-rail swings in a 1.2-μm technology and achieves a phase noise of -83 dBc/Hz at 100 kHz offset while dissipating 7.4 mW from a 5-V supply. Assuming that

$$\text{Relative Phase Noise} \propto \left(\frac{\omega_0}{\Delta\omega}\right)^2 \frac{1}{V_{\text{swing}^2}} \frac{1}{I_{DD}} \tag{35}$$

where V_{swing} denotes the internal voltage swing and I_{DD} is the total supply current, we can utilize the measured phase noise of one oscillator to roughly estimate that of the other. With the parameters of the 2.2-GHz oscillator and accounting for different voltage swings and supply currents, we obtain a phase noise of approximately -93 dBc/Hz at 100 kHz offset for the 900-MHz oscillator in [10]. The 10 dB discrepancy is attributed to the difference in the minimum channel length, $1/f$ noise at 100 kHz, and the fact that the two circuits incorporate different gain stages.

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