A 2-GHz 1.6-mW Phase-Locked Loop

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***Abstract*—This paper describes the design of a 2-GHz 1.6-mW phase-locked loop (PLL) fabricated in an 18-GHz 0.6-μm BiCMOS technology. Employing cross-coupled delay elements and inductive peaking, the circuit merges the oscillator and the mixer into one stage to lower the power dissipation. An experimental prototype exhibits an rms jitter of 2.8 ps, a tracking range of 100 MHz, and a capture range of 70 MHz while operating from a 3-V supply. The phase noise in the locked condition is −115 dBc/Hz at 400 kHz offset.**

***Index Terms*— Analog circuits, frequency synthesizers, phase-locked loops.**

I. Introduction

HIGH-SPEED low-power phase-locked loops (PLL's) are an integral part of frequency synthesizers and clock recovery circuits. The power dissipation of gigahertz PLL's becomes particularly critical in portable wireless terminals as well as highly integrated multichannel fiber optic receivers [1].

This paper describes the design of a 2-GHz 1.6-mW PLL that has been fabricated in an 18-GHz 0.6-μm BiCMOS technology. Originating from a one-stage oscillator, the PLL employs various circuit techniques to lower the power dissipation while operating at a high speed. An experimental prototype of the circuit exhibits an rms jitter of 2.8 ps, a tracking range of 100 MHz, and a capture range of 70 MHz while running from a 3-V supply. The measured phase noise in the locked condition is equal to −115 dBc/Hz at 400 kHz offset.

Section II of the paper presents the PLL architecture and Section III deals with phase shift issues in ring oscillators. Section IV describes the evolution of the circuit and Section V presents the complete PLL. Section VI summarizes the experimental results.

II. PLL Architecture

Fig. 1 shows the architecture of the PLL, a fairly standard topology consisting of an input mixer, a low-pass filter (LPF), a low-frequency amplifier A_1, and a voltage-controlled oscillator (VCO). The shaded box is to indicate that the enclosed three functions are merged and performed in only one stage so as to achieve a compact circuit implementation.

The PLL incorporates fully differential circuits in both the high-frequency signal path and the frequency control path to improve the common-mode rejection.

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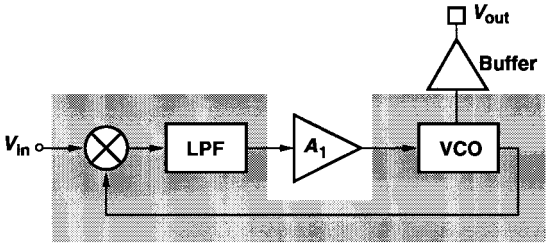


Fig. 1. Phase-locked loop architecture.

The design of the PLL has evolved from a one-stage ring oscillator, and it is described in a progression starting from the VCO circuit. To this end, we first consider issues in reducing the number of stages in a ring oscillator.

III. Phase Shift Issues in Ring Oscillators

Ring oscillators have been widely used as VCO's in phase-locked systems [2]–[4]. Providing a wide tuning range with relatively constant voltage swings, these oscillators also lend themselves to low-voltage operation.

From the viewpoint of speed–power tradeoff, it is desirable to decrease the number of stages in a ring to the extent possible. We note that if the number of stages is reduced by a factor of two, then the circuit can potentially oscillate at twice the frequency because the total delay around the loop is halved. Furthermore, the oscillator dissipates half as much power. Thus, for a given frequency of oscillation, the power dissipation decreases with roughly the *square* of the number of stages in the ring. While three-stage and two-stage oscillators have been used successfully [2], [3], [5], this trend makes it attractive to consider one-stage topologies.

For steady oscillation, however, the total phase shift around the loop must be equal to zero. As depicted in Fig. 2, in a three-stage ring each stage contributes 60° of frequency-dependent phase shift and 180° of dc phase shift, providing a total of 360°. In a two-stage circuit, each stage must exhibit an ac phase shift of 90°, usually requiring more than one pole [5]. Finally, in a single-stage loop, the signal must experience an ac phase shift of 180° at the frequency of oscillation in addition to the dc inversion.

From the above observations, we note that establishing sufficient phase shift becomes progressively more difficult as the number of stages in a ring is reduced. This issue can be considered in conjunction with the other condition for oscillation: unity loop gain. As illustrated in Fig. 3, insufficient phase shift means that at the frequency where the phase shift reaches 180°, the loop gain is less than one. In other words, the gain and phase crossover points do not coincide, and the

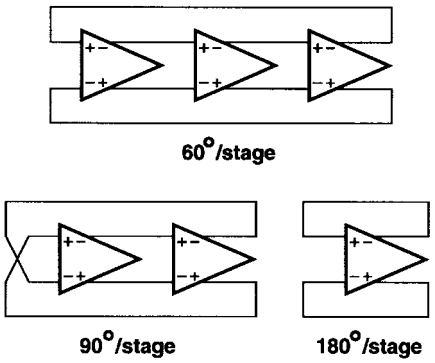


Fig. 2. Phase shift required in ring oscillators.

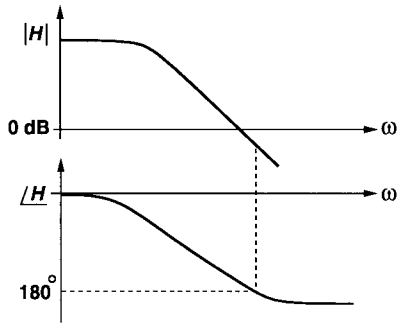


Fig. 3. Problem of insufficient phase shift.

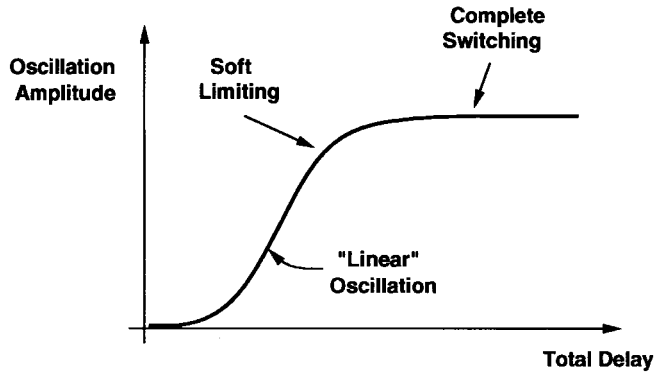


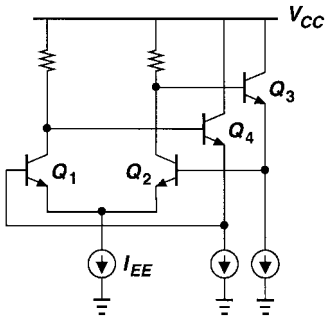
Fig. 4. Oscillation amplitude versus total delay.

two oscillation criteria cannot be met simultaneously. As more delay is introduced in the loop, the circuit eventually begins to oscillate but with a small amplitude so that the operation is linear and the gain is maximum-unity. As shown in Fig. 4, with further increase in the delay, the small-signal gain for which the phase shift is equal to 180° becomes greater than one, and the oscillator experiences soft limiting. For a sufficiently large delay, the circuit exhibits full switching.

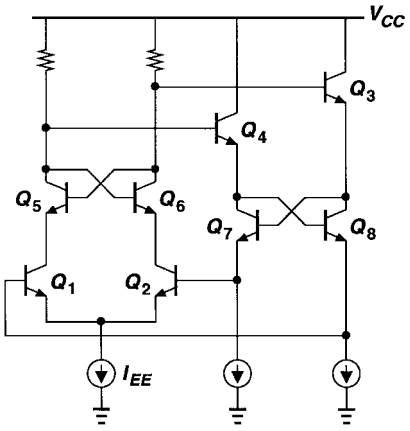
This intuitive study proves useful in designing "short" ring oscillators.

IV. Oscillator and Mixer Circuits

Consider the feedback differential stage of Fig. 5(a), which fails to oscillate because of insufficient phase shift. To overcome this problem, as shown in Fig. 5(b), cross-coupled



(a)



(b)

Fig. 5. (a) Simple differential stage with feedback and (b) addition of cross-coupled pairs.

pairs Q_5-Q_6 and Q_7-Q_8 are inserted in the signal path, thereby introducing a significant delay. At 2 GHz, the parasitic capacitances at the emitters of these four transistors provide a relatively low equivalent impedance to ground, allowing the positive feedback around each pair to contribute substantial phase shift. Simulations indicate that the modified circuit indeed oscillates, but the total delay is not enough to permit complete switching. This issue will be resolved later by inductive peaking.

With the basic oscillator designed, we now consider its interface with the mixer. Let us examine the collector currents of Q_3 and Q_4. Shown in Fig. 6 are the simulated waveforms for a bias current of 50 μA. The peak current in each transistor is approximately equal to 65 μA because of the displacement current required to charge parasitic capacitances from the emitters of Q_3-Q_4 to ground. The minimum current is about 30 μA. Thus, I_{C3} and I_{C4} experience a swing of 35 μA and can therefore be considered as the outputs of the oscillator.

Since the oscillator output is available in the current domain, mixing assumes a simple form. Stacking two differential pairs driven by the input on top of the emitter followers, we arrive at a circuit similar to a Gilbert cell [Fig. 7(a)]. With a current swing of 35 μA in Q_3 and Q_4, the gain of this mixer is close to that of a Gilbert cell having a total bias current of 70 μA.

In the circuit of Fig. 7(a), the addition of the switching quad drives Q_3 and Q_4 into saturation. To overcome

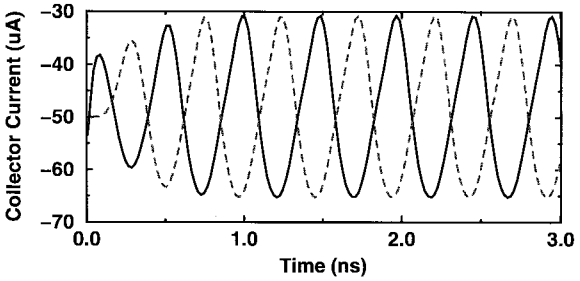


Fig. 6. Collector currents of Q_3 and Q_4 as a function of time.

this problem, as shown in Fig. 7(b), the voltage level at nodes G and H is shifted down by means of transistors Q_9 and Q_{10}. Also, resistors R_{B1} and R_{B2} are placed in series with the base of each device to create inductive peaking at their emitters. The resulting resonance boosts the gain and, more importantly, the voltage swings at nodes G and H, allowing more complete switching in the circuit. To further increase the speed, small currents are pulled from nodes A, B, M, and N with negligible power penalty. Small NMOS transistors ($W/L = 1.6\ \mu$m/0.6 μm) with low parasitics prove especially useful in the implementation of these current sources.

The compact, low-power topology of Fig. 7(b) suffers from an important limitation: a minimum supply voltage of $4V_{BE}$. This can be seen in the path comprising the base-emitter junctions of Q_9, Q_4, Q_8, and Q_1 (and a similar path through Q_{10}, Q_3, Q_7, and Q_2). To circumvent this difficulty, we note that the feedback signal at nodes E and F can be coupled to the *emitters* of Q_1 and Q_2, with a swap in the differential voltages to maintain negative feedback. Illustrated in Fig. 8(a), such a modification places Q_1 and Q_2 in a common-base configuration.

The value of the bias voltage V_b in Fig. 8(a) is critical because it determines how I_E and I_F are shared between the common-base transistors and the cross-coupled devices. Rather than generate V_b using a replica circuit, we make an observation. The signals at nodes M and N are similar to those at F and E, respectively, but with a common-mode level that is one V_{BE} higher. Thus, as shown in Fig. 8(b), the bases of Q_1 and Q_2 can be connected to nodes M and N, respectively. Note that this technique also doubles the loop gain because the base and emitter voltages of Q_1 and Q_2 now change in opposite directions.

Simulations indicate that, owing to the finite output impedance of the NMOS current sources used in the VCO, the frequency of oscillation has a sensitivity of approximately 5 MHz/V with respect to the supply voltage. Lower sensitivities can be attained by increasing the length of the NMOS devices.

V. Complete PLL

Fig. 9 shows the PLL circuit excluding the low-frequency amplifier A_1. in order to vary the frequency of the oscillator, differential pairs Q_{11}-Q_{12} and Q_{13}-Q_{14} adjust the turn-on delay of Q_5 and Q_6. Plotted in Fig. 10 is the simulated output frequency of the VCO as a function of the differential

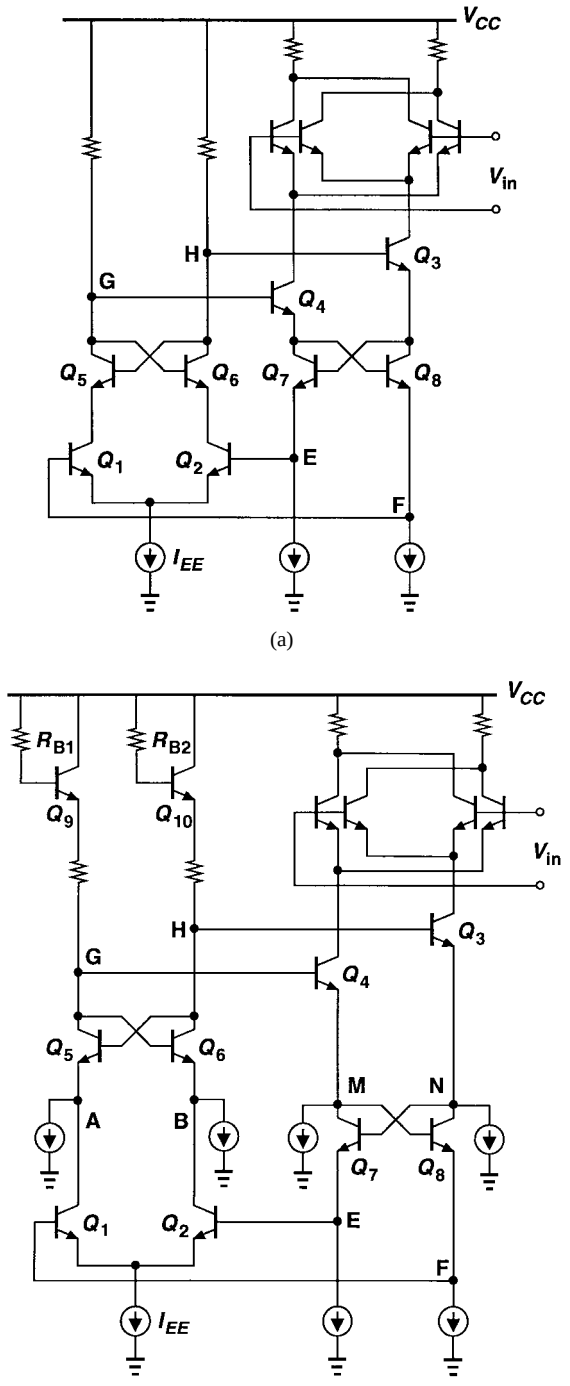
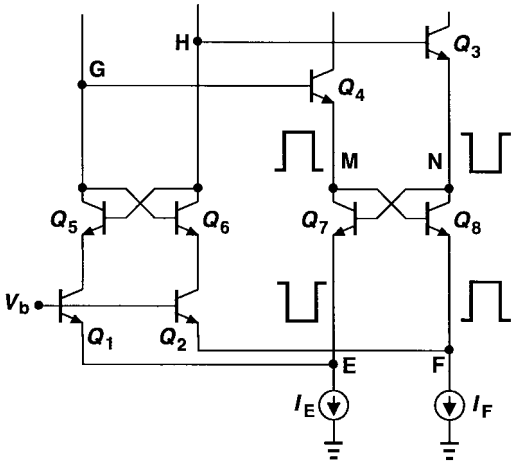


Fig. 7. (a) Addition of mixer to oscillator and (b) level shift, inductive peaking, and speed-up current sources.

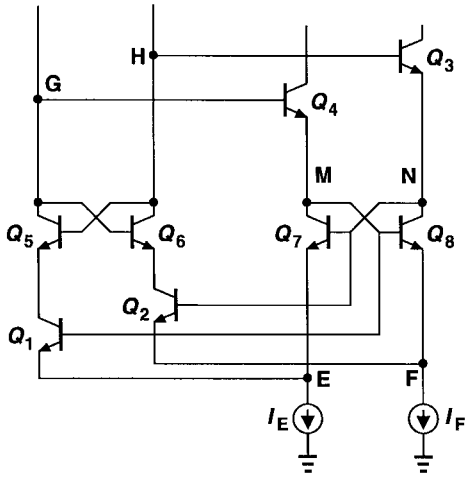
control voltage, exhibiting a tuning range of approximately 350 MHz.

The low-pass filter is simply a lead-lag network placed at the output of the mixer. The filtered signal is applied to A_1—a differential pair with level shift emitter followers—and the result controls the VCO frequency.

The low current levels and relatively high impedances in the VCO core make the frequency and amplitude of oscillation sensitive to the loading imposed by the output buffer. The signal is nonintrusively sensed by converting the collector



(a)



(b)

Fig. 8. (a) Coupling of feedback signals to emitters of Q_1 and Q_2 and (b) elimination of V_b.

currents of Q_9 and Q_{10} to voltage and applying the result to the output stage. This technique minimizes the effect of loading with no power penalty.

Fig. 11 shows the simulated capture behavior of the phase-locked loop. Plotted here is the VCO control voltage as a function of time for input frequencies of 1.9 GHz and 2 GHz. The lock time increases to roughly 100 ns as the input approaches the edge of the capture range.

In frequency synthesis applications, the input to the PLL is derived from a crystal oscillator and hence has a low phase noise. In order to suppress the VCO phase noise, the loop bandwidth is chosen to be approximately equal to 200 MHz so that random variations in the output period are corrected by the feedback. A possible application is in a heterodyne receiver where the first local oscillator has a fixed frequency and the second local oscillator performs the channel selection [6]. In practice, a frequency divider is inserted in the loop and the bandwidth may need to be reduced by roughly an order of magnitude. Nevertheless, as experimental results indicate, the noise skirts of the VCO flatten out well below an offset of 20 MHz. Also, the divider can be merged with the VCO circuit using similar techniques.

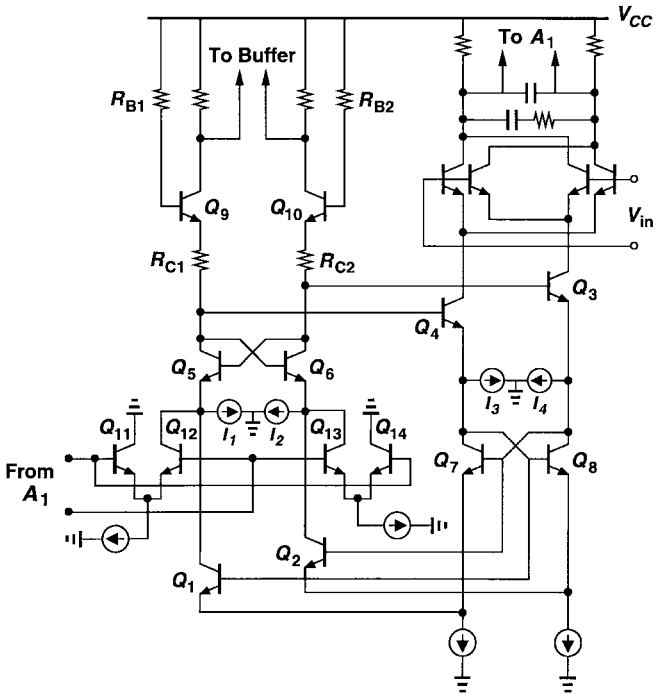


Fig. 9. VCO/mixer/LPF.

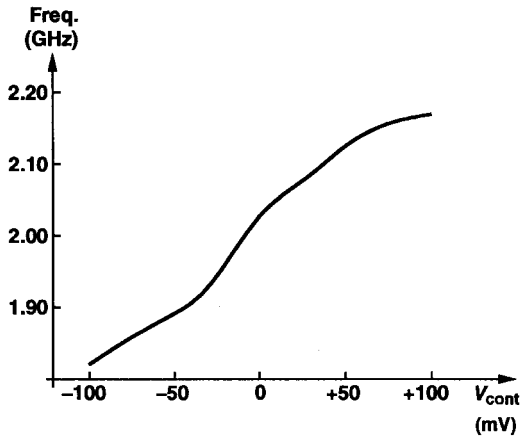


Fig. 10. VCO tuning characteristic.

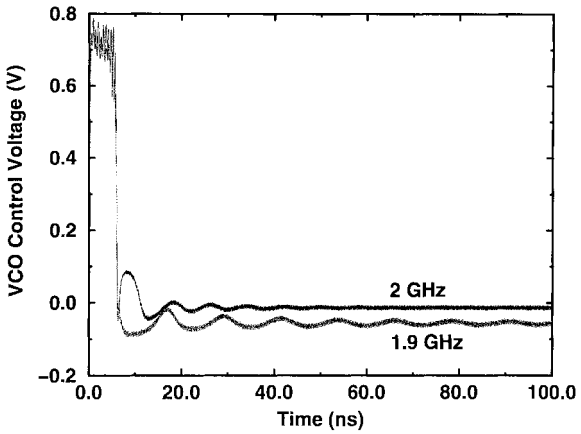


Fig. 11. Simulated capture behavior of PLL.

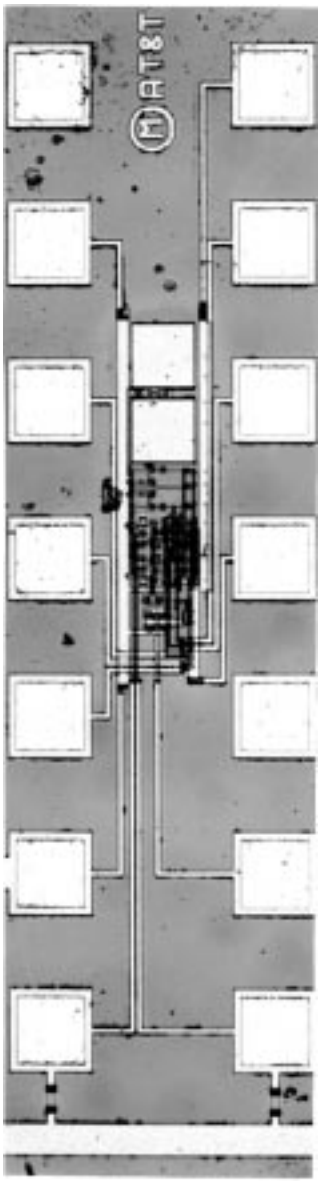


Fig. 12. PLL die photograph.

VI. Experimental Results

The PLL has been fabricated in an 18-GHz 0.6-μm BiCMOS technology. Shown in Fig. 12 is a photograph of the die, whose active area is approximately equal to 75 μm $\times$ 300 μm. The circuit has been tested on wafer using a high-speed Cascade probe station while running from a 3-V supply. The total supply current excluding that of the output buffer is 530 μA. Of this value, approximately 430 μA is drawn by the VCO/mixer combination and 100 μA by the low-frequency amplifier, A_1.

Fig. 13 shows the measured output in the time domain when the circuit is locked to a 2-GHz input. The bottom window displays one of the edges on a horizontal scale of 20 ps/div., revealing an rms jitter of 2.8 ps and a peak-to-peak jitter of 18 ps. The PLL achieves a capture range of 70 MHz and tracking range of 100 MHz. To increase these values, an additional frequency detection mechanism can be employed.

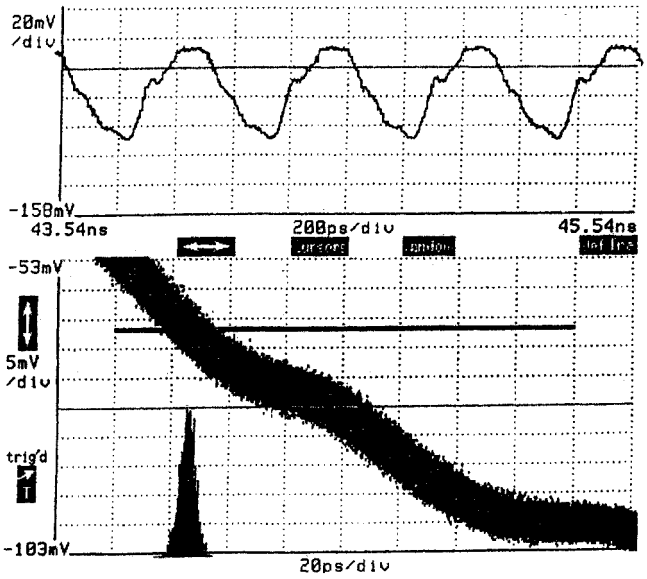


Fig. 13. Measures output in the time domain.

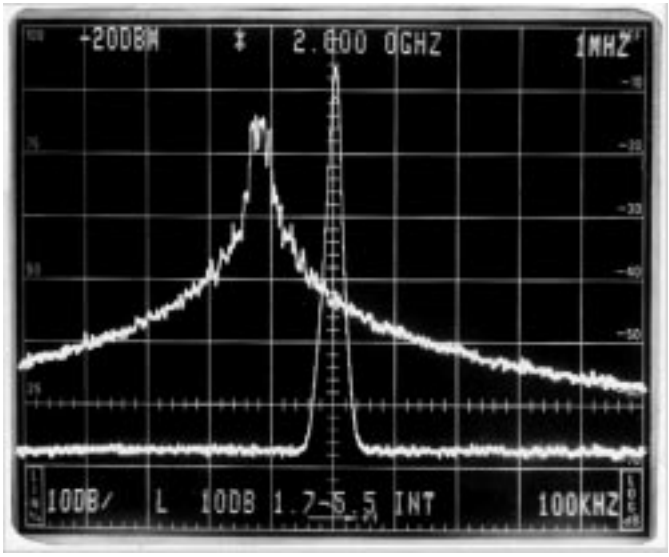


Fig. 14. Measured output in the frequency domain.

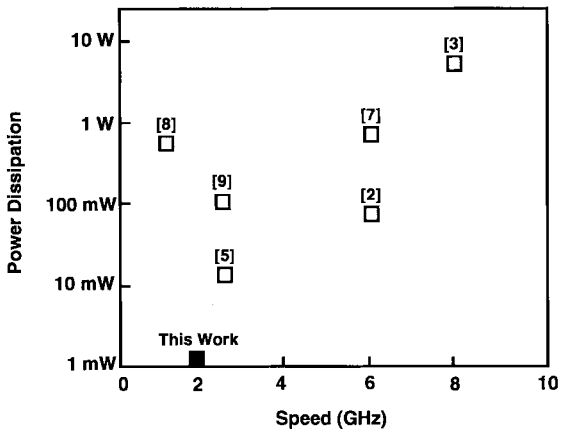


Fig. 15. Power–speed tradeoff in gigahertz PLL's and clock recovery circuits.

TABLE I
PERFORMANCE OF PLL

Center Frequency	2 GHz
Power Dissipation	1.6 mW
Tracking Range	100 MHz
Capture Range	70 MHz
Jitter	2.8 ps, rms
Phase Noise	–110 dBc/Hz @ 400 kHz offset
Supply Voltage	3 V
Technology	0.6–μm 18–GHz BiCMOS

The performance has also been examined in the frequency domain. Fig. 14 depicts the measured output with a resolution bandwidth of 100 kHz. The spectrum to the left corresponds to the free-running VCO, exhibiting substantial phase noise (approximately −75 dBc/Hz at 1 MHz offset). The spectrum to the right is obtained when the loop is locked, with the phase noise dropping to −110 dBc/Hz at 400 kHz offset.

Table I summarizes the performance of the PLL.

Fig. 15 illustrates the power–speed tradeoff for a number of gigahertz PLL's and clock recovery circuits. It is interesting to note that for a range of four to one in the speed, the power dissipation varies by more than three orders of magnitude.

VII. CONCLUSION

High-speed PLL's can be implemented as compact, low-power circuits through the use of techniques such as cross-coupled delay elements, inductive peaking, and minimum-length ring oscillators. An experimental prototype incorporating these techniques achieves a center frequency of 2 GHz while dissipating 1.6 mW from a 3-V supply. The oscillator jitter in the locked condition is reduced to an rms value of 2.8 ps by choosing a loop bandwidth of approximately 200 MHz.

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