

# From Red to Gold

*The rise of IEEE Journal of Solid-State Circuits  
to a high-impact journal*



**IEEE Journal of Solid-State Circuits**

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**T**he first issue of *IEEE Journal of Solid-State Circuits (JSSC)*, called the “red rag” by some old timers, was published when I was five years old. Today’s *JSSC* readers would have been roughly –30 to +30 years old at the time. The journal is not among the oldest publications in the IEEE or worldwide, but it enjoys one of the highest impact factors. Why? In this article, I ponder this question and demonstrate the longevity of the *JSSC*

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papers through some examples. In the interest of space, I have selected papers only from the first ten years, focusing on ideas that are still applicable today.

### Attributes of *JSSC* Papers

The papers published in *JSSC* generally have some attributes in common that make it a rich source of knowledge for IC designers. The journal’s review process—carried out by diverse generations of engineers and academicians over five decades—has consistently upheld certain criteria in judging the quality of the submitted papers, thus defining a uniquely high

bar for publication. My conjecture is that these criteria were, deliberately or not, inherited from the International Solid-State Circuits Conference paper selection standards. I have been reading the journal for more than 30 years and served two terms as an associate editor; I will share my view of its quality assurance mechanisms.

### Solving Real Problems

An important aspect of *JSSC* papers is that they address real problems, not “invented” ones. They push for speed if it is a bottleneck, for power consumption if it is significant. This perspective is naturally held by industry papers,

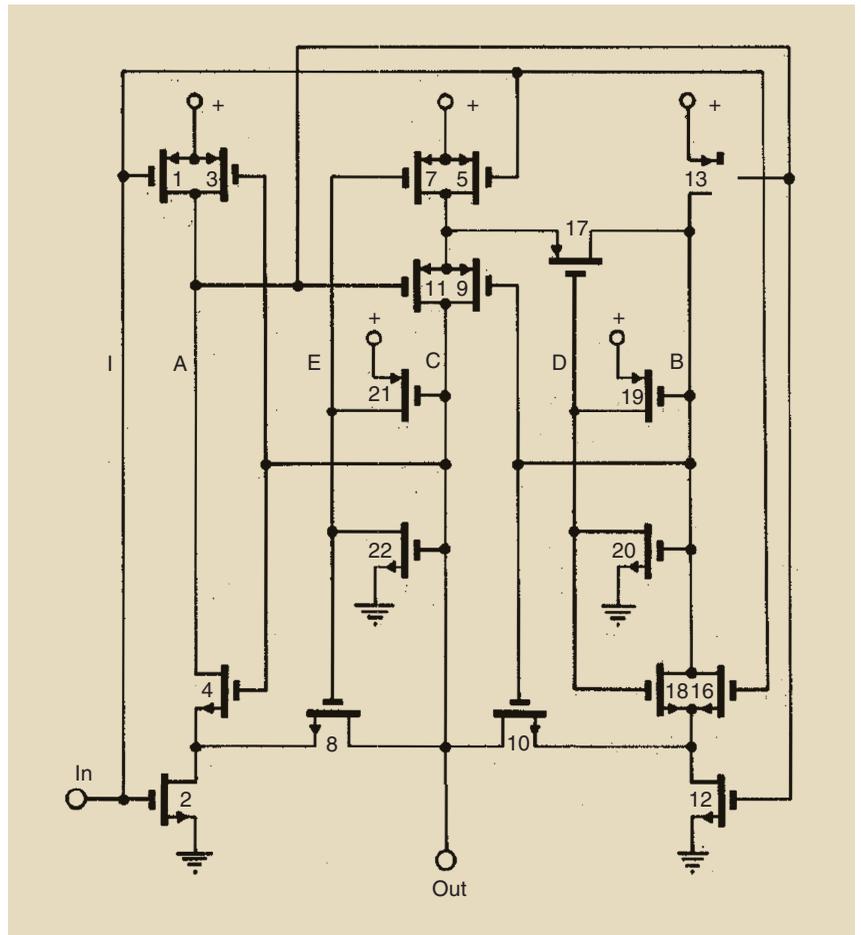
but it has also been present in university work. The term “real” does not necessarily mean imminent. If founded in great vision, research can deal with problems that would become real in the future.

Consider, for example, the 1972 paper “Silicon-Gate CMOS Frequency Divider for the Electronic Wrist Watch,” by Vittoz et al. [1]. The problem was real—after all, the authors worked at Centre Electronique Horloger (Center for Electronic Watch Making)—but their work also had a far-reaching impact. At the time, the industry was struggling with the question of noncomplementary metal–oxide–semiconductor (MOS) processes (which cost less but drew static power) versus complementary (CMOS) technology (which required more masks but had nearly zero static power consumption). Shown in Figure 1, the frequency divider stage was among the first to exploit the capabilities of complementary devices. The three-stage implementation in [1] consumed 1.6 nW/kHz in 5- $\mu\text{m}$  technology. It is remarkable that today’s counterparts in 40-nm processes are only about one order of magnitude better.

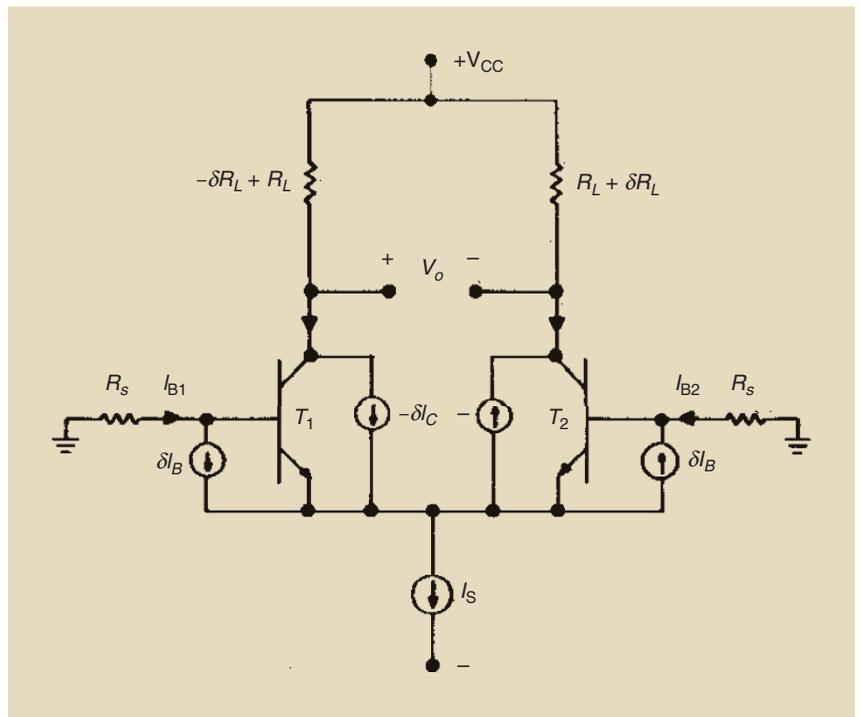
**Novelty**

The emphasis on novelty has been a solid pillar of JSSC’s paper review process. That is, the papers solve a real problem through the use of new methods—and justifiably. This facet has constantly pushed the designers to develop new topologies, new analyses, and new insights.

An example of new insights is Jaeger’s 1976 paper, “Unifying the Concepts of Offset Voltage and Common-Mode Rejection Ratio” [2]. Using the differential pair shown in Figure 2, Jaeger articulates how the variation of the input offset voltage with the input common-mode (CM) level translates to finite CM rejection and provides a simple, yet versatile, relationship. (In general, we can say  $\text{CMRR} = \partial V_{OS} / \partial V_{CM}$ , where  $V_{OS}$  denotes the input-referred offset.) This insight proves particularly valuable in today’s nanometer circuits, which suffer from large mismatches. The idea



**FIGURE 1:** The CMOS frequency divider reported by Vittoz et al. in 1972 (from [1]).



**FIGURE 2:** The differential pair used by Jaeger to relate offset and CMRR (from [2]).

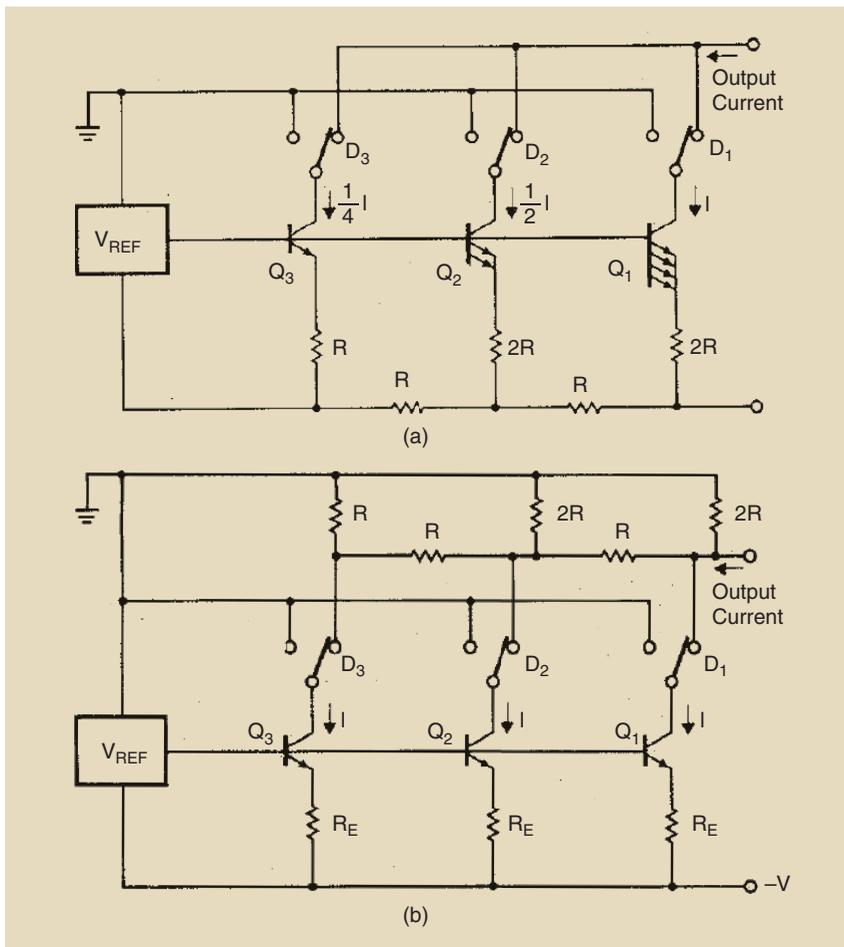


FIGURE 3: Current-steering DACs studied by Kelson et al. (from [3]).

can be readily extended to the power supply rejection ratio as well.

### Simple Is Beautiful

Most of the techniques that have survived these past five decades are simple and elegant. Despite migration from bipolar technology to CMOS processes and continual device and supply scaling, some topologies have remained attractive and applicable.

Figure 3 illustrates, as an example, Kelson's 1973 study of R-2R ladders in current-steering digital-to-analog converters (DACs) [3]. In Figure 3(a), the ladder is connected to the emitters of the current sources, but it requires binary scaling of the transistor emitter areas. In Figure 3(b), on the other hand, the ladder is moved to the collector network, allowing nominally identical unit current sources. The complexity of the circuit is thus reduced dramatically.

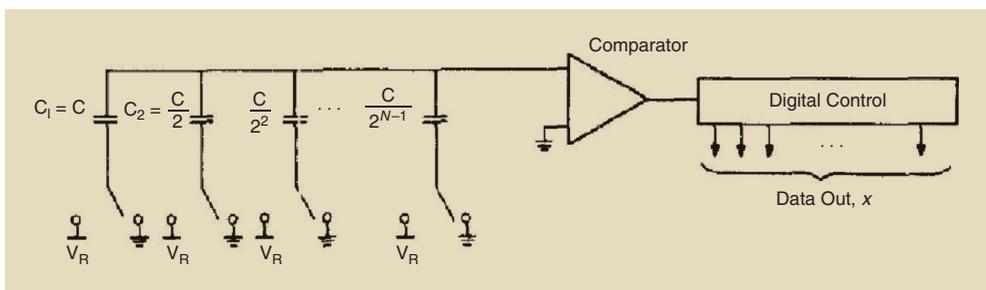


FIGURE 4: The charge redistribution SAR ADC proposed by McCreary et al. (from [4]).

Indeed, the latter approach is common today in MOS current-steering realizations as well. Moreover, the idea has been extended to C-2C networks in capacitor DACs.

Another example of simple, yet long-lasting, ideas is the notion of charge redistribution and its use in analog-to-digital converters (ADCs) [4], [5]. Shown in Figure 4 is a successive approximation (SAR) ADC incorporating this idea [4]. The circuit consists of a binary-weighted capacitor array operating as a DAC, a comparator, and SAR logic. The analog input is sampled on the bottom plates of the capacitors while the top plates are grounded. Next, over a succession of cycles, the bottom plates are switched to zero or  $V_R$  (causing "charge redistribution"), and the comparator determines the sign of the resulting voltage at its input. With the aid of the logic and by virtue of the high loop gain, the bottom-plate switching drives, over some clock cycles, the comparator input voltage toward zero. The digital input of the DAC therefore approaches a precise representation of the analog input.

The charge redistribution concept was distinctly different from previous SAR designs in two respects: 1) it merged the front-end sampler with the DAC, obviating the need for an explicit sample-and-hold circuit, and 2) it replaced the power-hungry current-steering DACs with a capacitor array. The impact of this approach has been greatly felt in the resurrection of SAR ADCs in the past ten years.

### "Silicon" Requirement

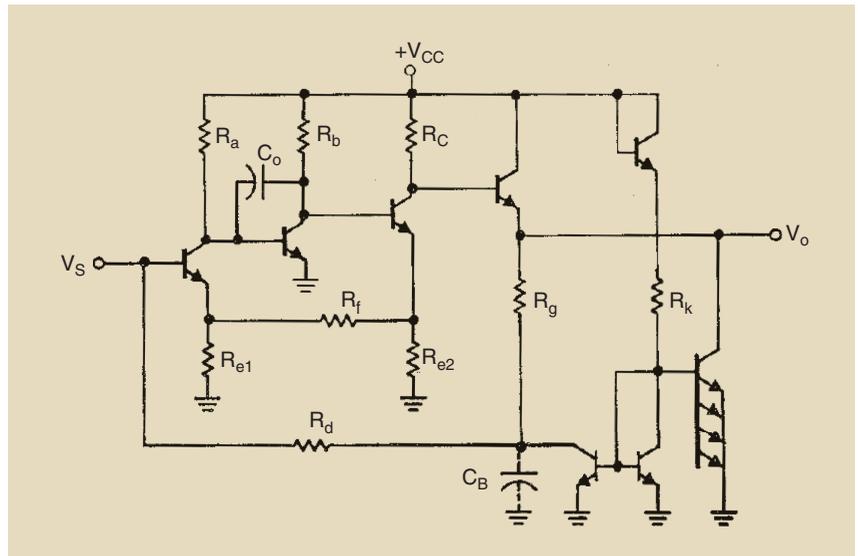
Unlike most other IEEE or non-IEEE publications, JSSC has generally required experimental results that support the concepts introduced in the submitted papers. It is interesting to look back and see how this (unwritten) rule has shaped the journal. An innovative idea should be tested in a realistic environment, with the imperfections that the designer will face present. It is the

lengthy process of design, layout, and testing that reveals the issues that may not manifest themselves in simulations. In other words, when the efficacy of a proposed concept is demonstrated by experimental verification, the reader is more convinced that the solution is robust and the results are reproducible.

The experimental component in *JSSC* papers also demands that the authors have a deep understanding of device physics, process technology, layout extraction and verification, and high-performance testing—all valuable skills for anyone working in IC industry. Indeed, these aspects of *JSSC* papers have prepared engineers very well for increasingly more complex technologies over the past five decades.

### Other Examples from the First Ten Years

From its first issue, *JSSC* has presented fundamental ideas that continue to serve us today. In their September 1966 paper, “A Highly Desensitized Wide-Band Monolithic Amplifier” [6], Solomon and Wilson introduce the feedback circuit shown in Figure 5, describing two remarkable aspects, namely, the use of Miller compensation capacitor  $C_p$ , and the pole splitting that results from this type of frequency compensation. Half a century later, we continue to exploit these properties in our designs.



**FIGURE 5:** A wideband amplifier incorporating Miller compensation and pole splitting reported by Solomon and Wilson (from [6]).

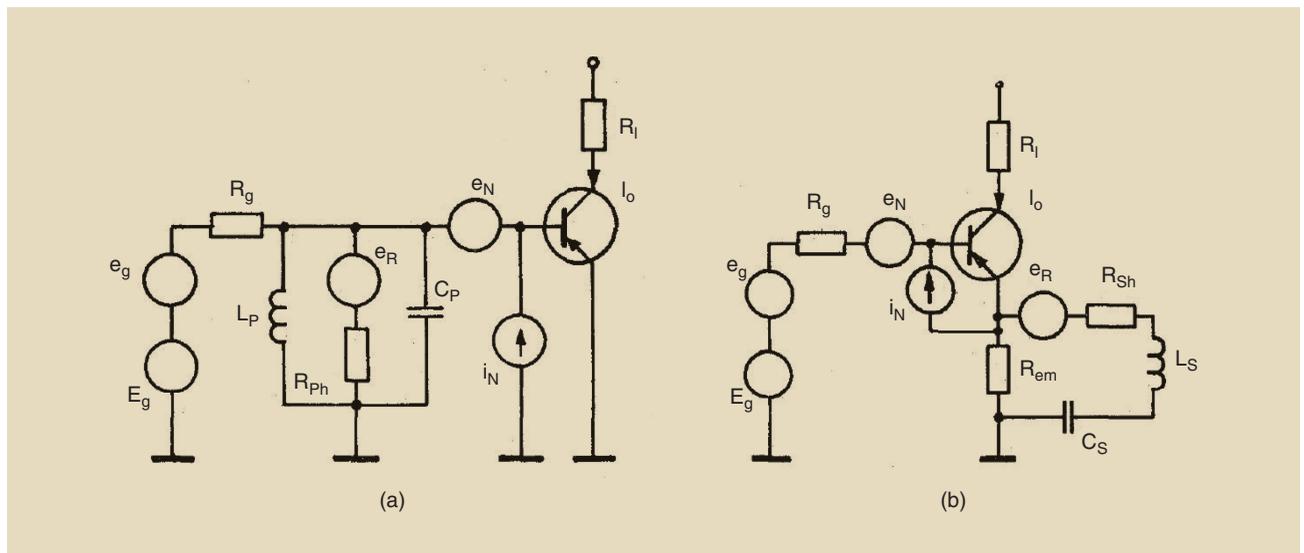
In his 1967 paper, Suominen analyzes the two amplifier topologies shown in Figure 6 and makes the important observation that inductive degeneration (“series tuning”) of a common-emitter stage leads to a lower noise figure than does a tank in parallel with the input (“parallel tuning”) [7]. Present inductively degenerated low-noise amplifiers benefit from this property.

While not directly related to mainstream circuit design, the 1969 paper, “A Fully Integrated Timing Generator for the PICTUREPHONE Video-Telephone Camera,” by Davis et al. [8] exemplifies

long-term vision. Shown in Figure 7 is the PICTUREPHONE station developed by Bell Telephone Laboratories and used by 40 employees of Westinghouse for video communication. The grand idea was well ahead of its time, but the authors wrote “In an effort to minimize volume, heat dissipation, and cost,” many of the circuits were realized in integrated form—the same tenet pursued by today’s semiconductor industry.

### The Next 50 Years

One wonders whether, in 1966, anyone could have predicted the



**FIGURE 6:** Low-noise amplifiers using (a) parallel and (b) series resonance (from [7]).



**FIGURE 7:** The PICTUREPHONE, a video communication device developed at Bell Labs (from [8]).

astounding developments that the semiconductor industry would witness in the following half century. By the same token, our vision today of what will happen in the next 50 years may heavily underestimate human ingenuity. Nevertheless, we can look into the crystal ball and make some predictions.

While computing and communications—and their convergence—have formed the driving force thus far, it is likely that future developments will be dictated by applications. From land and air vehicles to robotics and health care, one can imagine myriad roles for the semiconductor industry. The following are some ideas that come to mind.

### A Swarm of Cars

The notion of self-driving cars becomes more attractive if the vehicles on the road coordinate their movements among themselves. The automated nature of such a large network of vehicles can avoid human-induced delays and accidents while providing optimum routes for each user. Furthermore, if coordinated like a swarm of bees, the cars on the road need not belong to anyone: we hop from one car to another so as to reach our destination in the shortest time.

The principal enablers of such “networked cars” include wireless communications, radar technology, and global positioning systems. If the vehicles themselves act as nodes in a distributed system, then communication can occur based on node hopping, thereby allowing simple, low-cost standards to be used.

### Is There a Doctor in the Air?

It is conceivable that, sometime in the future, our cities will be covered by a network of drones. Occasionally visiting charging stations available on, for example, cell phone towers or tall buildings, the drones will serve as a powerful, highly coordinated distributed system. According to today’s plans, the drones will deliver goods and possibly the mail. But they will also be able to act in medical emergencies, reaching people much faster than land vehicles (think uber drones). Now imagine that, upon landing in such a situation, a drone reconfigures itself into a robot and performs basic procedures on the person in need, under the supervision of a remote doctor, before emergency help arrives. Or perhaps several drones can quickly form a small helicopter and transport the patient. As outlandish as it may sound, this convergence of drone technology, robotics, wireless communications, and bioengineering already has most of its components in place. One can extend the idea of “robotdrones” to other fields as well.

### Look, Ma! No Fingers!

The interface between humans and computers has been studied for decades, but we still type our messages in one form or another. What if our brains directly interfaced with machines? Brain-wave decoding has made significant progress in the past ten years. For example, Neurosky’s Orbit Mobile is a US\$200 model helicopter that can be flown under the command of brain waves. An electroencephalogram headset picks up the user’s neural activity and wirelessly

communicates with the vehicle. It is plausible that, over the next decade or so, our brain-wave recognition algorithms advance enough to yield an acceptable error rate for interfacing with machines. Of course, walking around with a probe attached to your head may look geeky, but is it really geekier than wearing earphones?

### References

- [1] E. Vittoz, B. Gerber, and F. Leuenberger, “Silicon-gate CMOS frequency divider for the electronic wrist watch,” *IEEE J. Solid-State Circuits*, vol. 7, pp. 100–104, Apr. 1972.
- [2] R. C. Jaeger, “Unifying the concepts of offset voltage and common-mode rejection ratio,” *IEEE J. Solid-State Circuits*, vol. 11, pp. 557–561, Aug. 1976.
- [3] G. Kelson, H. Stelrecht, and D. Perloff, “A monolithic 10-b digital-to-analog converter using ion implantation,” *IEEE J. Solid-State Circuits*, vol. 8, pp. 396–403, Dec. 1973.
- [4] J. L. McCreary and P. R. Gray, “All-MOS charge redistribution analog-to-digital conversion techniques—Part I,” *IEEE J. Solid-State Circuits*, vol. 10, pp. 371–379, Dec. 1975.
- [5] R. E. Suarez, P. R. Gray, and D. A. Hodges, “All-MOS charge redistribution analog-to-digital conversion techniques—Part II,” *IEEE J. Solid-State Circuits*, vol. 10, pp. 379–385, Dec. 1975.
- [6] J. E. Solomon and G. R. Wilson, “A highly desensitized wideband monolithic amplifier,” *IEEE J. Solid-State Circuits*, vol. 1, pp. 19–28, Sept. 1966.
- [7] O. Suominen, “Series-tuned amplifier, a low noise preamplifier,” *IEEE J. Solid-State Circuits*, vol. 2, pp. 116–118, Sept. 1967.
- [8] P. Davis, K. Gardner, and A. Gordon, “A fully integrated timing generator for the PICTUREPHONE video-telephone camera,” *IEEE J. Solid-State Circuits*, vol. 5, pp. 250–254, Oct. 1969.

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