Jitter-Power Trade-Offs in PLLs

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(Invited Paper)

***Abstract*— As new applications impose jitter values in the range of a few tens of femtoseconds, the design of phase-locked loops faces daunting challenges. This paper derives basic relations between the tolerable jitter and the power consumption, predicting severe issues as jitters below 10 fs are sought. The results are also applied to the sampling clocks in analog-to-digital converters and suggest that clock generation may consume a greater power than the converter itself.**

***Index Terms*— Oscillators, phase noise, crystal oscillators, integrated jitter, data converters.**

I. Introduction

THE problem of phase-locked loop (PLL) jitter manifests itself in various systems, particularly in communications and in data converters. Several trends have led to the recent demand for low jitter. First, higher data rates tighten the timing budget for most of the stages in a link. Second, the limited available bandwidth in both wireline and wireless media necessitates spectrally efficient modulation schemes, which further constrain the tolerable jitter in clock and local oscillator (LO) generation. Third, as analog-to-digital converters (ADCs) target higher speeds and resolutions, their sampling clock jitter must commensurately fall. State-of-the-art PLL design has achieved jitter values in the range of 50 to 75 fs_{rms} at frequencies from 5.5 GHz to 16 GHz [1]–[6].

The phenomenon of jitter in PLLs has been investigated in prior work [7]–[10]. The objective of this paper is to formulate the trade-offs between the PLL jitter and power consumption and predict the design issues as the former is reduced to sub-10-fs values. Extending the work in [11], we derive trends that suggest formidable challenges lie ahead.

Section II provides an overview of today's desirable jitter values, and Section III presents the framework for our analysis. Section IV deals with the effect of oscillator phase noise, and Section V takes into account the reference contribution as well. Section VI concerns the charge pump (CP) noise. Sections VII and VIII respectively analyze the effect of jitter on ADCs and factors that can mitigate jitter-power trade-offs.

II. The Need for Low Jitter

Wireline transceivers have steadily pushed for greater speeds, reaching rates as high as 112 Gb/s through the use of PAM4 signaling [12]–[14]. It is expected that the next generation will rise to 224 Gb/s [15]. If a symbol rate of 112 Gbaud is assumed, the symbol period is about 9 ps, requiring that the transmit (TX) PLL exhibit a jitter less than roughly 100 fs_{rms}.[1] But the situation is far more severe in the receive (RX) path. Typical PAM4 systems employ a 7-bit ADC to digitize the received signal [12], [13], calling for a jitter less than 10 fs (Section VIII-A) at a clock rate of 112 GHz.

Wireless transceivers, too, face the need for low jitters. For example, the use of 256QAM in 5G radios operating around 30 GHz introduces new challenges. As shown in [16], this modulation scheme necessitates an integrated phase jitter of -45 dB, which translates to $10^{-45/20}$ rad and hence 30 fs at 30 GHz. Thus, the TX and the RX frequency synthesizers must provide less than 21 fs of jitter.

High-speed, high-resolution ADCs also present tough PLL design issues. A 12-bit 10-GHz ADC can tolerate less than 10 fs of jitter (Section VIII-A). We thus observe the need for PLLs operating at various frequencies and achieving jitter values below a few tens of femtoseconds.

III. Analysis Framework

As a "best-case" scenario, we consider a simple integer-N PLL that delivers an output frequency of f_{CK} while employing a reference crystal oscillator running at $f_{REF} = f_{CK}/N$ [Fig. 1(a)]. In order to derive upper bounds for the performance, we neglect three noise components: (1) the flicker noise in all of the building blocks, (2) the phase noise of the phase/frequency detector (PFD), and (3) the phase noise of the frequency divider(s). Moreover, we consider only the voltage-controlled oscillator (VCO) power consumption.

We first include only the VCO phase noise, then that of the reference, and finally the charge pump contribution. In the absence of flicker noise, the VCO phase noise is of the form

$$S(f) = \frac{\alpha}{f^2}, \tag{1}$$

where α is a constant related to the oscillator topology and design, and f is the offset frequency.

As explained in Section V-A, the PLL bandwidth must be drastically reduced when the reference and CP noise is taken into account. In such a case, the PLL can be approximated by a first-order system. We represent the input-output transfer function in Fig. 1(a) by

$$\frac{\phi_{out}}{\phi_{in}} \approx \frac{N}{1+\frac{s}{\omega_1}}, \tag{2}$$

Manuscript received December 21, 2020; revised January 24, 2021; accepted February 2, 2021. Date of publication February 15, 2021; date of current version March 8, 2021. This work was supported by Realtek Semiconductor. This article was recommended by Associate Editor J. Zhao.

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/TCSI.2021.3057580.

Digital Object Identifier 10.1109/TCSI.2021.3057580

[1] For Gaussian jitter, this yields a peak-to-peak value of roughly 0.8 ps_{rms}.

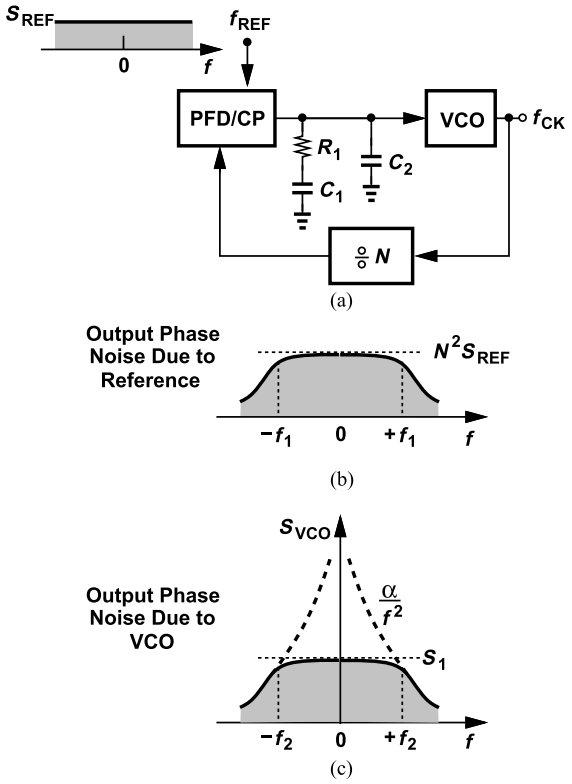


Fig. 1. (a) Basic PLL architecture, (b) output phase noise profile due to reference, and (c) output phase noise profile due to VCO.

where $\omega_1 = 2\pi f_1 \approx I_p K_{VCO} R_1/(2\pi N)$, I_p is the CP current, and K_{VCO} the VCO gain. For example, the reference phase noise is shaped by $|\phi_{out}/\phi_{in}|^2$ [Fig. 1(b)].

The phase noise and operation frequency of crystal oscillators can be selected based on the available values. The designs in [27]–[29] provide a phase noise in the range of -153 to -158 dBc/Hz at 100-kHz offset for operation frequencies from 40 MHz to 54 MHz while drawing less than 0.2 mW. On the other hand, Vectron's OX-305 100-MHz crystal oscillator exhibits a phase noise of -178 dBc/Hz but draws 1.8 W [30]. As an optimistic choice, we assume $f_{REF} = 100$ MHz and a flat profile given by $S_{REF} = -170$ dBc/Hz.

Similarly, as depicted in Fig. 1(c), we approximate the output phase noise due to the VCO by a plateau up to f_2 and an α/f^2 roll-off beyond. Here, S_1 denotes the free-running VCO phase noise at an offset frequency of f_2. Since the narrow loop bandwidth translates to a large damping factor, we have $f_2 \approx f_1$.

IV. Effect of VCO Phase Noise

The total random jitter contributed by the VCO is given by the area under S_{VCO} in Fig. 1(c). The area from $-f_2$ to $+f_2$ is equal to $2S_1 f_2$. Moreover, for a free-running phase noise profile of the form α/f^2, the areas under the tails also add up to $2S_1 f_2$. To express the total area, $4S_1 f_2$, in seconds squared, we multiply it by $T_{CK}^2/(4\pi^2)$, where $T_{CK} = 1/f_{CK}$, obtaining the integrated jitter as:

$$\sigma_j^2 = 4S_1 f_2 \left(\frac{T_{CK}}{2\pi}\right)^2. \tag{3}$$

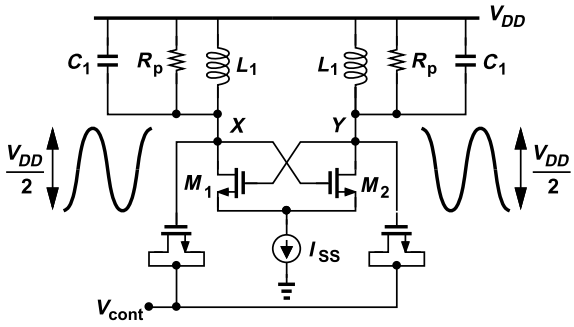


Fig. 2. Simple LC VCO.

We must next compute S_1. Let us consider the simple LC VCO topology shown in Fig. 2, where the circuit oscillates at a frequency of f_{CK} and R_p models the loss of the tanks. Neglecting the noise of I_{SS} and the flicker noise of M_1 and M_2, we write the free-running phase noise from [24] as:

$$S(f) = \frac{\pi^2 kT(1+\gamma)}{2R_p I_{SS}^2}\left(\frac{f_{CK}}{2Qf}\right)^2, \tag{4}$$

where γ denotes the MOS excess noise coefficient (assumed equal to unity here) and f is the offset frequency. We assume that the single-ended peak-to-peak voltage swing, $(4/\pi)I_{SS}R_p$, is approximately equal to $V_{DD}/2$. Denoting the VCO power consumption, $I_{SS}V_{DD}$, by P_{VCO}, we have

$$S(f) = \frac{4\pi kT(1+\gamma)}{P_{VCO}}\left(\frac{f_{CK}}{2Qf}\right)^2. \tag{5}$$

We should remark that (5) gives an oscillator figure of merit (FOM) of:

$$\text{FOM} = 10\log\frac{f_{CK}^2}{f^2 S(f)(10^3 P_{VCO})} \tag{6}$$

$$= 10\log\frac{Q^2}{10^3\pi kT(1+\gamma)}, \tag{7}$$

where the factor of 10^3 is introduced so as to express the power in milliwatts. For example, $Q = 10$ leads to FOM ≈ 186 dB at $T = 300$ K. We return to this point in Section IX. Noting that $S(f_2)$ in (5) yields S_1 in Fig. 1(c), we replace for S_1 in (3):

$$\sigma_j^2 = \frac{kT(1+\gamma)}{\pi P_{VCO} Q^2}\cdot\frac{1}{f_2}. \tag{8}$$

The jitter-power trade-off thus emerges as

$$P_{VCO} = \frac{kT(1+\gamma)}{\pi Q^2 f_2}\frac{1}{\sigma_j^2}. \tag{9}$$

This result merits three remarks. First, $P_{VCO} \propto \sigma_j^{-2}$; e.g., to halve σ_j, P_{VCO} must quadruple. Second, the trade-off is relatively independent of the output frequency. For example, if $f_2 = 0.1 f_{REF} = 10$ MHz and $Q = 10$, we have $P_{VCO} = 26$ mW for $\sigma_j = 10$ fs$_{rms}$. Third, if the jitter is expressed in radians rather than in seconds, P_{VCO} becomes proportional to f_{CK}^2.

Figure 3 plots the necessary VCO power consumption versus σ_j for two cases, namely, $f_2 = 10$ MHz (lower plot) and 5 MHz. Note that P_{VCO} reaches several watts as $\sigma_j \to 1$

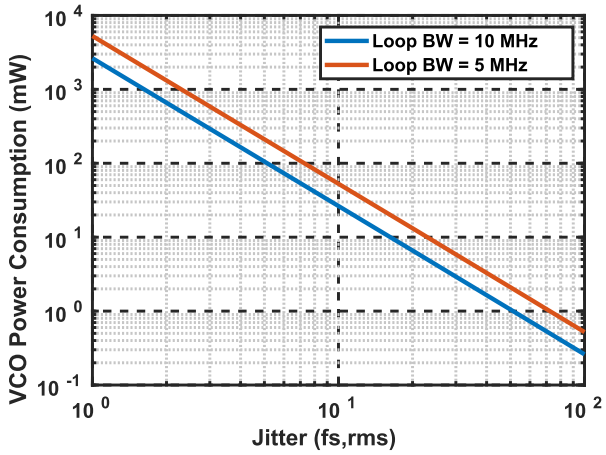


Fig. 3. Necessary VCO power consumption versus jitter for two PLL bandwidths.

fs. As seen in the next section, P_{VCO} climbs even more dramatically if the reference and CP noise is also taken into account.

V. Effect of Reference Phase Noise

A. Optimum Loop Bandwidth

The choice of $f_2 = 10$ MHz in the previous section appears somewhat arbitrary but well-suited to suppressing the VCO phase noise. On the other hand, in the presence of reference phase noise, the optimum PLL bandwidth may be lower.

We wish to minimize the sum of the phase noise spectra in Figs. 1(b) and 1(c). From (2), we write the output contribution of the reference as

$$S_{out,REF}(f) = \frac{N^2 S_{REF}}{1 + \frac{f^2}{f_1^2}}. \tag{10}$$

The area under this curve is equal to $\pi N^2 S_{REF} f_1$. We must minimize

$$S_{tot} = 4S_1 f_2 + \pi N^2 S_{REF} f_1. \tag{11}$$

In Fig. 1(c), $S_1 = \alpha / f_2^2$, yielding $4S_1 f_2 = 4\alpha / f_2$. If $f_1 \approx f_2$,

$$S_{tot} \approx 4\frac{\alpha}{f_2} + \pi N^2 S_{REF} f_2. \tag{12}$$

The optimum loop bandwidth is then equal to

$$f_2 = \sqrt{\frac{4\alpha}{\pi N^2 S_{REF}}}. \tag{13}$$

This choice leads to equal VCO and reference contributions. We now express the minimum S_{tot} as

$$S_{min} = 4\sqrt{\alpha \pi N^2 S_{REF}}. \tag{14}$$

The optimum loop bandwidth can be expressed in another useful form if the tolerable jitter, σ_j^2, is known. Since half of this amount stems from the reference, we have

$$\pi N^2 S_{REF} f_1 \cdot \left(\frac{T_{CK}}{2\pi}\right)^2 \approx \frac{\sigma_j^2}{2}. \tag{15}$$

That is,

$$f_1 = \frac{2\pi \sigma_j^2 f_{REF}^2}{S_{REF}}. \tag{16}$$

B. The Case of High Tolerable Jitter

In typical PLL designs, the loop bandwidth is less than $f_{REF}/10$. Thus, the result in (16) is valid only if it does not exceed this value, i.e., if σ_j is not very large. Suppose that the PLL jitter in a less demanding application translates to $f_1 > f_{REF}/10$. We assume $f_1 \approx f_2 \approx f_{REF}/10$ and express the reference jitter contribution as

$$\sigma_{j,REF}^2 = \pi N^2 S_{REF} f_1 \left(\frac{T_{CK}}{2\pi}\right)^2 \tag{17}$$

$$\approx \frac{0.1 S_{REF}}{4\pi f_{REF}}. \tag{18}$$

We then find the allowable VCO contribution as $\sigma_j^2 - \sigma_{j,REF}^2$ and use this value in lieu of σ_j in (9) to obtain P_{VCO}:

$$P_{VCO} = \frac{kT(1+\gamma)}{\pi Q^2 f_2} \frac{1}{\sigma_j^2 - \sigma_{j,REF}^2}. \tag{19}$$

C. Jitter-Power Trade-Off

Equation (14) provides the total jitter in terms of the oscillator's α factor. For the VCO topology of Fig. 2, we obtain α from (5),

$$\alpha = \frac{\pi kT(1+\gamma) f_{CK}^2}{P_{VCO} Q^2}, \tag{20}$$

and hence

$$S_{min} = 4\sqrt{\frac{\pi^2 kT(1+\gamma)}{P_{VCO} Q^2} N^2 f_{CK}^2 S_{REF}}. \tag{21}$$

Multiplying this result by $T_{CK}^2/(4\pi^2)$ yields the squared jitter:

$$\sigma_j^2 = \sqrt{\frac{kT(1+\gamma)}{P_{VCO}} S_{REF}} \frac{NT_{CK}}{\pi Q} \tag{22}$$

$$= \sqrt{\frac{kT(1+\gamma)}{P_{VCO}} S_{REF}} \frac{1}{\pi Q f_{REF}}. \tag{23}$$

It follows that

$$P_{VCO} = \frac{kT(1+\gamma) S_{REF}}{\pi^2 Q^2 f_{REF}^2} \frac{1}{\sigma_j^4}. \tag{24}$$

We should remark that this result applies to subsampling PLLs as well.

The jitter-power trade-off expressed by (24) reveals several important points. First, $P_{VCO} \propto \sigma_j^{-4}$, a sharp point of contrast to the behavior in (9). Thus, in the presence of reference phase noise, P_{VCO} must rise by a factor of 16 for every halving of σ_j. Second, P_{VCO} can be reduced by selecting a higher f_{REF}, but only if the corresponding S_{REF} does not increase proportionally. Third, P_{VCO} is relatively independent of the output frequency.

As an example, let us target $\sigma_j = 10$ fs_{rms} with $Q = 10$, $f_{REF} = 100$ MHz and $S_{REF} = -170$ dBc/Hz. Equation (24) gives $P_{VCO} \approx 840$ mW, about a factor of 32 higher than the value obtained in Section IV. We must ponder why this occurs. Recall from the optimization in Section V-A that half of the jitter power arises from the reference. That is, Eq. (16)

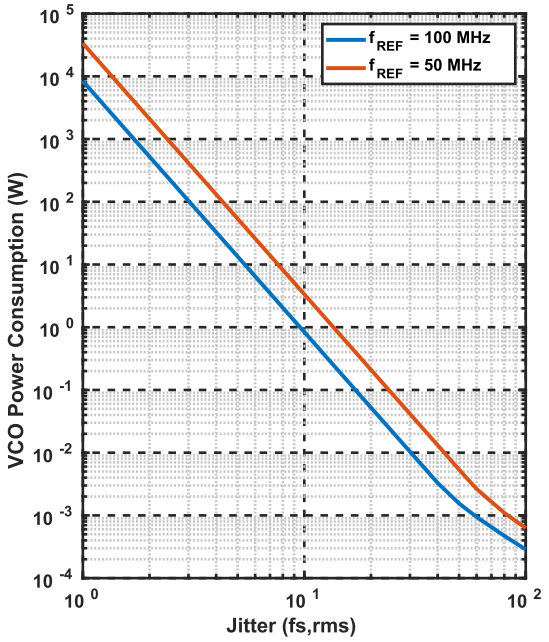


Fig. 4. Necessary VCO power consumption versus jitter for two reference frequencies.

indicates that $f_1 \approx f_2 = 630$ kHz. The loop bandwidth is thus reduced by a factor of 16, demanding a 16-fold increase in the VCO power consumption. Moreover, to accommodate the reference contribution, the VCO phase noise must drop by another factor of 2, leading to the 32-fold rise obtained above.

Figure 4 plots the required VCO power consumption with $S_{REF} = -170$ dBc/Hz and $f_{REF} = 100$ MHz (lower plot) or $f_{REF} = 50$ MHz. As explained in Section V-B, the loop bandwidth is restricted to $f_{REF}/10$ for the case of higher jitter values. The VCO power ascends to tens of thousands of watts for a jitter of 1 fs!

Equation (24) portrays a grim picture, thereby motivating us to explore LC VCOs with a greater FOM and also seek crystal oscillators with a more favorable S_{REF}/f_{REF}^2 value. We return to these points in Section IX.

VI. Effect of Charge Pump Noise

The noise, $\overline{I_n^2}$, injected by each current source in the charge pump onto the loop filter translates to phase noise at the PLL output [10]. Suppose the loop is locked and the CP up and down current sources turn on simultaneously for a finite time, T_{CP}, in every reference cycle, T_{REF}. This periodic switching of white noise still yields a white output noise current while scaling its spectral density by the duty cycle, T_{CP}/T_{REF}. The total equivalent noise current is thus given by $2\overline{I_n^2}T_{CP}/T_{REF}$, where the factor of 2 assumes equal noise spectral densities for the up and down current sources. Noting that the gain of the PFD/CP cascade is equal to $I_p/(2\pi)$ A/rad, we divide the resulting spectrum by the square of this gain so as to refer it to the PFD input:

$$S_{CP}(f) = 8\pi^2 \frac{T_{CP}}{T_{REF}} \frac{\overline{I_n^2}}{I_p^2}. \tag{25}$$

This phase noise is indistinguishable from that of the reference and can be included in our previous results if we simply replace S_{REF} with $S_{REF} + S_{CP}$. Equation (24) is therefore revised to

$$P_{VCO} = \frac{kT(1+\gamma)}{\pi^2 Q^2 f_{REF}^2}\left(S_{REF} + 8\pi^2 \frac{T_{CP}}{T_{REF}} \frac{\overline{I_n^2}}{I_p^2}\right)\frac{1}{\sigma_j^4}. \tag{26}$$

The CP noise proves quite serious even though the power consumption of the CP itself is negligible (as it is proportional to T_{CP}/T_{REF}). To appreciate this point, let us consider a simple case where the CP noise contribution in (25) is the same as that of the reference and equal to -170 dBc/Hz. For each CP current source, we have $\overline{I_n^2} = 4kT\gamma g_m = 4kT\gamma(2I_p)/|V_{GS} - V_{TH}|$; (25) thus emerges as

$$S_{CP}(f) = 64\pi^2 \frac{T_{CP}}{T_{REF}} \frac{kT\gamma}{|V_{GS} - V_{TH}|I_p}. \tag{27}$$

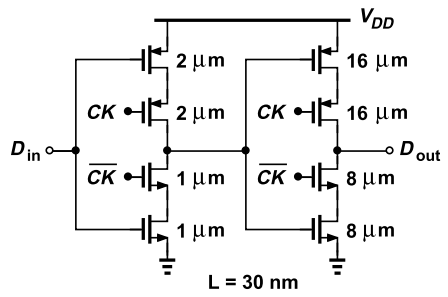
With a standard NOR-based PFD design, T_{CP} is roughly equal to 5 gate delays [17]. We then assume $T_{CP} \approx 50$ ps, $T_{REF} = 10$ ns, and $|V_{GS} - V_{TH}| = 100$ mV, obtaining $I_p = 13$ mA. (Simulations in 28-nm technology confirm that $T_{CP} \approx 50$ ps suffices to turn the charge pump transistors on and off.) We should remark that these results apply to single-ended charge pumps and should be revisited for differential topologies.

This example provides two critical insights. First, the necessary CP current reaches very high levels, exacerbating issues such as the ripple on the oscillator control voltage and the CP supply regulator output impedance. Second, as it relates to the focus of this paper, even with $I_p = 13$ mA, $S_{REF} + S_{CP}$ is twice as large as S_{REF}, requiring a twofold increase in P_{VCO}. That is, the 10-fs jitter target in Section V-C can only be met if $P_{VCO} \geq 1.68$ W. We recognize the enormous increase in P_{VCO}, from 26 mW in Section IV to 1.68 W, as we have taken into account the VCO, the reference, and the CP contributions.

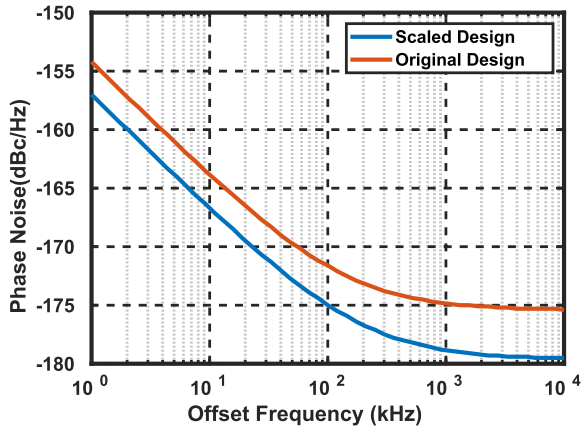
VII. A Note on Frequency Dividers

The analysis of phase noise in frequency dividers is beyond the scope of this paper, but we make three observations that help explain their role in our projections. First, the divider output phase noise experiences the low-pass rsponse of the PLL as it travels to the output and hence simply adds to the reference phase noise. We thus wish to ensure that the former is well below the latter. Second, the use of a retiming flipflop that is clocked by the VCO can remove the divider phase noise. For example, [18] reports a 27-mW 32/33 divider that operates up to 3 GHz and, by virtue of a retimer, achieves a phase noise of about -172 dBc/Hz for offsets greater than a few hundred kilohertz at an output frequency of 70 MHz.

Third, we simulate the retiming flipflop example shown in Fig. 5(a), assuming it senses a 100-MHz signal from the feedback divider in our PLL and retimes it by a 20-GHz clock. The circuit draws a total of 0.6 mW from a 1-V supply, most of which is consumed in the clock path. The output phase noise is plotted in Fig. 5(b) (denoted as the "original design"; higher plot). Given that the PLL bandwidth is limited to less than 1 MHz, we integrate this phase noise from 1 kHz to 1 MHz, obtaining a jitter of 5.4 fs_{rms}. We then double the widths of all of the transistors, arriving at the second phase noise plot in Fig. 5(b) (denoted as the "scaled design"). The power dissipation



(a)



(b)

Fig. 5. (a) Retiming flipflop example, and (b) its phase noise for the original and scaled designs.

is doubled and the jitter falls to 3.5 fs_{rms}. We can conclude that the phase noise of dividers can be managed at a much lower power penalty than that of oscillators.

VIII. PLL Jitter-Power Trade-Offs for ADCs

The quest for higher ADC speeds and resolutions continues [19]–[22]. The sampling clock jitter in ADC design presents daunting challenges. In this section, we formulate the necessary VCO power consumption for a given ADC signal-to-noise ratio (SNR) penalty.

A. SNR Penalty Due to Jitter

Suppose an M-bit ADC senses an analog input of the form $x(t) = A_{in}\cos\omega_{in}t$ and samples it at $f_{CK} \approx 2f_{in} = 2(\omega_{in}/2\pi)$ (Fig. 6). An rms clock jitter of σ_j introduces a noise power given by $P_j = 2\pi^2 A_{in}^2 f_{in}^2 \sigma_j^2$ [23]. We wish to select P_j for no more than m dB of penalty in the ADC SNR:

$$\frac{A_{in}^2/2}{P_q} \div \frac{A_{in}^2/2}{P_q + P_j} = 10^{m/10}, \tag{28}$$

where P_q denotes the quantization noise power and is given by

$$P_q = \frac{1}{12}\left(\frac{2A_{in}}{2^M}\right)^2. \tag{29}$$

Substituting for P_q and P_j in (28) yields

$$\sigma_j^2 = \frac{10^{m/10} - 1}{3\pi^2 f_{in}^2 2^{2M+1}}. \tag{30}$$

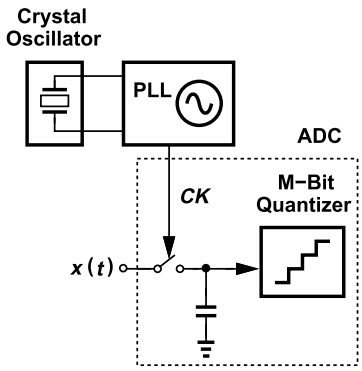


Fig. 6. ADC driven by a PLL.

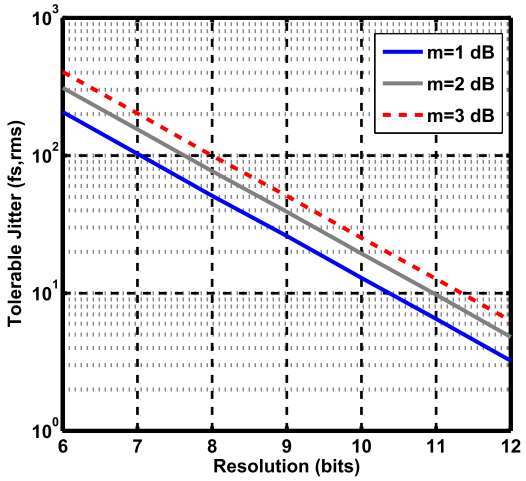


Fig. 7. Tolerable jitter for a 10-GHz ADC for SNR penalties of 1, 2, and 3 dB.

If $f_{in} \approx f_{CK}/2$, the maximum tolerable jitter for an m-dB SNR penalty is equal to

$$\sigma_j^2 = \frac{10^{m/10} - 1}{3\pi^2 f_{CK}^2 2^{2M-1}}. \tag{31}$$

For example, a 7-bit ADC sampling at 112 GHz requires $\sigma_j < 9.2\ \text{fs}_{rms}$ for a 1-dB penalty. As another example, a 12-bit 10-GHz converter can tolerate only 3.2 fs_{rms} for the same penalty. Figure 7 plots σ_j for such a sampling rate as a function of M and m. Also, Figure 8 shows the corresponding PLL bandwidth. Note that the bandwidth is deliberately limited to $f_{REF}/10 = 10$ MHz.

B. Lower Power Bound

The jitter constraint imposed by (31) naturally leads to a lower bound for the VCO power consumption according to (26). Replacing for σ_j in (26) from (31), we have

$$P_{VCO} = 9\pi^2 kT(1+\gamma)(S_{REF} + S_{CP}) \times \left[\frac{2^{2M-1} f_{CK}^2}{(10^{m/10} - 1)Qf_{REF}}\right]^2, \tag{32}$$

where S_{CP} is given by (25). In summary, this result prescribes the minimum necessary VCO power that guarantees at most an m-dB penalty in the SNR of an M-bit ADC.

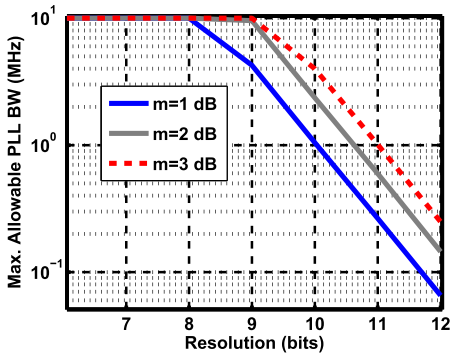


Fig. 8. Optimum PLL bandwidth for obtaining the jitter values shown in Fig. 7.

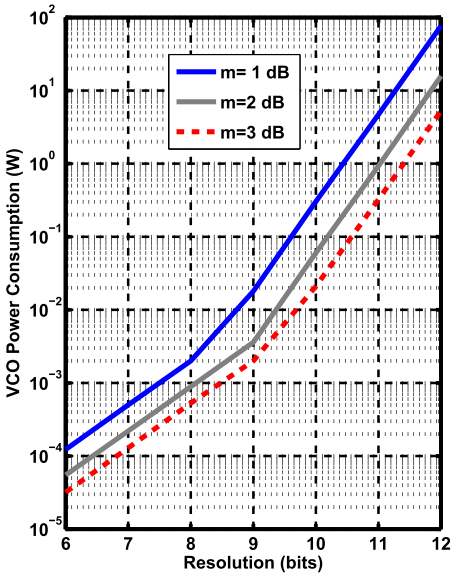


Fig. 9. VCO power consumption for a 10-GHz ADC for SNR penalties of 1, 2, and 3 dB.

Equation (32) suggests a number of troubling trends. First,

$$P_{VCO} \propto 2^{4M}, \tag{33}$$

implying that doubling the ADC resolution demands a 16-fold increase in P_{VCO}. By comparison, in ADC design, we typically encounter a twofold increase in the power, P_{ADC}, if the SNR is limited by the quantization noise. If the SNR is dominated by white noise, P_{ADC} quadruples for an extra bit of resolution. Thus, P_{VCO} can exceed P_{ADC} in the future.

To underscore this point, Fig. 9 plots the necessary P_{VCO} for $f_{CK} = 10$ GHz versus M, with m as a parameter. As an optimistic estimate, the CP contribution is excluded here. The kinks in the plots arise because the PLL bandwidth is not allowed to exceed $f_{REF}/10$. We observe that a 1-dB penalty for a 12-bit 10-GHz ADC calls for $P_{VCO} \approx 77$ W! Even for a 3-dB penalty, we have $P_{VCO} = 5.2$ W.

As another example, for the 12-bit 5-GHz 159-mW ADC in [22] to incur 3 dB of SNR penalty due to clock jitter, we have $P_{VCO} \approx 330$ mW. The charge pump noise further raises these power numbers.

The second difficulty revealed by Eq. (32) is that $P_{VCO} \propto f_{CK}^4$. For ADCs, on the other hand, P_{VCO} is typically proportional to f_{CK}. Consequently, doubling the conversion rate necessitates a 16-fold increase in P_{VCO} but a twofold increase in P_{ADC}.

C. PLL-ADC Power Trade-Off

Facing the grave picture portrayed by Eq. (32), we may surmise that the situation can be ameliorated if we design the ADC for a higher resolution and allow the PLL jitter to lower it to the desired value. Since $P_{ADC} \propto 2^M$ or 2^{2M}, whereas $P_{VCO} \propto 2^{4M}$, we expect that $P_{ADC} + P_{VCO}$ can be minimized.

Unfortunately, such an endeavor fails. As an example, suppose we redesign a 12-bit ADC for a resolution of 13 bits and allow a jitter penalty of 6 dB in the SNR. In Eq. (32), we must raise M to $M + 1$ and select $m = 6$ dB. But this raises the quantity within the square brackets by a factor of $2^2/(10^{6/10}-1) = 1.34$ and P_{VCO} by a factor of 1.34^2. In other words, the growth of 2^{2M} has a greater slope than that of $10^{m/10} - 1$.

IX. Mitigating Factors

In order to ease the jitter-power trade-offs derived in the previous sections, we revisit four of our assumptions.

First, the single-ended voltage swing of $V_{DD}/2$ in the LC oscillator of Fig. 2 can be increased to V_{DD}, but at the cost of flicker noise upconversion. As seen in the previous sections, the loop bandwidth falls well below 1 MHz, unable to suppress the effect of flicker noise if the corresponding flicker corner frequency is comparable. This issue can be resolved through the use of tail resonance at twice the oscillation frequency [25]. Second, other oscillators provide a higher FOM. For example, [26] reports a class-C topology achieving FOM = 196 dB with $Q \approx 16$. Similarly, class-D and class-F structures are attractive candidates [31], [32].

Third, the jitter-induced noise power in ADCs, $P_j = 2\pi^2 A_{in}^2 f_{in}^2 \sigma_j^2$ (Section VIII-A), is, in fact, pessimistic as it assumes that the analog input signal energy occurs at a single frequency. In practice, a random signal having a flat spectrum from zero to $f_{CK}/2$ incurs half of this noise power [33]. The analysis in [33] is for a general random signal having a flat spectrum between $-f_{CK}/2$ and $+f_{CK}/2$. One may surmise that such a signal occasionally exhibits large peaks in the time domain, requiring a lower sampling jitter. Nonetheless, the signal changes with a lesser slope at other times. That is, the average SNR still follows the derivation provided in [33].

Fourth, the reference phase noise of -170 dBc/Hz can be revisited in terms of power consumption, cost, and form factor. For example, Vectron's OX-305 crystal oscillator exhibits a phase noise of -178 dBc/Hz but draws 1.8 W [30].

X. Conclusion

This paper quantifies the trade-offs between the jitter and power consumption of VCOs for clock generation. It is observed that, in the presence of reference phase noise, P_{VCO} grows with $1/\sigma_j^4$. Moreover, ADC sampling clocks impose a P_{VCO} that climbs by a factor of 16 for each bit of resolution or each doubling of the sampling rate. These trends point to formidable challenges in PLL design.

REFERENCES

[1] Z. Zhang, G. Zhu, and C. P. Yue, "A 0.65 V 12-to-16 GHz sub-sampling PLL with 56.4 fsrms integrated jitter and −256.4 dB FoM," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 488–489.

[2] J. Gong, F. Sebastiano, E. Charbon, and M. Babaie, "A 10-to-12 GHz 5 mW charge-sampling PLL achieving 50 fsec RMS jitter, −258.9 dB FOM and −65 dBc reference spur," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Aug. 2020, pp. 15–18.

[3] D. Turker *et al.*, "A 7.4-to-14 GHz PLL with 54 fsrms jitter in 16 nm FinFET for integrated RF-data-converter SoCs," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 378–379.

[4] M. Mercandelli *et al.*, "A 12.5 GHz fractional-N type-I sampling PLL achieving 58fs integrated jitter," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 274–275.

[5] A. Santiccioli *et al.*, "A 66-fs-rms jitter 12.8-to-15.2-GHz fractional-N bang–bang PLL with digital frequency-error recovery for fast locking," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 268–269.

[6] W. Wu *et al.*, "A 28-nm 75-fsrms analog fractional-*N* sampling PLL with a highly linear DTC incorporating background DTC gain calibration and reference clock duty cycle correction," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1254–1265, May 2019.

[7] M. Mansuri and C.-K. Ken, "Jitter optimization based on phase-locked loop design parameters," *IEEE J. Solid-State Circuits*, vol. 37, no. 11, pp. 1375–1382, Nov. 2002.

[8] D. C. Lee, "Analysis of jitter in phase-locked loops," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 49, no. 11, pp. 704–711, Nov. 2002.

[9] X. Gao, E. A. M. Klumperink, P. F. J. Geraedts, and B. Nauta, "Jitter analysis and a benchmarking figure-of-merit for phase-locked loops," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 2, pp. 117–121, Feb. 2009.

[10] F. Herzel, S. A. Osmany, and J. C. Scheytt, "Analytical phase-noise modeling and charge pump optimization for fractional-*N* PLLs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 8, pp. 1914–1924, Aug. 2010.

[11] B. Razavi, "Lower bounds on power consumption of clock generators for ADCs," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Oct. 2020, pp. 1–5.

[12] J. Im *et al.*, "A 112 Gb/s PAM-4 long-reach wireline transceiver using a 36-way time-interleaved SAR-ADC and inverter-based RX analog front-end in 7 nm FinFET," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 116–117.

[13] T. Ali *et al.*, "A 460 mW 112Gb/s DSP-based transceiver with 38 dB loss compensation for next-generation data centers in 7 nm FinFET technology," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 118–119.

[14] E. Groen *et al.*, "A 10-to-112Gb/s DSP-DAC-based transmitter with 1.2 V_{ppd} output swing in 7nm FinFET," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2020, pp. 120–121.

[15] J. Kim *et al.*, "A 224 Gb/s DAC-based PAM-4 transmitter with 8-tap FFE in 10 nm CMOS," presented at the ISSCC, Feb. 2021.

[16] Y. Saito and Y. Nakamura, "256 QAM modem for high capacity digital radio system," *IEEE Trans. Commun.*, vol. COM-34, no. 8, pp. 785–799, Aug. 1986.

[17] B. Razavi, *Design of Analog CMOS Integrated Circuits*, 2nd ed. New York, NY, USA: McGraw-Hill, 2017.

[18] L. Romano, S. Levantino, S. Pellerano, C. Samori, and A. Lacaita, "Low jitter design of a 0.35 μm-CMOS frequency divider operating up to 3 GHz," in *Proc. ESSCIRC*, Sep. 2002, pp. 611–614.

[19] L. Kull *et al.*, "A 24-to-72GS/s 8b time-interleaved SAR ADC with 2.0-3.3 pJ/conversion and >30 dB SNDR at Nyquist in 14-nm CMOS FinFET," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2018, pp. 358–359.

[20] B. Hershberg *et al.*, "A 3.2 GS/s 10 ENOB 61 mW ringamp ADC in 16 nm with background monitoring of distortion," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 58–59.

[21] W. Jiang, Y. Zhu, M. Zhang, C.-H. Chan, and R. P. Martins, "A 7.6 mW 1GS/s 60 dB SNDR single-channel SAR-assisted pipelined ADC with temperature-compensated dynamic Gm-R-based amplifier," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 60–61.

[22] A. Ramkaj *et al.*, "A 5GS/s 158.6 mW 12b passive-sampling 8x-interleaved hybrid ADC with 9.4 ENOB and 160.5 dB FoM in 28 nm CMOS," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2019, pp. 62–63.

[23] M. Shinagawa, Y. Akazawa, and T. Wakimoto, "Jitter analysis of high-speed sampling systems," *IEEE J. Solid-State Circuits*, vol. 25, no. 1, pp. 220–224, Feb. 1990.

[24] P. Andreani, X. Wang, L. Vandi, and A. Fard, "A study of phase noise in colpitts and LC-tank CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 40, no. 5, pp. 1107–1118, May 2005.

[25] E. Hegazi, H. Sjoland, and A. A. Abidi, "A filtering technique to lower LC oscillator phase noise," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1921–1930, Dec. 2001.

[26] A. Mazzanti and P. Andreani, "Class-C harmonic CMOS VCOs, with a general result on phase noise," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2716–2729, Dec. 2008.

[27] K. M. Megawer *et al.*, "A fast startup CMOS crystal oscillator using two-step injection," *IEEE J. Solid-State Circuits*, vol. 54, no. 12, pp. 3257–3268, Dec. 2019.

[28] S. Iguchi, T. Sakurai, and M. Takamiya, "A low-power CMOS crystal oscillator using a stacked-amplifier architecture," *IEEE J. Solid-State Circuits*, vol. 52, no. 11, pp. 3006–3017, Nov. 2017.

[29] A. Karimi-Bidhendi, H. Pu, and P. Heydari, "Study and design of a fast start-up crystal oscillator using precise dithered injection and active inductance," *IEEE J. Solid-State Circuits*, vol. 54, pp. 2543–2555, Sep. 2019.

[30] *OX-305 at 100 MHz, Ultra Low Phase Noise Oven Controlled Crystal Oscillator*. Hudson, NH, USA: Vectron, 2019.

[31] L. Fanori and P. Andreani, "Class-D CMOS oscillators," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3105–3119, Dec. 2013.

[32] M. Babaie and R. B. Staszewski, "A class-F CMOS oscillator," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3120–3133, Dec. 2013.

[33] Z. J. Towfic, S.-K. Ting, and A. H. Sayed, "Sampling clock jitter estimation and compensation in ADC circuits," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2010, pp. 829–832.

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