

# A Compact Low-Power D-Band Receiver With Integrated LO Generation and Phase Shifting for Beamforming Applications

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**Abstract**—This article presents a 140-GHz low-power receiver with integrated local oscillator (LO) generation and phase shifting, using a 250-MHz external reference. The heterodyne receiver incorporates a low-impedance front-end interface to relax the noise-stability trade-off, a wide-locking-range subsampling phase-locked loop, a new quadrature oscillator, and a new phase shift technique for beamforming. Realized in 28-nm CMOS technology with an active area of 0.11 mm<sup>2</sup>, the system achieves a minimum noise figure (NF) of 4.7 dB, an overall oscillator jitter of 130 fs<sub>rms</sub>, and a phase shift range of 180° while consuming 40 mW.

**Index Terms**—Amplifier, beamforming, continuous-time linear equalizer (CTLE), delay line, gain, jitter, LNA, local oscillator (LO) path, mixer, noise figure (NF), phase shifting, PLL, quadrature voltage-controlled oscillator (QVCO), RF path, subsampling.

## I. INTRODUCTION

RECENT work on 6G radios operating in the D-band has addressed many challenges at circuit and architecture levels [1], [2], [3], [4], [5], [6], [7], [8], [9], [10], [11], [12], [13], [14], [15], [16], [17], [18], [19], [20], [21]. For such radios to find traction in the consumer market, both their power consumption and cost must outperform those of Wi-Fi, when normalized to the data rate. To this end, [9] has reduced the power per element to 98 mW while incurring a noise figure (NF) of 7.8 dB and deferring beamforming to off-chip digital processing and requiring a 2.82-GHz external reference. As additional examples, [1], [4] demonstrate two-channel receiver architectures; however, they consume 148 and 197 mW per channel, respectively, and require an external reference signal at 17–23 GHz without enabling beamforming. The receivers reported in [2] and [3] consume more than 145 mW, have NFs of 7.2 and 8.2 dB, respectively, and require external 72-GHz and 140-GHz references, thereby increasing complexity. Agrawal et al. [8] draw 123 mW per element with NF = 12.4 dB but also without beamforming capability. Although the works in [18] and [19] implement beamforming in the receiver system using a multichip implementation, in which subblocks [receiver front-end, mixer, and local oscillator (LO)

generation] are realized on separate chips, these approaches reduce integration density and scalability. A low NF is critical for D-band receiver systems because it improves sensitivity and link budget to mitigate path loss [30], [34]. Implementing a compact, low-loss phase shifter for beamforming remains challenging at these frequencies and often requires higher power consumption. In addition, LO generation consumes a substantial fraction of total power in D-band receivers [1], [5], [6]. Furthermore, LO phase noise degrades receiver signal-to-noise ratio (SNR), so low-jitter LO generation is also important for high-performance receivers [1], [6], [43], [44].

This article proposes a compact receiver (RX) with dedicated LO generation for beamforming systems. A number of new techniques are introduced that improve both the signal and LO paths, resulting in a minimum NF of 4.7 dB, a total power consumption of 40 mW, and a phase shift range up to 180°, making this receiver a key enabler for power-efficient, integrated, and scalable D-band microwave beamforming systems. The main contributions include a low-impedance receiver front-end that relaxes the noise-stability trade-off at D-band frequencies; a wide-locking-range subsampling PLL for low-power LO synthesis; a new quadrature voltage-controlled oscillator (QVCO) for quadrature LO generation with improved phase noise and mode-ambiguity resolution; and an LO phase shift mechanism integrated within the PLL for beamforming. In addition, an intermediate-frequency mixer design contributes to improved receiver gain and overall noise performance. Collectively, these techniques enable low-power consumption, low NF, and integrated LO phase shift capability. The proposed work also achieves a compact floorplan for receiver and LO integration, particularly at the PLL-mixer interface. This article is an extended version of [31], presenting substantial new material for detailed discussion and analysis of the proposed techniques. Additional design and implementation details, along with comprehensive experimental results, are presented. Section II provides a brief background, and Section III describes the proposed RX architecture. Sections IV and V delve into the design of the RX and LO building blocks, respectively, and Section VI presents the experimental results.

## II. BACKGROUND

### A. Choice of Architecture

While direct conversion is generally attractive for receiver design, we must examine some of its properties for operation in the D-band. Due to limited speed, it is challenging to synthesize the in-phase (I) and quadrature (Q) phases of LO at

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140 GHz for direct downconversion using a frequency divide-by-two stage from a 280 GHz source. Consider the scenario shown in Fig. 1, where the LO directly generates quadrature phases at 140 GHz. We recognize two grave issues here.

- 1) The first frequency divider stage in the PLL feedback path, e.g., a  $\div 2$  circuit, must operate robustly at this frequency. This is a daunting challenge because frequency divide-by-two suffers from limited speed at 140 GHz without an inductor, and even after using an inductor, [38] shows that it requires 4–5 dBm of power in the SiGe BiCMOS process, thus imposing a risk on PLL operation. It is possible to avoid this issue through the use of frequency multipliers [1], [12], but typically at the cost of high power consumption (e.g., 71 and 38 mW, respectively) and without quadrature phases [1], [12].
- 2) Even a 1-ps mismatch between the traces carrying the I and Q phases of the LO to the downconversion mixers translates to  $51^\circ$  of phase mismatch. These thoughts point to heterodyne downconversion as a potentially more practical approach (Section III).

### B. Phase Shift Techniques for Beamforming

The elements in a beamforming environment can implement the necessary phase shift in the RF [10], [11], [13], [19], LO [15], [18], or baseband (BB) paths [16], [17] with the hardware and power overhead increasing in that order. The implemented true time delay circuit in [23] incurs a loss of 20 dB, which also degrades the NF. The vector modulator active phase shifter in the RF path has a loss of 4 dB and consumes 50 mW power [22]. Phase shifters in the RF path can be realized as true time delays [11], [23] so as to accommodate a wide channel bandwidth (BW),  $f_{BW}$ , but this becomes necessary only if  $f_{BW}$  does not satisfy this relation

$$f_{BW} \ll \frac{4f_0}{n-1} \quad (1)$$

where  $f_0$  and  $n$  denote the carrier frequency and the number of elements, respectively [35]. With  $f_0 = 140$  GHz and  $n = 8$ , for example,  $f_{BW}$  can reach nearly 10 GHz with no need for true time delays. We opt for such a scenario and propose a phase shift method for the LO path, avoiding any loss due to phase shift. Two aspects of LO phase-shifting are worth mentioning: beam squinting in the spatial domain and intersymbol interference (ISI) in the time domain [35]. The former is discussed in Section VI-C, and (1) ensures avoidance of array ISI [35]. The key advantage of our approach is that it implements the phase shift at a *low* frequency.

### C. LO Distribution

The distribution of the LO, especially when quadrature components are required, poses serious challenges for multichannel and beamforming systems, regardless of the beamforming architecture. For example, [1] resorts to an external LO frequency of about 17 GHz, multiplies it by 3, followed by a buffer and multiply-by-two stage before distributing the result to two channels, and locally feeds the mixer through additional buffer stages per channel to generate an intermediate

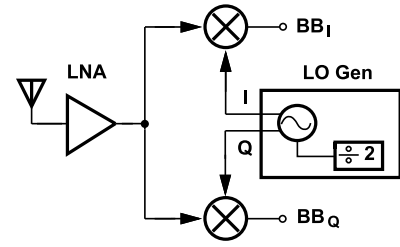


Fig. 1. Direct conversion receiver.

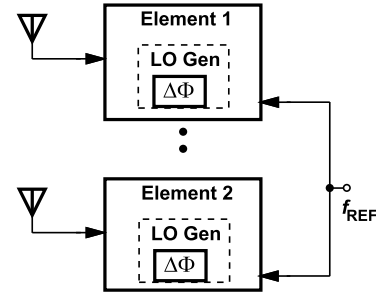


Fig. 2. Proposed LO beamforming architecture.

frequency (IF) of 26–34 GHz. Excluding the external LO, the LO network consumes 89 mW per channel. Similarly, the LO distribution network consumes more than 71 mW per element in an eight-element IF-beamforming receiver reported in [17]. LO power consumption, including the I/Q generation network, is 137 mW in [5]. In another example, [15] demonstrates an LO beamforming scheme in a D-band transmitter, where an external 13.8–15.5 GHz LO is distributed to each of four elements. Within each element, the LO signal passes through a phase shifter, a frequency tripler, quadrature generation, and an additional frequency tripler stage to drive the mixers. The power consumption per element in this design is 232 mW. Furthermore, although [6] uses a 40 MHz external reference for a single-element receiver to generate 12 GHz on-chip via a PLL, it then employs two frequency doublers in cascade. The PLL and the rest of the LO path consume 55 and 210 mW, respectively, and exhibit more than 700 fs jitter at the output of the PLL at 12 GHz. Thus, LO generation and distribution account for a significant portion of the power budget and pose a key bottleneck for D-band beamforming and multichannel systems.

We propose a per-element LO generation scheme that requires the distribution of only a 250-MHz reference,  $f_{REF}$ , to the elements. Illustrated in Fig. 2, the idea is to develop each element and its LO generation as a stand-alone block, with the LO phase shift,  $\Delta\Phi$ , also localized. For any independent phase offset between the elements, the initial phase difference can be compensated by appropriate adjustments to the phase shift code [18] and does not implement any on-chip calibration, as proposed for two LO elements in [46], which can increase complexity for more than two elements. The architecture of Fig. 2 appears to entail a great deal of overhead due to the dedicated LO networks, making it unclear whether it indeed offers a power advantage. Nonetheless, as demonstrated in subsequent sections, our approach consumes only a fraction of the power drawn by schemes employing frequency multipliers, passive phase shifters, and buffers.

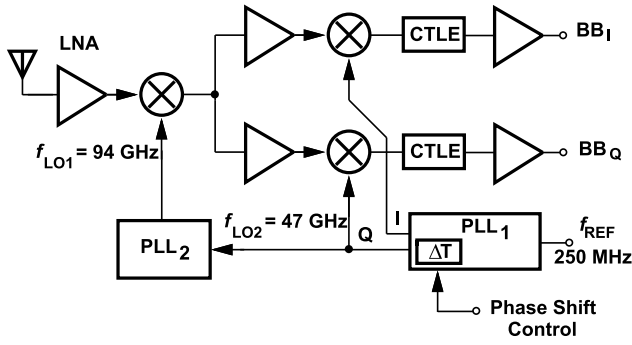


Fig. 3. Proposed receiver architecture.

### III. RECEIVER ARCHITECTURE

Shown in Fig. 3 is the heterodyne RX architecture [36]. The input signal is mixed with  $f_{LO1} = 94$  GHz, yielding an IF at 47 GHz. The result is then downconverted to BB by means of quadrature phases of  $f_{LO2} = 47$  GHz. Finally, the BB outputs travel through continuous-time linear equalizers (CTLEs) [6]. The LO generation network consists of PLL<sub>1</sub>, which multiplies  $f_{REF} = 250$  MHz to 47 GHz, and PLL<sub>2</sub>, which acts as an efficient frequency doubler. The separation and distribution of the I/Q components of the LO occur at 47 GHz rather than at 140 GHz, relaxing phase matching requirements [6], [15].

Several distinct attributes differentiate this receiver from the prior art, enabling sub-5 dB NF, low power, and a compact, efficient phase shift mechanism. First, a low-impedance interface in the second stage of the receiver front end is employed at sub-THz frequencies to improve noise performance and stability. A 47-GHz IF mixer design with enhanced gain improves overall receiver NF, which is critical for receiver sensitivity in a D-band beamforming system. Second, a wide-tuning-range subsampling PLL (PLL<sub>2</sub>) is proposed as a frequency doubler to reduce LO power consumption. Third, a new 47-GHz QVCO is implemented in PLL<sub>1</sub> to generate I/Q phases, resolve mode ambiguity, and improve phase noise and jitter, which is important for a high SNR. The LO path, including PLL<sub>1</sub> and PLL<sub>2</sub>, consumes only 17 mW of the total 40 mW. Fourth, the phase shift network,  $\Delta T$ , required for LO beamforming is embedded in the feedback path of PLL<sub>1</sub> and consumes less than 0.5 mW. We also incorporate no buffers between PLL<sub>1</sub> and PLL<sub>2</sub> and their respective mixers [54], thereby saving power and achieving a compact floor plan at the mixer and PLL interface for easy integration.

### IV. RECEIVER CHAIN

In our presentation of various concepts in this article, we report certain simulation results. Given the high frequencies involved, we focus on only results obtained from the extracted layout, with all inductors, transformers, and most interconnects, including the input signal pad, modeled in EMX and HFSS. Inductors and transformers are initially designed and optimized in HFSS, and exhibit good agreement with the corresponding EMX simulations in the 140-GHz band. Subsequently, all inductors, transformers, and important routing interconnects are co-extracted in EMX to capture mutual coupling and parasitic interactions. Therefore, the final circuit

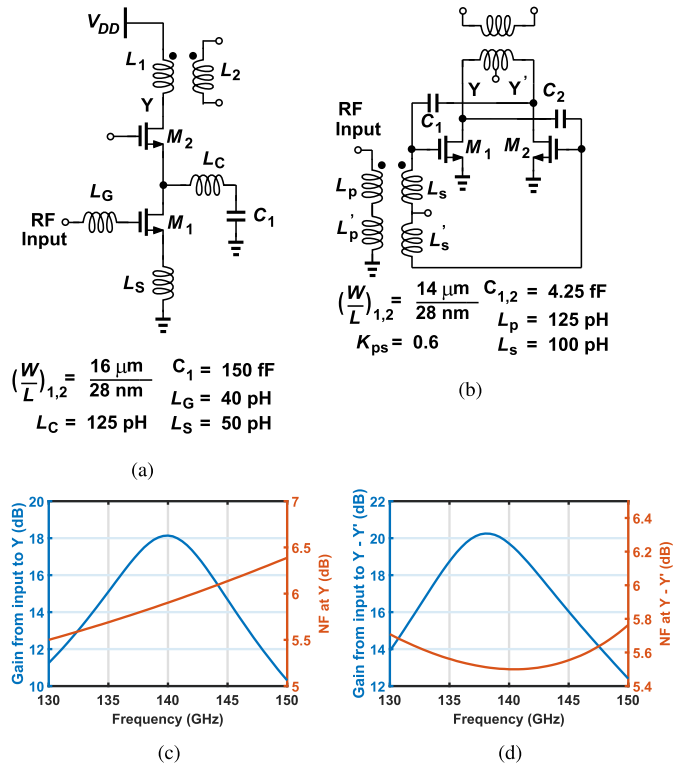


Fig. 4. (a) Cascode LNA, (b) neutralized differential LNA, (c) gain and NF performance of cascode LNA, and (d) neutralized differential LNA.

simulations are based on this EMX-extracted EM model, which shows reasonable agreement with the measurement results. These EM extractions utilized foundry-provided stack-up and metal thickness. 27 °C is used for these simulations. It is worthy to mention that active transistors are low-threshold-voltage (LVT) devices.

#### A. General Consideration

With an  $f_{max}$  of approximately 450 GHz, 28-nm CMOS technology presents significant trade-offs in low-noise amplification in the D-band. While cascode topologies [14], [19] are attractive for their stability by improving reverse isolation, simulations reveal a NF of about 6 dB for such structures even with resonance at their cascode node [Fig. 4(a) and (c)]. Without a cascode device, one must contend with feedback due to the gate-drain capacitance, often resorting to neutralization in a fully-differential signal path [Fig. 4(b)] [1], [4], [5], [6], [8], [9], [10], [12], [13], [27]. Unfortunately, the loss of the input balun and the noise contribution by both  $M_1$  and  $M_2$  still pose a lower bound of about 5.5 dB on this LNA's NF from input to nodes Y and Y' [Fig. 4(d)].

These thoughts suggest that the drain of the input transistor must still see a low impedance to guarantee stability. Intuitively, a low drain impedance reduces the effect of intrinsic feedback from gate-to-drain capacitance around a transistor for stability; but such an impedance must be established by a device other than a cascode transistor. The proposed topology in Section IV-B addresses this requirement by providing a low-impedance interface in an alternative way while avoiding NF degradation and making it well-suited for a D-band receiver system.

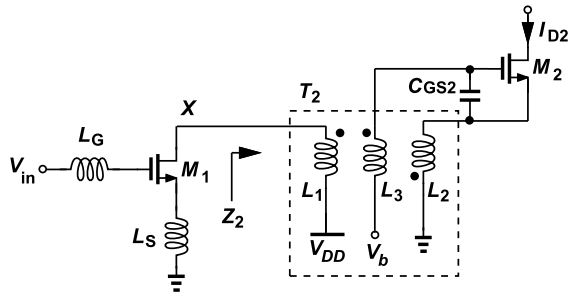


Fig. 5. Proposed simplified receiver front-end.

### B. Proposed LNA

Depicted in Fig. 5 in simplified form, the LNA consists of an inductively degenerated transistor,  $M_1$ , a trifilar transformer,  $T_2$ , and a second transistor  $M_2$ . This structure offers several benefits. First, it presents a low impedance to the drain of  $M_1$ , thereby ensuring the input stage's stability. Second, it boosts the gain. Third, it partially suppresses the noise of  $M_2$ . Fourth, it also provides stability in the second stage without a neutralization technique. A trifilar transformer-based LNA was previously reported at 140 GHz [31], 40 GHz [28], and 70 GHz [29]; However, these implementations have not identified the role of the trifilar transformer in stability enhancement or unilateralization at sub-THz frequencies. This article presents new design insights for low impedance, noise suppression, and stability at sub-THz frequencies and provides an intuitive understanding of these properties that differentiate the proposed design from prior work. We elaborate on these insights below.

To understand how the trifilar transformer creates a low impedance at node X in Fig. 5, we denote the mutual inductance between  $L_i$  and  $L_j$  by  $M_{ij}$  and define a series resonance frequency

$$\omega_S = \sqrt{\frac{1}{C_{GS2}(L_2 + L_3 + 2M_{23})}}. \quad (2)$$

It can be shown that the equivalent resistance seen by  $L_3$  at  $\omega_S$  is given by  $R_3 = g_{m2}(L_2 + M_{23})/C_{GS2}$ , which is similar to the input resistance of a simple inductively-degenerated CS stage. The coupling between the inductors transforms this resistance to

$$R_2 = \text{Re}\{Z_2\} = \frac{\omega_S^2 C_{GS2} (M_{12} + M_{13})^2}{g_{m2} (L_2 + M_{23})}. \quad (3)$$

To gain more insight, we write  $\omega_t = g_{m2}/C_{GS2}$  and hence,

$$R_2 = \left(\frac{\omega_S}{\omega_t}\right) \cdot \frac{(M_{12} + M_{13})}{(L_2 + M_{23})} \cdot \omega_S (M_{12} + M_{13}). \quad (4)$$

In this work, the first and second fractions are approximately equal to 0.36 and 0.77, respectively, and the last term,  $(M_{12} + M_{13})\omega_S$ , amounts to 70  $\Omega$ . Thus,  $R_2 \approx 20 \Omega$ . A detailed step-by-step approach is included in Appendix A. This proposed low-impedance technique, developed for 140-GHz operation, provides important design insights and a cross-stage stabilization approach in which the second-stage architecture stabilizes the preceding single-ended first stage.

To understand how the noise of  $M_2$  is canceled, consider the equivalent circuit shown in Fig. 6(a), where  $I_{n2}$  represents

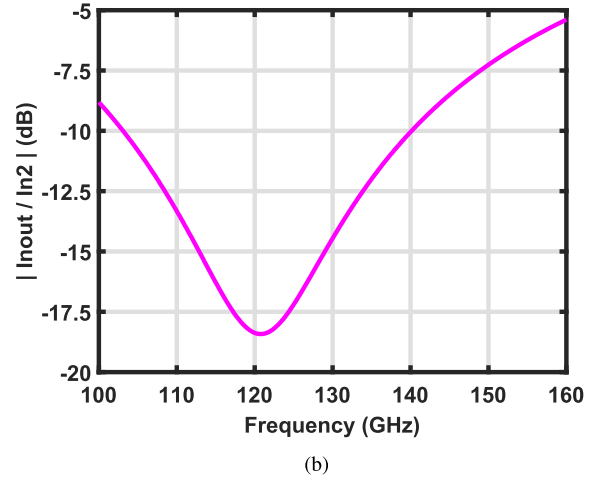
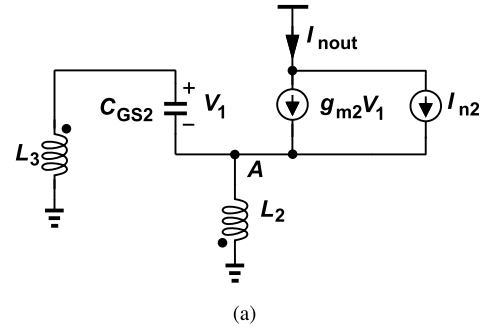


Fig. 6. (a) Small-signal model for noise analysis and (b) noise current transfer function of the second stage.

the noise of  $M_2$ , and the effect of  $L_1$  is neglected. With ideal inductors, KCL at A yields

$$\begin{aligned} I_{nout} &= -\frac{1 - \omega^2 C_{GS2} (L_2 + L_3 + 2M_{23})}{j\omega (L_2 + M_{23})} V_1 \\ &= g_{m2} V_1 + I_{n2}. \end{aligned} \quad (5)$$

At the series resonance frequency,  $\omega_S$ , we have  $g_{m2} V_1 = -I_{n2}$  and  $I_{nout} = 0$ .

The actual circuit exhibits the response,  $|I_{nout}/I_{n2}|$ , depicted in Fig. 6(b), revealing a suppression of 10 dB at 140 GHz. In this work,  $\omega_S = 2\pi(125 \text{ GHz})$  because some priority is given to gain optimization at 140 GHz. The simplified analysis in (5) shows that the resonance frequency  $\omega_S$ , primarily determined by the secondary side of the trifilar transformer and  $C_{GS2}$ , is the dominant factor in noise suppression at 140 GHz. This provides a clearer architectural interpretation, revealing that noise suppression is fundamentally resonance-based, a principle not explicitly identified in the prior art. The  $C_{GD2}$  capacitance of the  $M_2$  device and input stage loading through  $L_1$  reduce the frequency at which the minimum  $|I_{nout}/I_{n2}|$  occurs, to 121.7 GHz in Fig. 6(b). For the response plot ( $|I_{nout}/I_{n2}|$ ), an AC current source is applied between the drain and source of the  $M_2$  transistor in simulation of actual implementation (Section IV-C), and the differential short-circuited load output current is measured at the drain from PSS/PAC analysis [36].

The proposed second stage also provides gain boosting from node X to the drain of  $M_2$  in Fig. 5. This occurs because the polarity of coupling between  $L_3$  and  $L_2$  is chosen such that the gate and source voltages of  $M_2$  change in opposite directions.

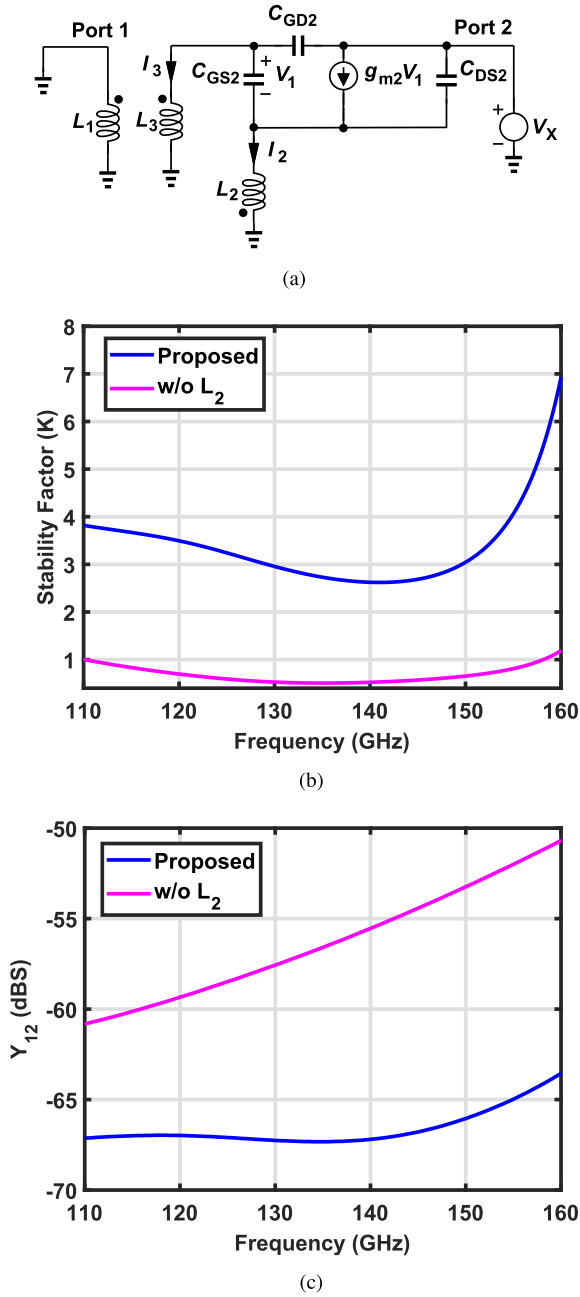


Fig. 7. (a) Small-signal model for stability analysis, (b) stability factor, and (c)  $Y_{12}$  of the second stage.

The second stage in Fig. 5 does not employ neutralization and yet it is stable. Notably, the trifilar transformer helps in unilateralization of this second stage, suppressing  $Y_{12}$  by 12 dB. This is because the drain–source capacitance of  $M_2$ , an inevitable parasitic arising from drain and source vias, counteracts the effect of  $C_{GD2}$ . Consider the simplified circuit of the second stage shown in Fig. 7(a), where we wish to minimize  $|Y_{12}|$  and hence maximize the stability factor,  $K \propto |Y_{12}|^{-1}$  [32]. We observe that  $V_X$  generates a current through  $C_{GD2}$ , and contributes to  $I_3$ . Also,  $V_X$  produces a current through  $C_{DS2}$  and hence  $I_2$ . With the coupling polarities that we have chosen, the induced voltages in  $L_1$  due to  $I_2$  and  $I_3$  partially cancel each other, yielding a small  $|Y_{12}|$ . Fig. 7(b) plots the simulated  $K$ , defined in [32], with and without  $L_2$ ,

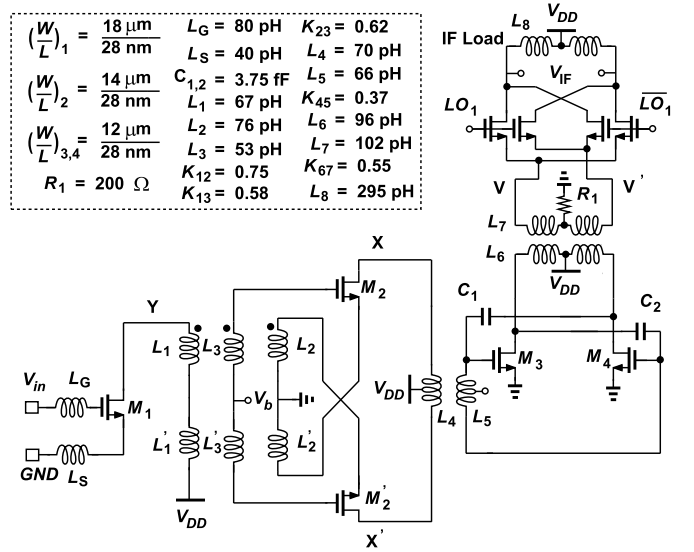


Fig. 8. Proposed receiver front-end (biasing not shown).

demonstrating another benefit of the trifilar network. Because front-end stability is a critical design challenge at 140 GHz, the proposed second-stage design demonstrates that the trifilar transformer-based architecture inherently improves the stability factor and enhances unilateralization without additional neutralization techniques. This benefit arises from coupling-assisted suppression of  $Y_{12}$ , a mechanism not reported in prior art [28], [29]. Without  $L_2$ , the second stage exhibits higher  $Y_{12}$  [Fig. 7(c)] and stability factor below unity [Fig. 7(b)]. The simulation setup for Fig. 7(b) and (c) includes the first port at the input of the trifilar transformer, with no loading from the first stage, and the second port at the drain of the  $M_2$  device in its differential implementation (Section IV-C), with next-stage loading. Even after the first-stage loading is included, the stability factor of this second stage remains below unity without  $L_2$ .

### C. Complete Front End

As shown in Fig. 8, the actual front end employs differential paths after the input stage. The third stage, consisting of  $M_3$  and  $M_4$ , acts as a transconductor and delivers an RF current through its balun to the RF mixer switching devices. The decision between single-ended and differential topologies is made as follows. NF considerations lead to a single-ended inductively degenerated [36] first stage (input stage) and eliminate the transformer at the beginning, while its supply and ground (on-chip) parasitics can be managed by placing the circuit near the input pads depicted in Fig. 9(a). The second stage, on the other hand, is chosen as differential to reject the common mode. Shown in Fig. 9(a),  $L_G, L_S$ , and the trifilar transformer are implemented with the top two metals,  $M_9$  and  $M_8$ , of this technology, where  $M_9$  is approximately  $4 \mu\text{m}$  above the substrate. The width of all three turns is about  $4.5 \mu\text{m}$  with a Quality factor above 10. The EM-parameters of the trifilar transformer are presented in Fig. 9(b) and (c). The  $G_1$  and  $G_2$  terminals of  $L_3$  and  $L'_3$  and the  $S_1$  and  $S_2$  terminals of  $L_2$  and  $L'_2$  are connected to the gate and source of the devices ( $M_2$ ,

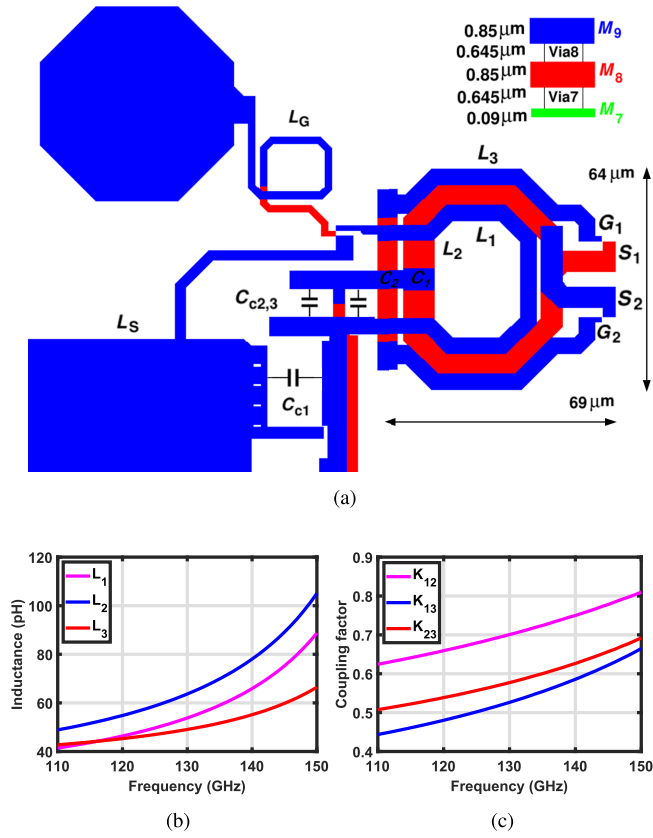


Fig. 9. (a) Floor plan of the input-matching and trifilar-transformer sections, (b) inductance, and (c) coupling factors of the trifilar transformer.

$M_2'$ ), respectively. The two center-tap terminals,  $C_1$  of  $L_2$  and  $L_2'$ , and  $C_2$  of  $L_3$  and  $L_3'$ , are AC-coupled through  $C_{c1}$  and  $C_{c2,3}$  to the primary side ( $V_{DD}$ ) and input ground pad in Fig. 9(a). The ESD diodes are integrated with the signal pad. They protect the active device  $M_1$  in the single-ended input stage shown in Fig. 8 from ESD events. The integrated ESD diodes contribute approximately 0.21 dB of NF degradation. They also affect S11 by introducing additional capacitive loading at the input signal pad. The presented NF and S11 results already account for these effects of the integrated ESD.

The common-mode gate bias for the second and third stages is provided through the transformer's center-tap point in Fig. 8. For example, the gate bias voltage for  $M_2$  and  $M_2'$  transistors, generated internally on the chip, is connected to the center-tap point  $V_b$  of the trifilar transformer, avoiding the use of gate-bias resistors in the signal path. In the proposed receiver, the interstage transformer inherently provides this center-tap node for common-mode biasing. In designs where the transformer does not offer a center tap, direct gate-bias resistors can be used with similar performance. Appendix B provides a detailed discussion of the common-mode bias stability of the second stage. Similarly, the common-mode gate bias for the third-stage devices ( $M_3$  and  $M_4$ ) is provided through the center-tap point of  $L_5$ . Both stages use dedicated bias-voltage generation networks.

Fig. 10 plots various simulated parameters of the front end up to nodes X and X' in Fig. 8. The voltage gain ranges from 17 to 27 dB, and NF varies from 3.5 to 5 dB across a 20-GHz

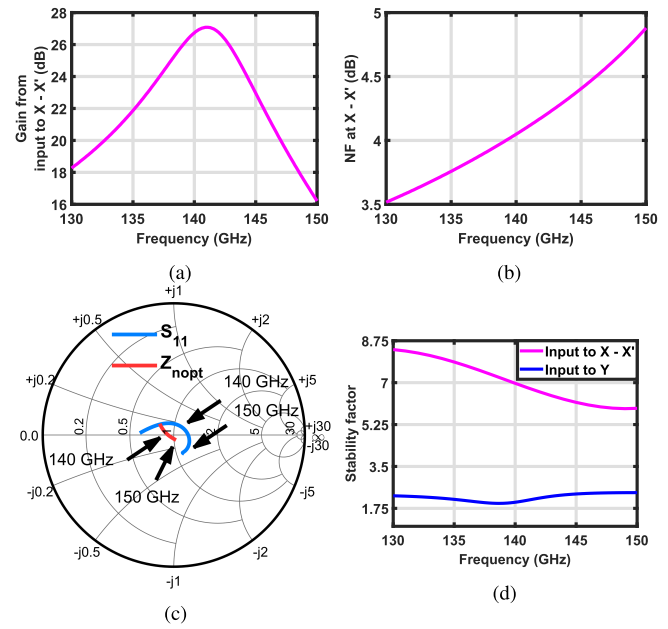


Fig. 10. (a) Voltage gain up to node X-X' in Fig. 8, (b) NF, (c) S11 and  $Z_{nopt}$  in smith chart from 130 to 150 GHz, and (d) stability factor.

band as obtained from PSS/PAC/PNOISE simulation. The  $M_2$  and  $M_2'$  devices contribute less than 8% to the 4.1 dB NF at 140 GHz differentially between X and X' in Fig. 10(b) due to the aforementioned noise cancellation effect with the trifilar transformer. Without  $L_2$  and  $L_2'$ , the NF rises above 5 dB at 140 GHz, and the contribution of  $M_2$  and  $M_2'$  devices is more than 30%. The (5) in Section IV-B also suggests that  $I_{nout} = I_{n2}$  without  $L_2$ . The input return loss is better than -12 dB. Fig. 10(c) plots S11 and the optimum noise impedance ( $Z_{nopt}$ ) at the receiver input from 130 to 150 GHz.  $Z_{nopt}$  shows broadband optimum noise matching. Both impedances are very close to 50  $\Omega$  at 140 GHz, so simultaneous noise and power matching can be achieved with the proposed receiver front end. It is worth noting that only the input is power-matched, whereas we deal with voltage quantities inside the receiver chip because the distance between the stages (75  $\mu\text{m}$ ) is much smaller than the wavelength of interest. The Gain and S11 of Fig. 10 are simulated with an AC-coupled single port at the input, whereas a second port is placed at node Y or differentially between X and X' for the NF and stability simulations. NF can also be simulated using a single port at the input and selecting the output-voltage nodes between X and X'. Depicted in Fig. 10(d), the input-stage stability factor is greater than 1.9 across a wide band due to the low impedance provided by the second stage (Section IV-B). The stability factor exceeds 5.5 when measured between the input to X and X' is presented in Fig. 10(d). S11,  $Z_{nopt}$ , and the stability factor shown in Fig. 10(c) and (d) are obtained using SP simulation. The gain response in Fig. 10(a) is obtained using PSS/PAC simulation because nodes X and X' in Fig. 8 are connected via the  $L_4/L_5$  transformer to the gates of  $M_3$  and  $M_4$ ; these devices are coupled to the RF mixer switching quad through the  $L_6/L_7$  transformer. The differential impedances at X-X' and at the gates of  $M_3$  and  $M_4$  are primarily determined by the  $L_4/L_5$  transformer network and the RF mixer switching-quad

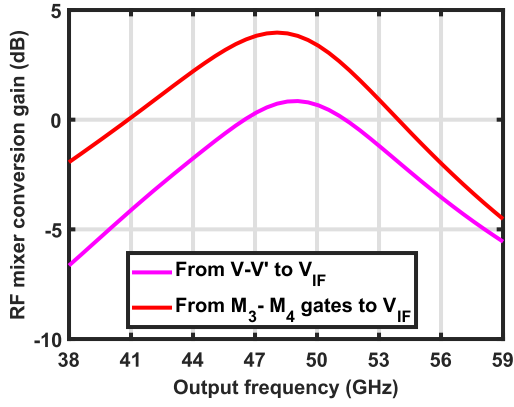


Fig. 11. RF mixer conversion gain from  $M_3$ - $M_4$  gates and  $V$ - $V'$  to  $V_{IF}$ .

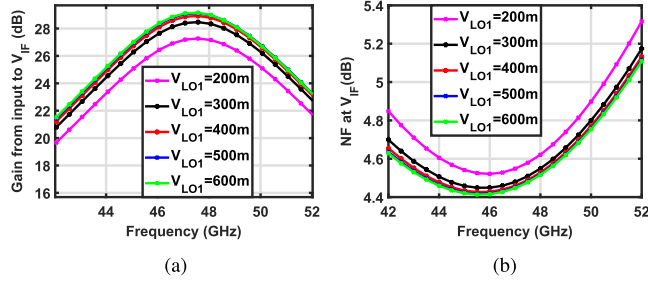


Fig. 12. (a) Gain and (b) NF to the RF mixer output in the receiver chain with  $LO_1$  swings.

loading under LO-driven, time-varying switching operation. These impedances are part of the receiver's gain and noise optimization. Therefore, PSS/PAC analysis more accurately captures the receiver gain than an isolated interstage analysis.

The input AC coupling capacitance is not used in the proposed design. In the measurement, the probe tip, after landing on the signal pad in Fig. 9(a), has the same LNA gate-bias voltage as the input stage. The gate bias is applied through a series 10 k $\Omega$  resistor to the gate of  $M_1$  in Fig. 8. No external biasing is used. If 100 fF of AC coupling capacitance, implemented as a metal capacitor, is applied at the input in simulation, the NF degrades by 0.32 dB.

The VCO in  $PLL_2$  sets the common mode gate voltage (550 mV) of the nMOS switching quad in the RF mixer through  $LO_1$  and  $\overline{LO}_1$  lines in Fig. 8. The sizes of the nMOS switching quad (3  $\mu$ m/28 nm) are chosen primarily to minimize capacitance loading on the VCO while preserving the low NF performance of the receiver chain. The resistance,  $R_1$ , in the common-mode path sets the current of the switching devices. The source voltage of these switching quad devices is approximately 220 mV. The conversion gain of the standalone RF mixer switching quad is shown in Fig. 11, with a peak of 0.67 dB. When evaluated from the gates of  $M_3$  and  $M_4$  differentially to  $V_{IF}$ , the gain rises to 3.97 dB. The two-sided BW of the RF mixer is 11 GHz. The gain and NF at the RF mixer output in the receiver chain nearly remain unchanged in Fig. 12(a) and (b) when the peak LO swing goes above 300 mV. The RF mixer in Fig. 8 employs a resonant load, IF load ( $L_8$ ), centered around 47 GHz and providing 1 V DC bias to the drain of the switching quad at node  $V_{IF}$ . If designed for a wide BW, such a load suffers from a low Q, yielding an

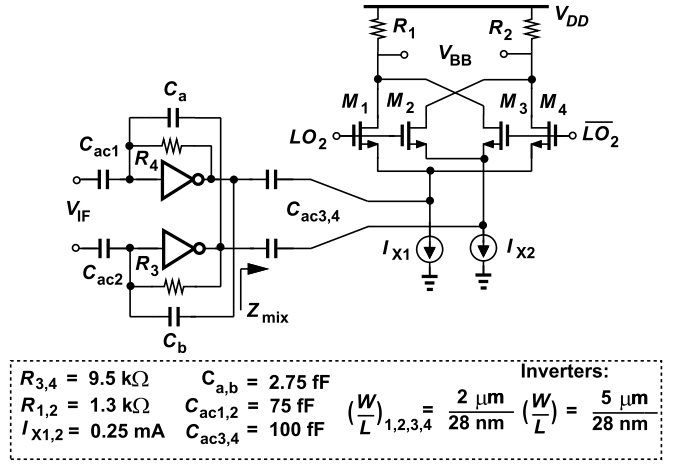


Fig. 13. Proposed IF mixer architecture.

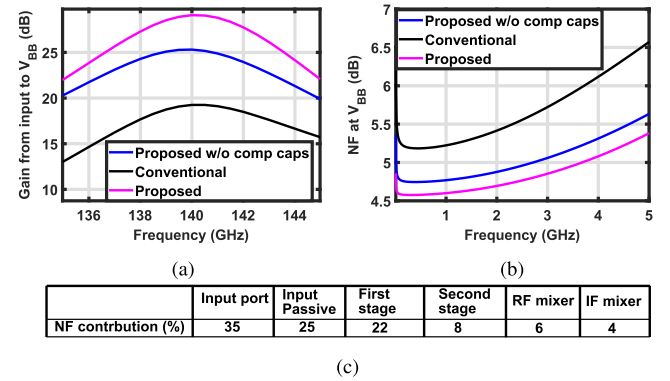


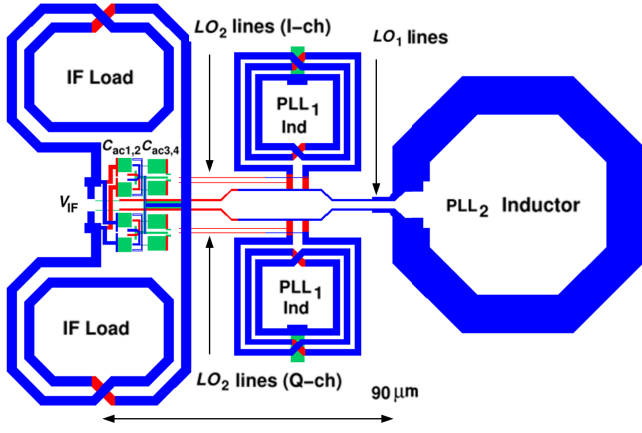
Fig. 14. (a) Gain to the IF mixer output with input frequency, (b) NF DSB to the IF mixer output, and (c) NF contribution breakdown up to the IF mixer output.

excessively low conversion gain for the mixer. We select a loaded Q of 7.8 and hence a two-sided BW of 6 GHz in the receiver chain. To accommodate wider channels, we introduce equalization in the BB (Section IV-E).

As discussed in Appendix A and Section IV-B, node Y in Fig. 8 exhibits wideband, low-impedance behavior when implemented with the trifilar transformer. The analytical evaluation of  $V_C/I_1$  in Appendix A likewise indicates a wideband response. Together, these results show that the trifilar transformer does not impose an RF BW limitation on either side. Furthermore, the EM-simulated parameters of the trifilar transformer in Fig. 9(b) and (c) show that its self-resonant frequency is well above the band of interest. Therefore, the receiver's RF BW is not limited by the trifilar transformer. The RF BW of the receiver is primarily set by the resonant differential impedances at three locations in Fig. 8: the node pair X-X', the gate nodes of  $M_3$  and  $M_4$ , and the output of the RF mixer ( $V_{IF}$ ). The first ( $M_1$ ), second ( $M_2$ ,  $M_2'$ ), third stage ( $M_3$ ,  $M_4$ ), and nMOS switching quad of this low-power receiver consume 3.6, 5.2, 4.0, and 1.1 mA, respectively.

#### D. IF Mixers

Realized as active topologies, the 47-GHz IF mixers incorporate resistive loads and face a severe trade-off between their gain and the supply voltage in a conventional architecture


 Fig. 15. Mixer interface with PLL<sub>1</sub> and PLL<sub>2</sub>.

where an nMOS transconductor is DC-coupled to the switching quad [36]. We present two techniques to improve their performance. First, we employ a complementary transconductor (i.e., a self-biased inverter) with capacitive coupling through  $C_{ac3,4}$  to the switching quad (Fig. 13). Owing to the relaxed gain-headroom trade-off, the circuit achieves 5.5 dB higher voltage gain and 0.4 dB less NF at the IF mixer output (Fig. 14). But the gate-to-drain capacitance of the self-biased inverter provides a resistive loading at its input in a similar way that a capacitive feedback LNA realizes a real input impedance [26]. Second, to counter this effect, we add negative Miller capacitors (comp caps),  $C_a$  and  $C_b$ , thereby reducing the load seen by the RF mixer and improving the voltage gain (Fig. 14). The  $C_a$  and  $C_b$  values are chosen close to the combined gate-to-drain capacitance of the self-biased inverter. A lower  $Z_{mix}$  magnitude of 380  $\Omega$  in the proposed design compared to  $R_{3,4}$  of 9.5 k $\Omega$  and the output resistance of the inverters in Fig. 13 enables the self-biased inverters to deliver the majority of signal current toward the switching quad of the IF mixer. The BW of the transconductance gain of this inverter-based active  $g_m$ -stage exceeds 50 GHz.

With these modifications, Fig. 14(a) and (b) presents the simulated performance of the receiver up to the output of the IF mixer. The RX gain to the IF-mixer output rises from 19.5 to 29 dB, and its NF falls from 5.15 to 4.55 dB. The noise contribution is obtained from Cadence PSS/PNOISE analysis up to the IF mixer output. Fig. 14(c) summarizes the breakdown of noise contributions for each major circuit block. The input port, passive structures, first stage, second stage, RF mixer, and IF mixer contribute 35%, 25%, 22%, 8%, 6%, and 4%, respectively, to the 4.55 dB NF. Here, the RF mixer contribution refers to the combined noise from the transconductor devices  $M_3$  and  $M_4$  and the switching quad in Fig. 8. This noise breakdown indicates that the input passive structure (which includes  $L_G$ ,  $L_S$ , and the trifilar transformer) and the first stage in Fig. 8 together contribute 47% of the overall NF, demonstrating that the receiver front-end is the dominant contributor to the overall NF. The RF mixer output,  $V_{IF}$  in Fig. 8, is connected to I and Q IF mixers, each having AC-coupling capacitors ( $C_{ac1,2}$ ) inside. As shown in Fig. 15, the IF mixers (I and Q) are integrated within the IF Load

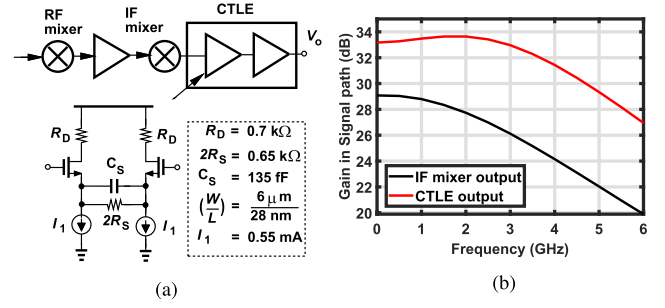


Fig. 16. (a) CTLE stages in the receiver chain and (b) BW extension in the receiver signal path.

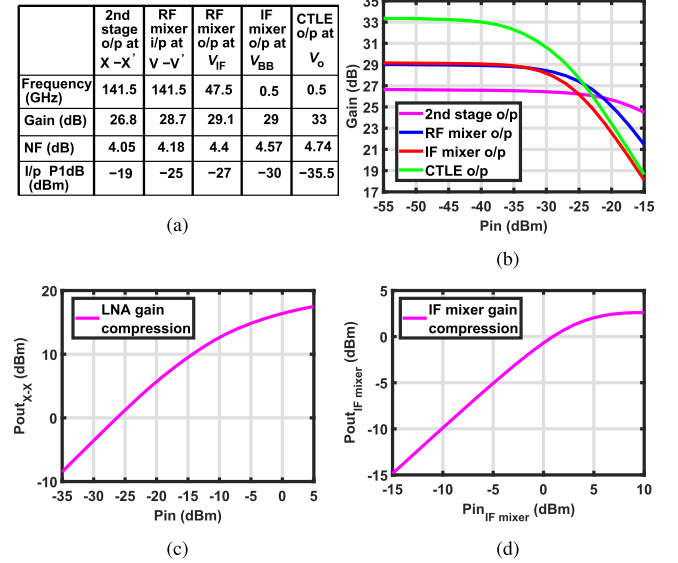


Fig. 17. (a) Gain, NF, and linearity summary in the receiver path, (b) linearity performance in the receiver signal path, (c) gain compression performance of the stand-alone LNA, and (d) gain compression performance of the stand-alone IF mixer.

inductor. This unique floor plan provides an easy-to-integrate interface between the PLLs and the mixers via the  $LO_1$  and  $LO_2$  lines in a near-symmetric manner, thereby contributing to a compact receiver with LO generation and an active area of 0.11 mm<sup>2</sup>, in comparison to [1], [2], [3], [4], and [10]. However, the  $LO_1$  and  $LO_2$  lines add additional loading to the prospective VCOs. For example, after implementing the  $LO_1$  line, the differential loading from the RF mixer increases to 8 fF from 3.75 fF. IF mixers consume 4.5 mA.

### E. Continuous-Time Linear Equalizers

As mentioned in Section IV-C, the RF mixer exhibits a one-sided 3-dB BW of 3 GHz at its output. To allow wider channels, we introduce a two-stage CTLE in the BB path [Fig. 16(a)] at the output of the IF mixer. With a total bias current of 4.4 mA, CTLEs provide a boost of 5 dB at 5 GHz offset, leading to the overall RX response shown in Fig. 16(b). We observe a (one-sided) BW of 3 GHz before the CTLE is added and 4.9 GHz after.

Fig. 17(a) summarizes the receiver's cascaded gain, NF, and linearity. These quantities are evaluated at the receiver chain's second-stage output (X-X'), the RF mixer switching-quad input (V-V'), the RF mixer output ( $V_{IF}$ ), the IF mixer output

( $V_{BB}$ ), and the CTLE output ( $V_0$ ). After the second stage, the receiver achieves a gain of 26.8 dB, and the NF is 4.05 dB [Fig. 10(a) and (b)], indicating that the front-end dominates the noise performance. The cumulative gain reaches 33 dB, while the NF increases only modestly from 4.05 to 4.55 dB and 4.74 dB at the IF mixer and CTLE output [Fig. 17(a)], respectively. Fig. 17(b) presents the gain-compression performance with an input P1dB of  $-35.5$  dBm. The compression characteristics deteriorate toward the BB output, as expected due to limited voltage headroom. Accordingly, the receiver's linearity is mainly limited by the IF/BB stages, particularly at the CTLE output where the signal swing is large due to the accumulated gain, as shown in Fig. 17(b) while the available voltage headroom is reduced. By contrast, the first and second stages of the receiver front-end in Fig. 8 are biased at 1 V at their drain nodes, providing sufficient voltage headroom for the signal swing. Additionally, the signal amplitude in the front-end stages remains relatively small. This is reflected in the linearity of the standalone LNA. As shown in Fig. 17(c), the LNA exhibits an input-referred P1dB of  $-19$  dBm. The simulated IIP3 of the LNA, obtained from a two-tone test, is  $-11$  dBm. Likewise, the standalone RF mixer switching quad has input-referred P1dB of 4.7 dBm and an IIP3 of 12.5 dBm. The situation changes in the IF mixer, where the available voltage swing is more constrained. The IF mixer shown in Fig. 13 has reduced voltage headroom compared with the RF front-end section because the complementary transconductor stage of the IF mixer uses stacked nMOS and pMOS devices operating from a 1-V supply. In addition, the switching quad of this IF mixer, composed of  $M_1$ ,  $M_2$ ,  $M_3$ , and  $M_4$  in Fig. 13, employs current sources ( $I_{X1}$  and  $I_{X2}$ ) at the source nodes of the switching quad devices and load resistors ( $R_1$  and  $R_2$ ) at their drain nodes, thereby reducing the allowable voltage swing. The input-referred P1dB of the stand-alone IF mixer is 1 dBm, as shown in Fig. 17(d). The simulated IIP3 of this IF mixer stage is 10 dBm. This trend continues in the CTLE, which experiences the largest signal swing in the receiver chain while also having limited available headroom due to the degeneration network ( $R_s$  and  $C_s$ ), bias current source ( $I_1$ ), and load resistance ( $R_D$ ) in the two-stage CTLE shown in Fig. 16(a), making it the dominant nonlinearity contributor in the receiver chain as shown in Fig. 17(b).

## V. LO GENERATION

The system architecture presented in Fig. 3 incorporates two PLLs for per-element LO synthesis. The power consumption of these blocks therefore proves critical. For this reason, and to eliminate the complexities associated with additional inductors, we prefer to avoid the use of buffers between the PLLs and the RX path. As discussed in Section IV-D, the compact floor plan of the proposed design allows both VCOs to directly drive their respective mixers without the need for a buffer.

### A. 47-GHz PLL

This PLL operates with  $f_{\text{REF}} = 250$  MHz and delivers quadrature phases at 47 GHz to the IF mixers. A frequency

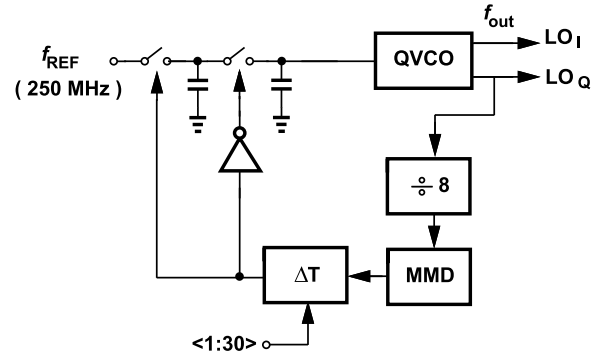


Fig. 18. PLL<sub>1</sub> architecture.

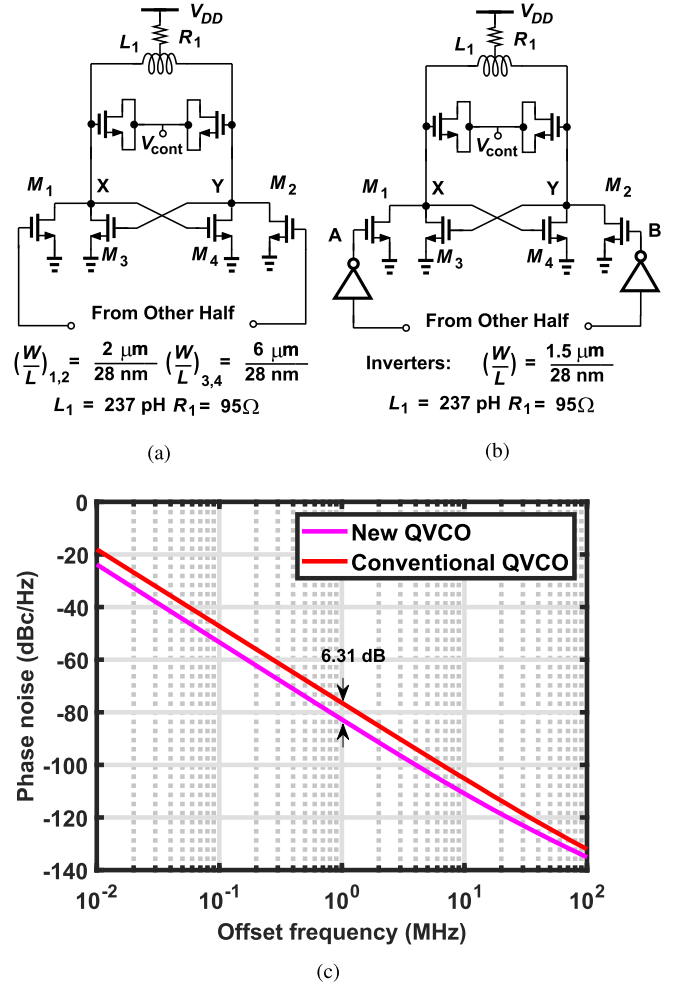


Fig. 19. (a) Conventional QVCO, (b) proposed QVCO, and (c) phase noise comparison.

multiplication factor of 15 is achieved using harmonic extraction techniques in [37], whereas this PLL exhibits a frequency multiplication factor close to 188. Shown in Fig. 18, the loop consists of a QVCO, three cascaded divide-by-two stages acting as a  $\div 8$  circuit, a multimodulus divider (MMD) [42], a programmable delay,  $\Delta T$ , and a sampling phase detector (PD) [42]. The differential Q lines feed the signal to the  $\div 8$  stage, and the I lines are loaded with the dummy devices for symmetry.

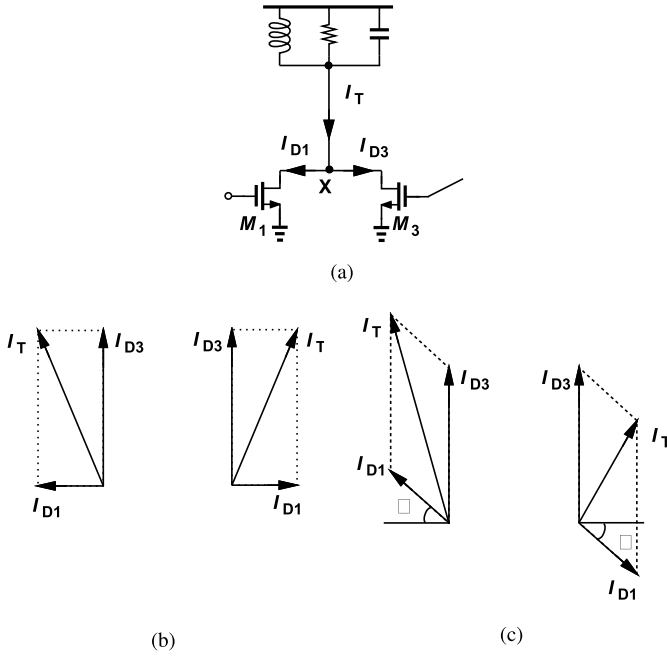


Fig. 20. (a) Proposed QVCO model for mode analysis, (b) first and second modes in conventional QVCO, and (c) first and second modes in proposed QVCO.

Generation of the 47-GHz I/Q phases of the LO proves difficult. Coupler-based I/Q generation is reported in [2], [6], [10], and [19]. The QVCO appears to be power-efficient compared to coupler-based I/Q phase generation, which requires buffer stages to achieve the required swing to drive the mixer [6]. Consider a conventional QVCO [36], half of which is shown in Fig. 19(a). This topology suffers from two issues: 1) the flicker noise of  $M_1$  and  $M_2$  modulates the injection strength and hence the output phase; and 2) the circuit exhibits two possible oscillation frequencies because it operates away from the resonance frequency of the tanks. To alleviate these issues, we insert inverters in the injection paths [Fig. 19(b)]. Thus, a delay of  $2.97 \text{ ps} \approx 51^\circ$  is introduced, shifting the oscillation frequency close to the tank resonance frequency, increasing signal swing, and reducing the flicker noise contributed by  $M_1$  and  $M_2$ .

Illustrated in Fig. 19(c), the simulation results reveal a phase noise drop of 6.31 dB in the entire flicker-dominated frequency range. The cost is 0.25 mW consumed by each inverter. It can be shown that, in this regime, the PN due to  $M_1$  and  $M_2$  is equal to [39]

$$S_{\phi n}(\Delta\omega) \propto \frac{K\alpha \cos^2 \phi}{V_0(1 + \alpha \sin \phi)^4} \cdot \frac{1}{\Delta\omega^3} \cdot \left(\frac{\omega_0}{2Q}\right)^2 \quad (6)$$

where  $K$  is the flicker noise constant of  $M_1$  and  $M_2$ ,  $\alpha = g_{m1}/g_{m3}$ ,  $\phi$  is the inverters' phase shift, and  $V_0$  is the amplitude. The voltage gain of the inverters is close to unity. In this work,  $\phi \approx 51^\circ$ , and  $\alpha = (1/3)$ , reducing the PN by nearly a factor of 6. The  $\phi$  varies from  $45^\circ$  in FF to  $58^\circ$  in SS process corner. Phase noise also improves by 7.63 dB in the SS and 5.57 dB in the FF corner.

Another remarkable property of the proposed QVCO is that it makes one oscillation frequency dominant, avoiding mode ambiguity. Shown in Fig. 20(a), the tank current,  $I_T$ , consists

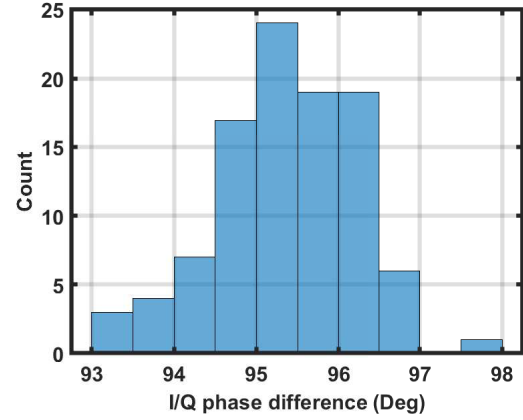


Fig. 21. Histogram of simulated I/Q phase difference.

of  $I_{D3}$  and  $I_{D1}$ . In the absence of the inverters, both phase relationships in Fig. 20(b) can occur, indicating the existence of two modes.

On the other hand, the inverters' phase shift,  $\phi$ , alters the results to those depicted in Fig. 20(c). Interestingly, the tank current is greater in one case than in the other, encouraging the circuit to oscillate only in that mode. The geometry of the phasor diagram in Fig. 20(c) also indicates that one mode has a higher amplitude than the other by a factor of  $(1 + \alpha \sin \phi)/(1 - \alpha \sin \phi)$ .

The quadrature accuracy is preserved for  $\phi$  ranging from  $0^\circ$  to  $90^\circ$  due to the symmetric injection between the two halves of QVCO. The I/Q phase difference of the proposed QVCO is simulated, and a histogram plot is depicted in Fig. 21 showing a systematic I/Q error close to  $5.5^\circ$  and a standard deviation of  $0.82^\circ$  due to random mismatches. The I/Q phase mismatch of up to  $5^\circ$  can provide adequate image rejection when the receiver SNR is on the order of 21.5 dB (Section VI-A). The systemic I/Q error arises from unavoidable interconnect asymmetry between the two QVCO cores and coupling between the inductors of the two cores.

With the proposed QVCO and a loop BW of 25 MHz ( $f_{\text{REF}}/10$ ) [36], PLL<sub>1</sub> exhibits an rms jitter of 118 fs<sub>rms</sub> and 120 fs<sub>rms</sub> from 10-kHz to 40-MHz and 100-MHz offset, respectively. The MMD with  $\Delta T$  network and sampling PD, frequency-divided-by-8 stage, and reference contribute 12%, 4%, and 11% of the phase noise, respectively, and the remaining phase noise is contributed by the new QVCO, which has 6.3 dB lower phase noise than a conventional one. Thus, phase-noise improvement in the QVCO proves useful for reducing jitter of PLL<sub>1</sub>. PLL<sub>1</sub> consumes 11 mA, and QVCO consumes 8.5 mA. PLL<sub>1</sub> shows competitive power consumption and jitter performance compared with other state-of-the-art PLLs operating near 47 GHz [41], [42], [43], [44], [45]

### B. LO Phase Shift for Beamforming

We wish to impart a phase shift with a range of  $180^\circ$  to the LO without the use of high-frequency phase shift networks. To this end, we propose the use of a programmable delay line,  $\Delta T$ , in the feedback path of PLL<sub>1</sub>. A time shift of  $\Delta T$  seconds translates to a phase shift of  $2\pi\Delta T f_{\text{out}} = \Delta\phi$  radians

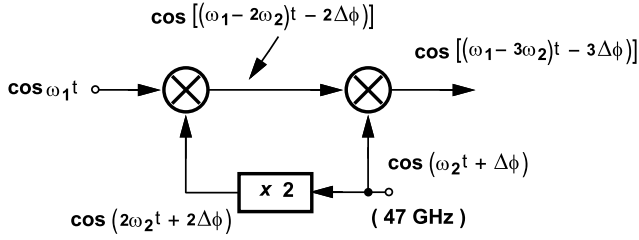


Fig. 22. LO phase shift mechanism.

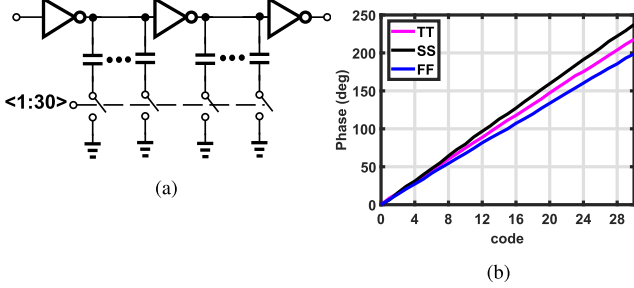
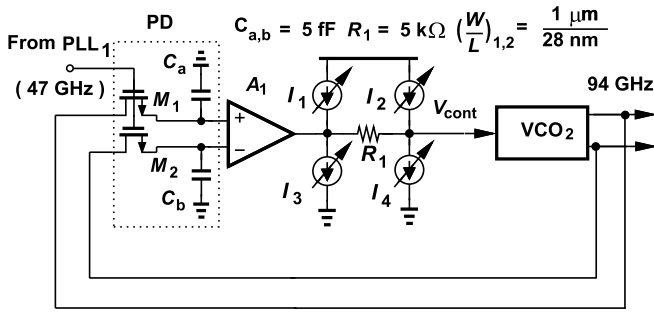


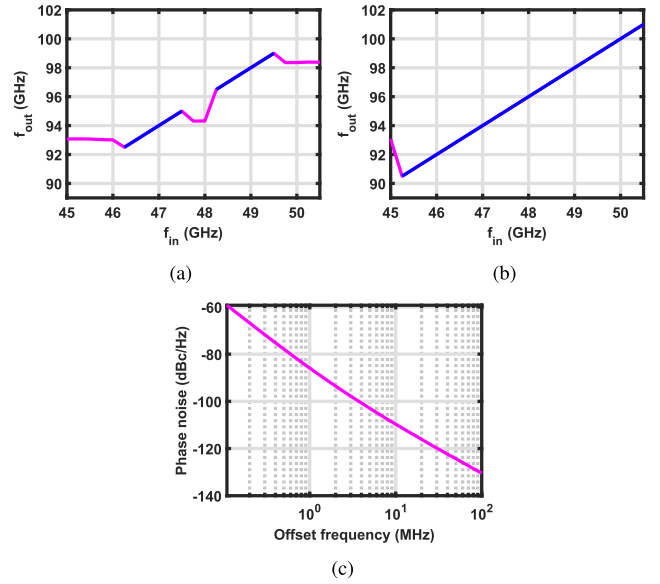
Fig. 23. (a) Implemented phase shift network based on a delay line and (b) phase shift simulation across corners.

Fig. 24. Proposed PLL<sub>2</sub> as subsampling frequency doubler.

at 47 GHz. For example, if  $\Delta T$  varies by 4.3 ps in steps of 145 fs, the output phase spans  $73^\circ$  with a resolution of  $2.45^\circ$  at 47 GHz. However, since this output also drives PLL<sub>2</sub>, as shown in Fig. 22, the total phase change in the downconverted signal is  $3\Delta\phi$ , corresponding to approximately  $219^\circ$  with a resolution of  $7.35^\circ$  at 141 GHz. Another  $180^\circ$  of phase shift can be realized by a detour through an inverter. Shown in Fig. 23(a), the variable-delay line consists of three inverters and 30 switched capacitors, and Fig. 23(b) plots the simulated absolute phase shift across corners. It consumes 0.2 mW and incurs 16 fs of rms jitter. The proposed delay-line-based approach applies phase shift at a low frequency (250 MHz) without causing LO amplitude variation, whereas [15], [47], and [48] perform phase shift at intermediate frequencies on the order of 15 GHz, and the next-stage buffer removes any LO amplitude variation caused by the phase shifter.

### C. 94-GHz PLL

As indicated in the architecture of Fig. 3, this PLL serves as a frequency doubler based on a subsampling topology. Other state-of-the-art frequency multipliers rely on harmonic generation from device nonidealities, resulting in low-power efficiency [49], [50]. The injection-locked oscillator consumes

Fig. 25. (a) Lock range for subsampling PLL without proposed technique, (b) lock range for proposed subsampling PLL, and (c) simulated phase noise of VCO<sub>2</sub>.

low power but faces a trade-off between tuning range and output LO swing [51], [52]. The subsampling topologies reported in [53] and [54] suffer from a narrow lock range of less than 2.5%. The proposed PLL<sub>2</sub> extends this lock range to 10%. Shown in Fig. 24, the proposed topology applies the outputs of the VCO (VCO<sub>2</sub>) to the PD and converts the differential result to a single-ended voltage. The proposed network consisting of  $I_1, \dots, I_4$  and  $R_1$  provides a DC level shift to widen the lock range and is discussed below. The VCO<sub>2</sub> includes: 1) a single switched-capacitor and 2) an nMOS varactor for a  $K_{VCO}$  of 5 GHz/V, to provide a total 10 GHz of tuning range. The  $C_{max}$  to  $C_{min}$  range of the varactor devices ( $2.4 \mu\text{m}/200 \text{ nm}$ ) is from 10.21 to 2.57 fF with a minimum quality factor of 5. VCO<sub>2</sub> also faces loading from the RF mixer with lines driving to it, and sampling capacitors through sampling switches.

The use of a subsampling PLL as a frequency doubler offers a number of advantages over other doubling techniques in the integrated receiver [1], [2], [6], [12], [17], [19]. First, it generates large differential outputs that can directly drive the RF mixer. Second, it draws only 6 mW, far less than typical doublers in this frequency range. Nevertheless, as suggested by [54], and the simulated input-output frequency plot of Fig. 25(a), this loop suffers from a narrow, discontinuous lock range as it locks near  $V_{DD}/2$  for both ON and OFF state of the switched-capacitor of VCO<sub>2</sub>. This is because, as the output voltage of  $A_1$  in Fig. 24 moves away from  $V_{DD}/2$  toward lower or higher values, this amplifier's gain drops considerably. We must thus minimize this voltage range while still maximizing the available range for  $V_{cont}$ . This is accomplished by the DC level shift network where the voltage summation of the output of  $A_1$  and the voltage drop across  $R_1$  resistance constitutes  $V_{cont}$ : to deliver low voltage levels to  $V_{cont}$ , we enable  $I_1$  and  $I_4$ , producing a maximum drop of  $I_1 R_1 = (= I_4 R_1)$  300 mV across  $R_1$  in steps of 30 mV. Similarly,  $I_2$  and  $I_3$  are activated when a high  $V_{cont}$  near to the  $V_{DD}$  value is necessary. The  $I_1$ ,

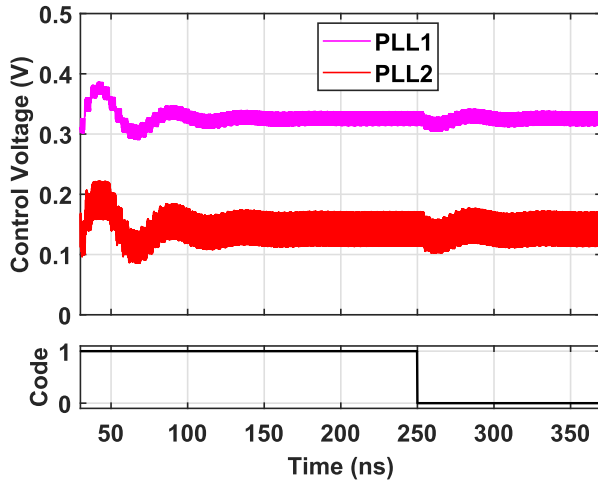


Fig. 26. Transient settling response of PLL<sub>1</sub> and PLL<sub>2</sub> following the phase shift control (code) transition.

|                          | Receiver chain |              |             |                         |          |      | LO path          |                  |   |   |
|--------------------------|----------------|--------------|-------------|-------------------------|----------|------|------------------|------------------|---|---|
|                          | First stage    | Second stage | Third stage | RF mixer switching Quad | IF mixer | CTLE | PLL <sub>1</sub> | PLL <sub>2</sub> |   |   |
| Current consumption (mA) | 3.6            | 5.2          | 4           | 1.1                     | 4.5      | 4.4  | 8.5              | 2.5              | 5 | 1 |

Fig. 27. Current consumption breakdown of the proposed receiver.

$I_2$ ,  $I_3$ , and  $I_4$  current sources are programmable up to 60  $\mu$ A in steps of 6  $\mu$ A. The headroom constraints at the output of  $A_1$  are therefore relaxed by  $2I_1R_1 = 600$  mV, leading to the results of the continuous lock range depicted in Fig. 25(b).

The open-loop VCO has a phase noise of -109 dBc/Hz at 10 MHz offset in Fig. 25(c) and consumes 5 mW of power. By virtue of a loop BW of 250 MHz, PLL<sub>2</sub> heavily suppresses the phase noise of VCO<sub>2</sub> and produces a jitter of 40 fs<sub>rms</sub> from 10 kHz to 40 MHz. Hence, the phase noise/jitter contribution from the PLL<sub>1</sub> dominates in the LO path.

Both PLLs in the cascaded LO generation architecture of Fig. 3 are evaluated using transient simulations. Because the phase shift is implemented within the PLL<sub>1</sub> feedback loop, the beam-switching speed is governed by the PLL settling dynamics. Therefore, the control voltages of PLL<sub>1</sub> and PLL<sub>2</sub> are plotted in Fig. 26 to illustrate the transient behavior of the cascaded PLL. The phase shift control (Code), consisting of all 30 bits as shown in Fig. 18, changes at 250 ns, and both PLL control voltages settle by approximately 310 ns, corresponding to a beam-switching settling time of about 60 ns for the cascaded PLL-based phase-shifting path. The small ripple observed on the PLL control voltages arises from second-order harmonic components generated by the nMOS varactors of the respective VCOs used for frequency tuning in PLL<sub>1</sub> and PLL<sub>2</sub> [54]. These harmonics do not affect the PLL settling behavior or overall PLL performance.

Fig. 27 summarizes current consumption for the major circuit blocks of the complete integrated receiver. It shows that 17 mW is consumed by the LO path, and the remaining approximately 23 mW is consumed by the receiver signal chain. Section II-C discusses how LO generation and distribution constitute a major bottleneck for power consumption in

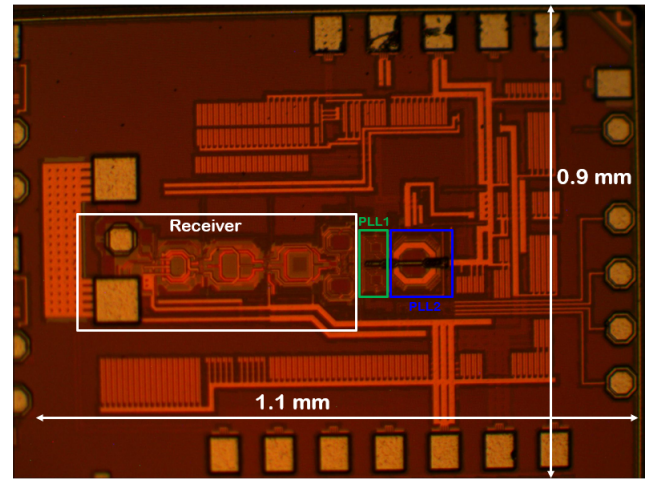


Fig. 28. Chip photograph.

the D-band systems reported in the state-of-the-art literature. In this work, a significant portion of the power savings comes from the proposed LO-generation architecture, which uses the cascaded PLL with an integrated LO phase shift and operates with only a 250 MHz reference. Compared to other D-band receiver and beamforming architectures that distribute the high-frequency LO signal and rely on passive frequency multipliers and power-hungry buffer stages, the proposed approach substantially reduces LO power and LO distribution losses while increasing system compactness.

The trade-off is the additional complexity of the cascaded PLL-based LO generation, which requires careful phase-noise optimization, improvement schemes, and a wide frequency tuning range, perhaps necessitating additional circuit techniques, as discussed in Sections V-A and V-C. In addition, the independent PLLs for per-element LO beamforming require initial phase adjustment, as discussed in Section II-C. The beam switching speed is also determined by the cascaded PLL loop dynamics, thereby imposing an inherent beam-switching timing constraint. Nevertheless, the proposed architecture achieves substantially lower LO-path power consumption than conventional LO-distribution approaches while maintaining receiver performance.

## VI. EXPERIMENTAL RESULTS

The system in Fig. 3 has been fabricated in TSMC's 28-nm CMOS technology. Fig. 28 shows the die photograph. The power breakdown is as follows: 14 mW in the LNA and RF mixer, 9 mW in the IF mixers and BB chains, 11 mW in PLL<sub>1</sub>, and 6 mW in PLL<sub>2</sub>.

### A. RF Signal Path Performance

The signal path performance has been characterized in a setup where Virginia Diodes' KT-8257DV08 provides a 140-GHz input through a variable attenuator and a waveguide to the RX as shown in Fig. 29(a). Before connection to the chip, the waveguide output is measured by a VDI Erikson power meter. Figs. 30 and 31 plots the measured signal path characteristics. The gain displayed in Fig. 30(a) corresponds to the case of a fixed LO frequency,  $f_{LO} = f_{LO1} + f_{LO2}$ ,

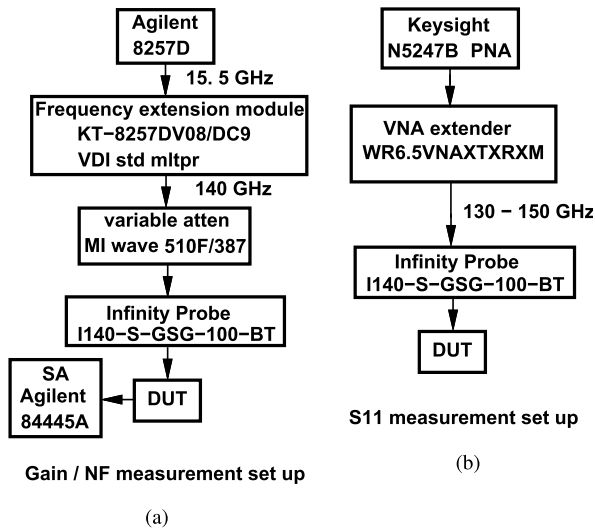


Fig. 29. (a) Gain and NF measurement setup and (b) S11 measurement setup.

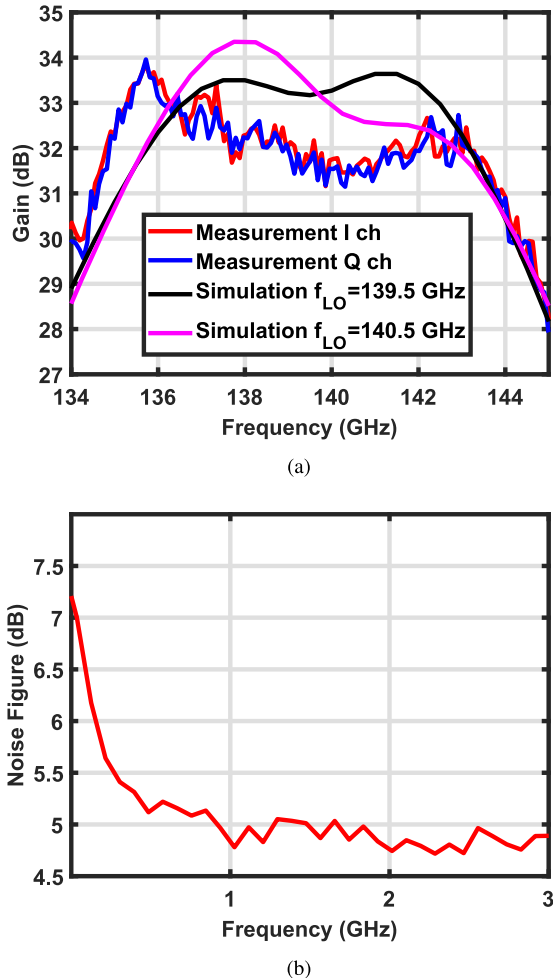


Fig. 30. (a) Conversion gain across channel and (b) NF DSB across channel at BB frequency.

revealing a channel BW of 10 GHz at 140 GHz. Simulation with two  $f_{LO}$  frequencies shows unequal sideband gain if  $f_{LO}$  is not chosen at the center of the BW (139.5 GHz). Based on this, the center frequency of the fabricated receiver is approximately 138.5–139 GHz.

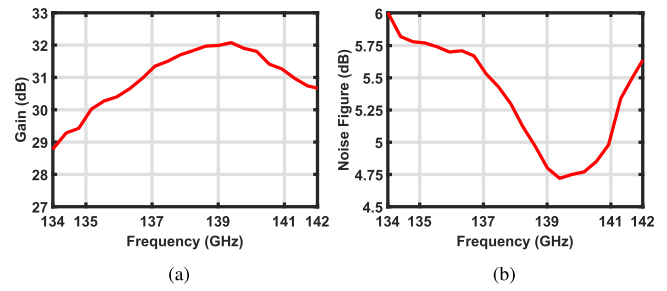


Fig. 31. (a) Conversion gain across RF BW and (b) NF DSB across RF BW.

Fig. 31(a) is obtained for a fixed BB frequency,  $f_{BB}$ , of 1 GHz, representing the RF BW.

Shown in Figs. 30(b) and 31(b) are, respectively, the NFs across a channel (with a fixed  $f_{LO}$  of 140 GHz), and across the RF BW (with a fixed  $f_{BB}$  of 1 GHz). The NF varies between 4.75 and 6 dB, the lowest reported for D-band receivers. The measured gain and NF curves exhibit small, frequency-dependent spikes, with less than 0.25 dB for NF. Similar behavior is also observed in prior D-band measurements [6], [8], [9], [11], [54]. Since the measured S11 at the receiver input is well behaved and consistent with simulation, input reflection is unlikely to be the primary source of these spikes. They are therefore likely associated with residual measurement-setup effects, including those at the probe and receiver-chip interfaces, rather than with the intrinsic receiver behavior. The NF is measured in two steps commonly adopted in gain method [1], [3], [9], [54].

- 1) The RX output noise floor is displayed on a low-noise spectrum analyzer (Agilent E4445A), whose spot noise floor is approximately  $-130$  dBm with a resolution BW (RBW) of 10 kHz and with a  $50\text{-}\Omega$  input termination before connecting to the chip. After RBW normalization, this corresponds to a noise spectral density of  $-130$  dBm  $-40$  dB =  $-170$  dBm/Hz, where 40 dB accounts for the 10 kHz RBW. After connecting the spectrum analyzer to the receiver output, the displayed spot noise power on the spectrum analyzer is more than 25 dB above the analyzer spot noise floor; thus, the spectrum analyzer does not limit the NF measurement accuracy. The receiver output noise floor is obtained by accounting for the BB loss following the chip.
- 2) In dB calculations, the receiver output noise spectral density is obtained from the receiver output noise floor after RBW normalization, and the input-referred noise spectral density is then obtained by subtracting the measured gain from the receiver output noise spectral density [9]. This input-referred noise spectral density is then compared with  $-174$  dBm/Hz to obtain SSB NF [9]. Equivalently, in the linear domain, the gain-subtraction step in the dB calculation corresponds to the following operation: the RX output noise power number is divided by the measured gain and compared with  $50\text{ }\Omega$  to obtain the SSB NF, where the “RX output noise power” term refers to the receiver output noise spectral density, and the  $50\text{ }\Omega$  reference corresponds to the room-temperature thermal-noise density of  $-174$  dBm/Hz [9]. DSB NF is

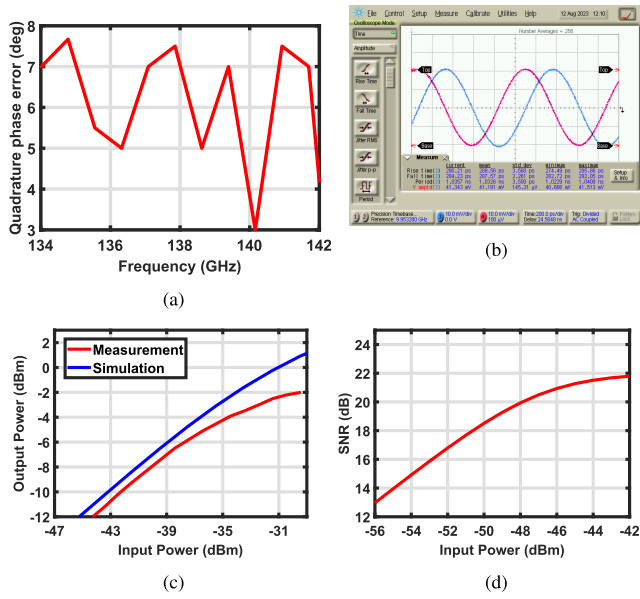


Fig. 32. (a) Quadrature error across frequency, (b) time-domain BB waveform of I and Q channels, (c) output P1dB compression point, and (d) receiver SNR with input signal power.

3 dB lower than SSB NF [3], [9]. The same setup shown in Fig. 29(a) is used for both gain and NF measurements. In the NF measurement, Virginia Diodes' frequency extension module (KT-8257DV08) is turned off, and the remainder of the measurement setup remains unchanged, thereby maintaining a matched input termination at the receiver input [54]. As the receiver gain is measured from the same setup in Fig. 29(a), the same BB loss is de-embedded in both the gain and NF measurements. Power (rms) averaging is used to measure the noise power spectral density.

Fig. 32(a) plots the I/Q phase error of the RX BB outputs for a fixed BB frequency of 1 GHz, suggesting a maximum value of  $7.2^\circ$  and an average of  $5.5^\circ$  across the frequency due to the LO path, and Fig. 32(b) displays the time-domain results for the BB output at 1 GHz. Systematic I/Q error can be externally calibrated. Measurement shows close agreement with simulation (Section V-A). Fig. 32(c) shows the input–output characteristic of the RX at 1 GHz offset and an output 1-dB compression point of  $-4$  dBm, which closely matches the simulation.

The calculated SNR is plotted in Fig. 32(d) when imperfections from the receiver path and LO jitter, discussed in Section VI-B, are considered. For the receiver signal path, with a 5 dB average NF, the total equivalent input noise power over a 10 GHz channel BW is  $-174$  dBm/Hz +  $10\log(\text{BW})$  + NF =  $-69$  dBm. If we consider an input signal power of  $-44$  dBm (8 dB back-off from input compression), the SNR from the signal path is 25 dB. For LO phase noise, the measured IPN is close to  $-22$  dBc (Section VI-B). Thus, the total SNR becomes LO jitter-dominated at 21.5 dB when the input power reaches  $-44$  dBm. The SNR is estimated to be 15.8 dB in [6] over an 18 GHz BW. The calculated SNR, therefore, captures the dominant receiver-side impairments relevant to D-band links because it is derived from measured

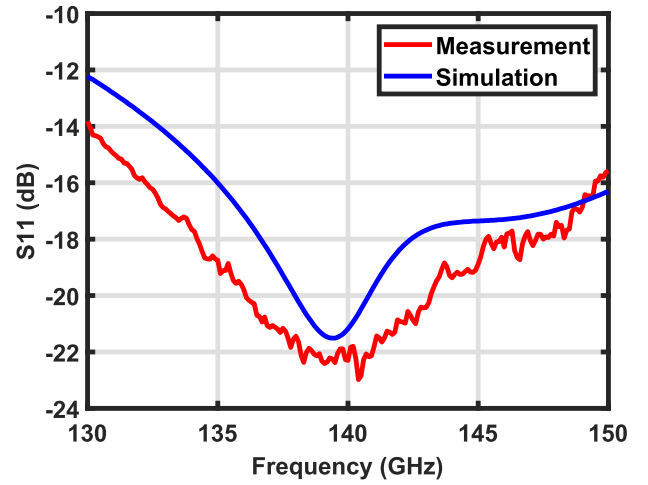


Fig. 33. Measured S11.

NF and jitter performance. Thus, this estimated SNR provides a meaningful system-level benchmark based on measured NF and jitter characteristics. The calculated SNR is comparable to that reported for state-of-the-art D-band communication systems [6]. Together with low-power consumption, operation from a low-frequency reference, high LO/RX integration, the applicability of LO-phase shifting, and a fully integrated compact system, these results demonstrate the suitability of the proposed receiver for highly integrated D-band microwave systems.

The S11 is measured using Keysight PNA (N5247B) and VDI VNA extender module (WR6.5VNAXTXRXM) as shown in Fig. 29(b). Before the measurement, a one-port short-open-load calibration, part of SOLT [55], is performed using an impedance substrate compatible with the probe. The S11 is better than  $-12$  dB. The close matching between the simulation and measurement shows the reasonable accuracy of the EM modeling and simulation conditions at 140 GHz. In the measurement, an input power well below the first stage compression is assured through built-in attenuation in the WR6.5VNAXTXRXM module. This also ensures that the ESD diodes remains off and does not affect the measurement. Fig. 33 plots the measured S11 of the fabricated receiver chip.

The stability factor shown in Fig. 10(d) is obtained from the SP simulation of the receiver front-end up to node X-X' in Fig. 8, where the circuit is treated as a linear two-port network for small-signal front-end stability analysis. The Rollet stability factor is a commonly reported metric for front-end modules in the literature. For the complete receiver, however, the Rollet stability factor is not directly applicable because the RF and IF mixer stages operate in a periodically time-varying manner; thus, the receiver cannot be strictly represented as a linear two-port network. Therefore, the K-factor of the complete down-conversion receiver does not provide the same linear two-port stability interpretation as it does for the front-end. Instead, the stability of the overall receiver is verified through measurements of gain, NF, and S11, with no spurious or unwanted tones observed. Furthermore, no oscillatory behavior is observed in either the measurements or the time-domain transient simulations.

TABLE I  
PERFORMANCE SUMMARY AND COMPARISON TO PRIOR ART

|                                     | This work                   | Affi<br>TMTT' 25 [1]   | Yun<br>TMTT' 25 [2]    | Ibrahim<br>TMTT' 24 [3] | Wang<br>RFIC' 21 [4]   | Guan<br>JSCC' 24 [6]    | Chou<br>ESSCIRC' 22 [9]         | Dong<br>RFIC' 23 [10]  | Karakuzulu<br>JSSC' 23 [11] | Bo<br>TMTT' 24 [18] |
|-------------------------------------|-----------------------------|------------------------|------------------------|-------------------------|------------------------|-------------------------|---------------------------------|------------------------|-----------------------------|---------------------|
| Tech. (nm)                          | 28-nm CMOS                  | 45-nm SOI              | 40-nm CMOS             | 130-nm SiGe<br>BiCMOS   | 22-nm FDSOI            | 28-nm CMOS              | 28-nm CMOS                      | 22-nm FDSOI            | 130-nm SiGe<br>BiCMOS       | GaAs<br>Inp HBT     |
| Frequency (GHz)                     | 140                         | 131–173                | 140                    | 140                     | 137–156                | 141                     | 135                             | 140                    | 110–170                     | 194.5–234.5         |
| Channel BW (GHz)                    | 10                          | 8                      | N/A                    | 10                      | 14                     | 18                      | 10                              | 4–8                    | 60                          | 40                  |
| 3 dB RF BW (GHz)                    | 10                          | 42                     | 15                     | 40                      | 19                     | N/A                     | N/A                             | 12                     | N/A                         | N/A                 |
| Number of Elements                  | 1                           | 1                      | 1                      | 1                       | 1                      | 1                       | 4                               | 4                      | 4                           | 4                   |
| Number of Channels                  | 1                           | 2                      | 1                      | 1                       | 2                      | 1                       | 1                               | 1                      | 1                           | 1                   |
| Beamforming<br>Architecture         | Low-Frequency<br>Delay Line | No<br>Beamforming      | No<br>Beamforming      | No<br>Beamforming       | No<br>Beamforming      | No<br>Beamforming       | External Digital<br>Beamforming | RF<br>Beamforming      | RF<br>Beamforming           | LO<br>Beamforming   |
| Core Area (mm <sup>2</sup> )        | 0.11 per<br>RX element      | 0.38 per<br>RX channel | 0.67 per<br>RX element | 0.24 per<br>RX element  | 1.55 per<br>RX channel | 5.76 per<br>TRX element | 4 per<br>TRX element            | 1.75 per<br>RX element | 5.64 per<br>TRX element     | N/A                 |
| NF (dB)                             | 4.7                         | 5.7                    | 7.2                    | 8.2                     | 9                      | 9.3                     | 7.8                             | 7.5                    | 10.08                       | 7.5                 |
| Gain (dB)                           | 32                          | 24.4                   | 29.7                   | 12.7                    | 27                     | 30                      | 58                              | 32                     | 22                          | 14                  |
| IP1dB (dBm)                         | −35                         | −28                    | −29                    | −3.5                    | −29                    | −37                     | N/A                             | −45                    | −30                         | −10                 |
| On-Chip I/Q Gen                     | Yes                         | No                     | Yes                    | Yes                     | Yes                    | Yes                     | Yes                             | Yes                    | Yes                         | No                  |
| Power per element<br>/ Channel (mW) | 40                          | 148                    | 145                    | 158                     | 197                    | 485                     | 98                              | 120                    | 487                         | 675                 |
| Phase Resolution<br>(deg)           | 7                           | Not applicable         | Not applicable         | Not applicable          | Not applicable         | Not applicable          | Not applicable                  | 3                      | 22.5                        | > 6                 |
| REF Frequency                       | 250 MHz                     | 17–23 GHz              | 72 GHz                 | 140 GHz                 | 17–19.5 GHz            | 40 MHz                  | 2.82 GHz                        | 14.4–15.5 GHz          | 35 GHz                      | 13.5 GHz            |
| Integrated Jitter                   | 130 fs                      | N/A                    | N/A                    | N/A                     | N/A                    | > 700 fs                | N/A                             | N/A                    | N/A                         | N/A                 |

• Minimum noise figure across the bands.

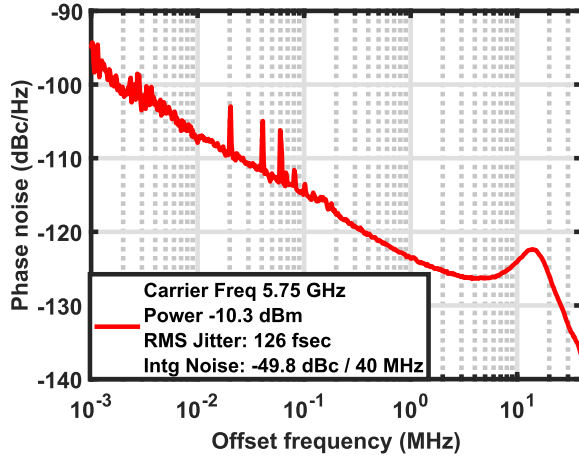


Fig. 34. Jitter performance of  $PLL_1$  after  $\div 8$  stage for output frequency of 46 GHz.

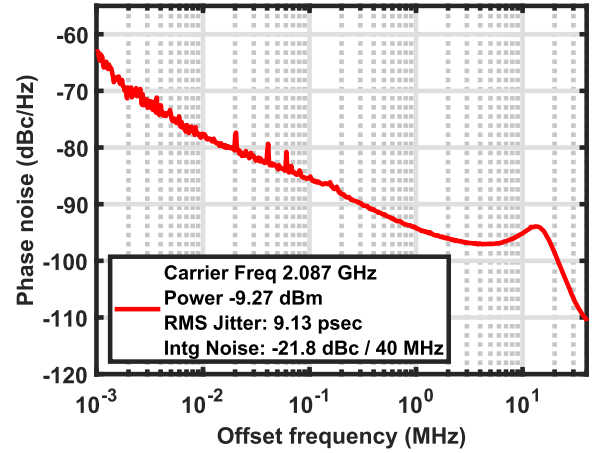


Fig. 35. Combined jitter of  $PLL_1$  and  $PLL_2$  at BB output when  $f_{LO1} = 46$  GHz and  $f_{LO2} = 92$  GHz.

### B. LO Path Performance

The performance of  $PLL_1$  in Fig. 18 is monitored at the output of the  $\div 8$  stage. The loop exhibits a lock range of 4.5 GHz, limited by the VCO continuous tuning range. Displayed in Fig. 34, the phase noise profile yields an rms jitter of 126 fs from 10 kHz to 40 MHz that shows close agreement with the simulation. It is worth mentioning that a 250 MHz crystal reference from Crystek's CRBSCS-01-250.000 is used as  $f_{REF}$  to  $PLL_1$ .

With no direct access to  $PLL_2$  in Fig. 3, we simply measure the phase noise at a 2-GHz BB frequency while the RX senses and downconverts a 140-GHz input. This observation provides the phase noise in Fig. 35 as a summation of those of  $PLL_1$  and  $PLL_2$ . Integrated from 10 kHz to 40 MHz, this profile produces a jitter of 9.1 ps for a 2-GHz carrier in Fig. 35, and hence 130 fs at 140 GHz because jitter is inversely proportional to frequency. Assuming uncorrelated phase noise components for  $PLL_1$  and  $PLL_2$ , we estimate the latter's contribution to

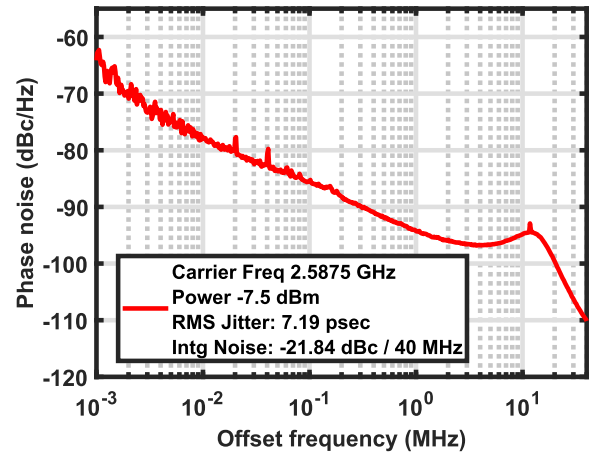


Fig. 36. Combined jitter of  $PLL_1$  and  $PLL_2$  at BB output when  $f_{LO1} = 48$  GHz and  $f_{LO2} = 96$  GHz.

be 32 fs. Fig. 36 show a similar jitter performance when

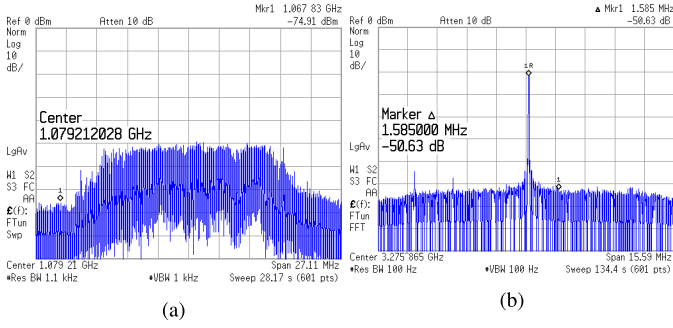


Fig. 37. Receiver output spectrum with (a) unlock and (b) lock state of  $PLL_2$ .

measured for another frequency ( $f_{LO1} = 48$  GHz, and  $f_{LO2} = 96$  GHz). The lock range of  $PLL_2$  is 9 GHz.

No pulling between the two PLLs has been observed, nor any false lock in the subsampling loop. The output frequency of  $PLL_2$  in Fig. 24 can be an integer multiple of the reference frequency of the order of 47 GHz. As the output frequency of  $VCO_2$  in  $PLL_2$  is between 90 and 100 GHz, this ensures the output frequency of  $PLL_2$  will be 94 GHz if a 47 GHz reference is applied. Fig. 37 shows the BB output spectrum for unlocked and locked states of  $PLL_2$ .

### C. Phase Shift Network Performance

The programmable phase shift,  $\Delta T$ , shown in Fig. 3 and realized as depicted in Fig. 23(a) for beamforming is characterized as follows. The phase is a relative quantity; thus, it needs to be measured relative to a reference. As shown in Fig. 38(a), two RX chips,  $DUT_1$  and  $DUT_2$ , are mounted on the same printed-circuit board (PCB) with the same  $f_{REF}$  applied to both the DUTs and a signal-ground-signal footprint ( $DUT_0$ ) is split and bonded to each RX input. A probe is then landed on the PCB to apply the 140-GHz signal. The phase shift setting for  $DUT_1$  is fixed while that of  $DUT_2$  is varied. The receiver outputs are compared using an oscilloscope (Agilent 86117A). Thus, the phase difference between the BB outputs of the two receivers can be measured with high accuracy. It is ensured that both receiver outputs have nearly identical swings for the phase shift measurement. The photograph of the phase shift measurement is shown in Fig. 38(b). Any mismatch between the two measurement paths, including the PCB and wirebond interconnects, can introduce amplitude and phase differences. Additional electromagnetic evaluation of the PCB, wirebond, and chip-interface paths was performed to assess path mismatch, indicating limited amplitude imbalance between the two measurement paths at the desired frequency. The nearly identical output amplitudes measured at the receiver outputs indicate that both receivers are excited under closely matched conditions. Because the phase shift of  $DUT_2$  is measured relative to the reference  $DUT_1$ , whose phase shift control code is fixed, any residual path mismatch that results in phase imbalance appears as a fixed phase offset between the two measurement paths. The phase difference between the two receiver outputs can be expressed as

$$\Delta\phi_{out} = \Delta\phi_{RX} + \phi_{offset} \quad (7)$$

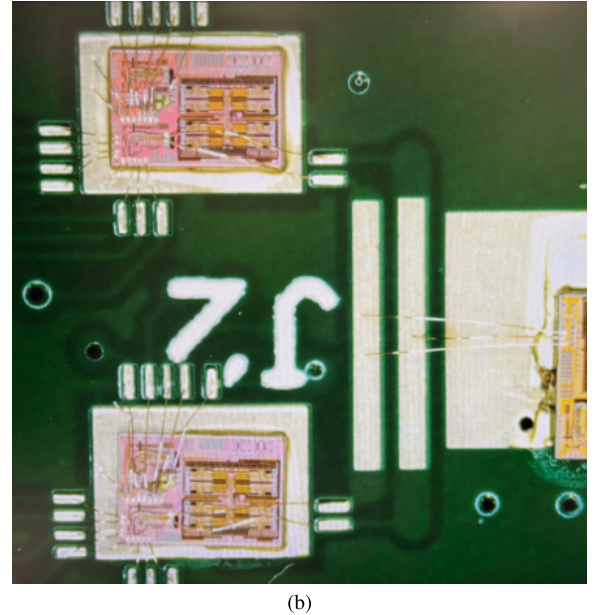
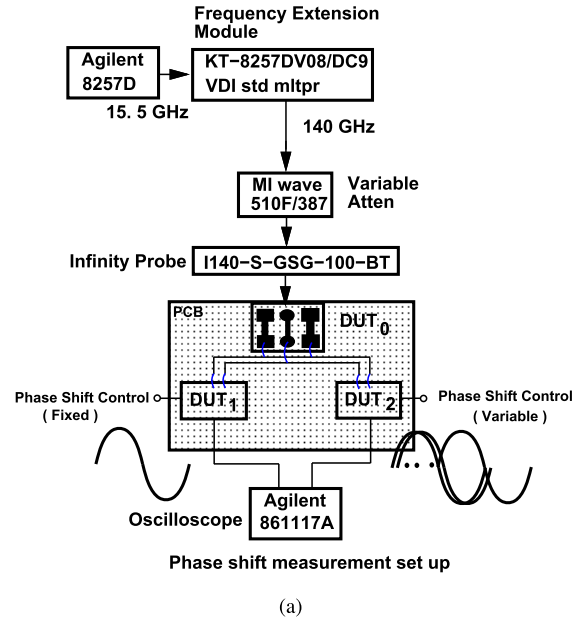


Fig. 38. (a) Receiver phase shift measurement setup and (b) photograph of phase shift measurement setup.

where  $\Delta\phi_{RX}$  denotes the phase difference generated by the receiver and  $\phi_{offset}$  represents the constant phase offset between the two measurement paths. Because  $\phi_{offset}$  is independent of the receiver's phase shift control code, it does not affect the measured phase shift range. Consequently, the reported phase shift characteristic reflects the receiver-generated relative phase shift rather than the fixed offset between the measurement paths. This arrangement is intended solely to measure the phase shift between two chips. Shown in Fig. 39(a) is the phase shift versus the input code for a 141-GHz input, covering more than  $200^\circ$  with an average resolution of  $7^\circ$  and rms error of  $2^\circ$ . The INL is plotted in Fig. 39(b), reaching from 0 to 1 LSB. Fig. 39(c) plots the DNL which stays within  $\pm 0.5$  LSB. Fig. 39(d) plots the phase shift versus the RX input frequency for code values ranging up to 30. The gain variation with phase shift is negligible,

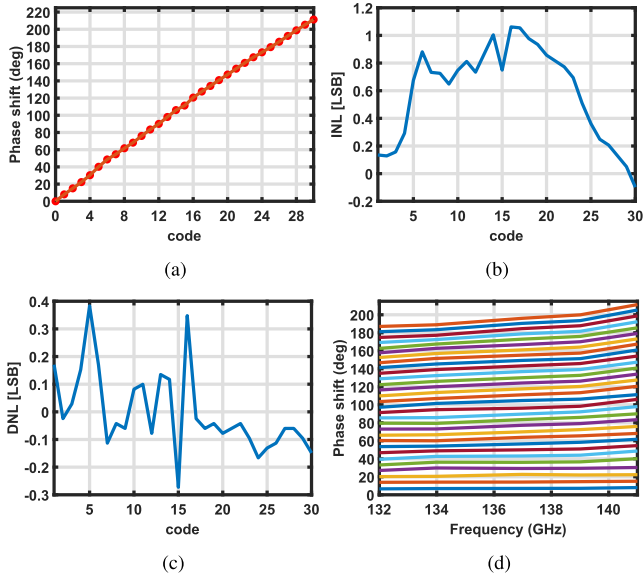


Fig. 39. (a) Phase shift at 141 GHz, (b) INL, (c) DNL, and (d) phase shift in all the frequency.

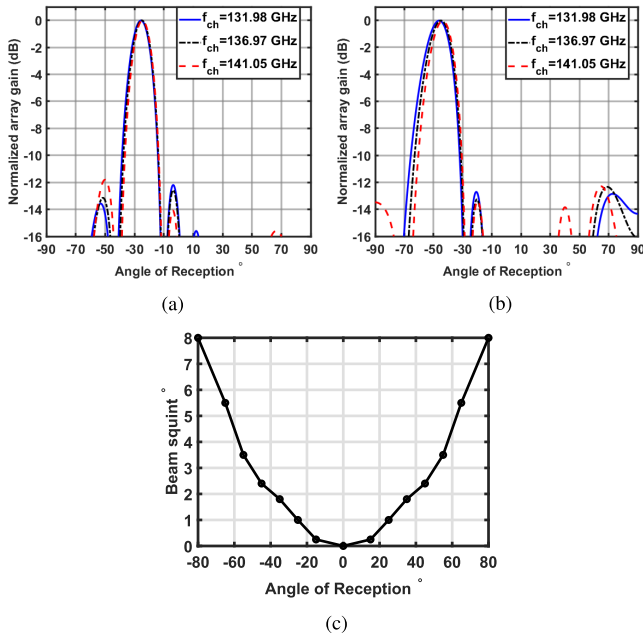


Fig. 40. (a) Synthesized beam pattern for 25°, (b) 45° beam steering angle, and (c) beam squint with angle of reception.

as expected. To evaluate the effect of the LO phase shift at 140 GHz over nearly 10 GHz of channel BW discussed in Section II-B, the data from Fig. 39(d) are used to plot the beam patterns in Fig. 40(a) and (b), assuming an eight-element array [17], with  $\lambda/2$  spacing. The beam squinting angle ([57], [58], [59]) is 1° and up to 2.5° for 25° and 45° beam steering angles. Fig. 40(c) shows the effect of beam squinting for different angle of reception.

Table I compares the proposed receiver performance with other state-of-the-art prototypes.

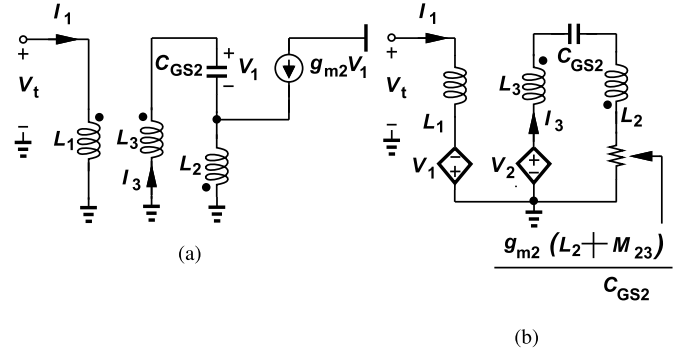


Fig. 41. (a) Small signal model for input impedance and (b) simplified model for input impedance of second stage.

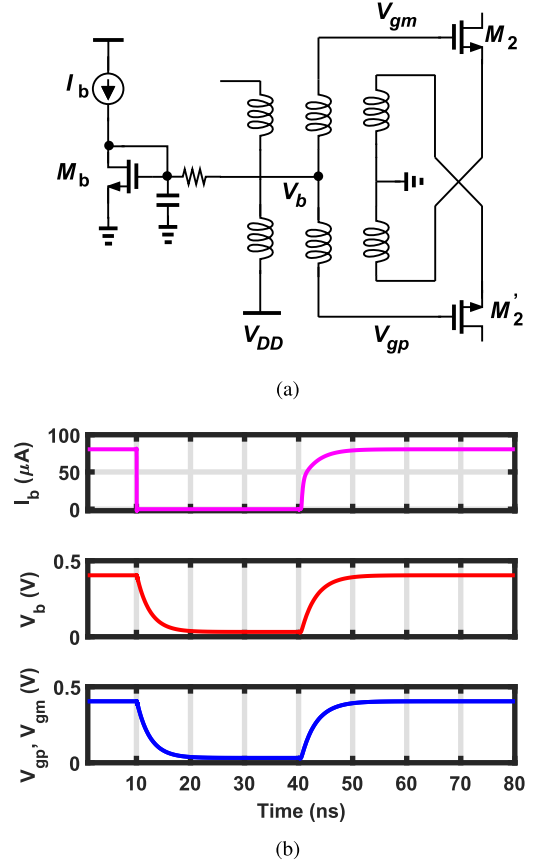


Fig. 42. (a) Biasing strategy of the receiver second stage and (b) transient bias settling.

## VII. CONCLUSION

This article presents several concepts that improve the performance of 140-GHz receivers. A new LNA topology, Gain and NF improvement techniques in the IF mixer, a wide-range subsampling PLL, a new QVCO, and a new phase shift method for beamforming are described in detail. The measurement validates the presented theory and analysis of the proposed receiver with integrated LO generation with phase shift in the LO path at 140 GHz.

## APPENDIX A

As a first step, the small-signal model for the input impedance of second stage half circuit is shown in Fig. 41(a).

A small signal test voltage,  $V_t$ , is applied at the input, and the currents on the primary side,  $L_1$ , and on the  $L_3$  of the secondary side are denoted by  $I_1$  and  $I_3$ , respectively. We identify that  $I_3$  flows through  $C_{GS2}$ , creating a voltage drop of  $V_1 = I_3/j\omega C_{GS2}$ . As a result, the device  $M_2$  generates current  $g_{m2}V_1 = g_{m2}I_3/j\omega C_{GS2}$ . When this current flows through  $L_2$ , it produces a voltage drop of  $((L_2 + M_{23})g_{m2}I_3)/C_{GS2}$ . Thus, this can be modeled as a resistance of  $R_3 = ((L_2 + M_{23})g_{m2})/C_{GS2}$ .

After modeling the resistance in the previous step, the simplified model for input impedance is shown in Fig. 41(b), where the dependent voltage sources,  $V_1$  and  $V_2$  are due to the magnetic coupling between  $L_1$  and  $L_2$  and between  $L_1$  and  $L_3$

$$V_1 = \frac{g_{m2}M_{12}I_3}{C_{GS2}} + j\omega(M_{12} + M_{13})I_3 \quad (8)$$

$$V_2 = j\omega(M_{12} + M_{13})I_1. \quad (9)$$

We recognize that the secondary side in Fig. 41(b) consist of  $L_2$ ,  $L_3$ , and  $C_{GS2}$  form a series resonance at  $\omega_S$  frequency, which is defined in (2). At  $\omega_S$ ,  $R_3$  transforms to  $R_2$  at the primary side, is defined in (3). The reactive part of  $Z_2$  represents an inductance at  $\omega_S$

$$Z_2 = \frac{\omega_S^2 C_{GS2} (M_{12} + M_{13})^2}{g_{m2} (L_2 + M_{23})} + \frac{j\omega_S (L_1 (L_2 + M_{23}) - M_{12} (M_{12} + M_{13}))}{(L_2 + M_{23})}. \quad (10)$$

$R_2$  in simplified structure in Fig. 5 is 20  $\Omega$  at  $\omega_S$ . It is 40  $\Omega$  in the complete front end shown in Fig. 8 as the second stage employs a differential path after the input stage. It reduces the quality factor to 1.16 at the drain of the  $M_1$  device in Fig. 8, showing wideband, low-impedance behavior. When this resistance is converted to a parallel equivalence ( $R_p$ ), it becomes close to 95  $\Omega$  in this design.

The voltage across  $C_{GS2}$  of  $M_2$  device, denoted by  $V_C$ , due to the current  $I_1$  in Fig. 41 can be expressed as

$$V_C = \frac{j\omega(M_{12} + M_{13})I_1}{1 - \omega^2(L_2 + L_3 + 2M_{23})C_{GS2} + j\omega(L_2 + M_{23})g_{m2}}. \quad (11)$$

The BW of this transfer function is proportional to  $g_{m2}$ , and the quality factor is inversely proportional to  $g_{m2}$ . Therefore, with the chosen device transconductance  $g_{m2}$ , the  $V_C/I_1$  transfer characteristic in (11) indicates a wideband response. In contrast, when  $g_{m2} = 0$ , the ideal response becomes sharply peaked. Similarly, if the source of the  $M_2$  device is tied to ground rather than connected to the trifilar transformer arrangement used in this work, the response becomes narrow-band.

## APPENDIX B

The programmable bias voltage for the second-stage transistors  $M_2$  and  $M_2'$  in Fig. 8 is generated by the bias generation circuit shown in Fig. 42(a), in which a current ( $I_b$ ) is passed through a diode-connected device ( $M_b$ ) with its gate and drain tied together, and the resulting gate-bias voltage is applied to the center-tap point of the trifilar transformer,  $V_b$ . Common-mode bias stability is verified by transient simulation in which

the current source ( $I_b$ ) is turned on and off. Specifically, the transient simulation confirms that the generated common-mode bias voltages settle to their intended steady-state values following both turn-on and turn-off transitions. The bias voltages ( $V_b$ ,  $V_{gp}$ , and  $V_{gm}$ ) settle within 10 ns in both the on-to-off and off-to-on transitions of  $I_b$  as shown in Fig. 42(b). In time-division duplexing systems, a settling time shorter than 10 ns may be required. The resistor tied to the gate of  $M_b$  in Fig. 42(a) can then be reduced from 8 k $\Omega$  to 800  $\Omega$  to improve the settling speed. Alternatively, direct gate-bias resistors can be used. The full receiver chain is also examined through transient simulation, with the PLLs driving the respective mixers, and no oscillatory behavior is observed. Additionally, small-signal analysis in Cadence indicates that the interaction between the bias-generation block and the receiver's second stage is negligible. The receiver's bias voltages are generated internally and are programmable via control bits, eliminating the need for an external bias source.

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