A Low-Power 28-GHz Beamforming Receiver With On-Chip LO Synthesis

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***Abstract*—This article introduces a beamforming technique that employs a novel high-impedance transmission line (T-line) architecture and several other concepts to alleviate the trade-off between loss, power consumption, and phase shift resolution. An eight-element prototype receiver (RX) fabricated in 28-nm CMOS technology draws 156 mW, achieving a minimum noise figure (NF) of 3.7 dB, a phase shift resolution of 5.8°, and a local oscillator (LO) jitter of 155 fs_{rms}.**

***Index Terms*—5G receiver (RX), beamforming, phase shift.**

I. Introduction

THE high data rates offered by 5G millimeter-wave radios can materialize if low-cost, low-power beamforming becomes feasible to overcome the high path loss. This demand has motivated extensive work on receiver (RX) implementations targeting the 28-GHz band [1], [2], [3], [4], [5], [6], [7], [8].

Among beamforming RX architectures, those with phase shift in the RF path potentially incur minimum power and hardware overhead as they simply duplicate the low-noise amplifier (LNA) and the phase shift network while sharing the rest of the RX. However, RF phase shifters have typically suffered from severe trade-offs among loss, power consumption, total phase range, and phase resolution. Such realizations draw, per element, 27.5 mW [1] to 103 mW [3]. Moreover, the reported RXs typically do not include complete on-chip local oscillator (LO) synthesis.

This article introduces an eight-element beamforming RX that consumes, per element, 12 mW (18 mW) while achieving a noise figure (NF) of 6.8 dB (3.7 dB) [9]. If the LO synthesis power is included, the power rises to 13.6 mW (19.5 mW).

Section II provides a brief background on RF phase shifting based on transmission lines (T-lines), Section III presents the proposed phase shifter, and Section IV analyzes its time delay. Section V describes the overall RX architecture, and Section VI delves into the design of the building blocks. Section VII deals with the magnetic coupling issues, and Section VIII presents the experimental results.

II. Background

T-lines are a natural candidate for implementing variable RF phase shifters. For example, Kim et al. [2] obtain a phase range of 315° with a resolution of 45° through the use of bypass switches to change the number of sections in a T-line and hence its electrical length. The cost is a loss of 8 to 9 dB. Another method changes the length digitally by either connecting a discrete capacitor between the signal path and return path or enabling return paths that are physically closer to the signal path [3]. This method inevitably increases the loss. As a result, a phase range of 190° with a resolution of 5° is achieved with a loss of 9.3 dB and a power per element of 103 mW. As another example, Kang and Hong [10] propose a standalone 50-Ω T-line sensed at uniformly-spaced taps. Driven by an off-chip signal source and drawing 26.6 mW, the structure achieves a range of 360° at 12 GHz, with a resolution of 22.5°. Of course, an LNA capable of delivering an output to such a low impedance would also consume high power.

III. Proposed Phase Shifter Architecture

A. Basic Idea

Depicted in Fig. 1(a) is the essence of the proposed RF phase shifter. A common-source transistor delivers the RF current to a properly-terminated T-line, and the output voltage tap can slide along this line. This topology offers two benefits. First, the T-line, in principle, achieves an arbitrarily high resolution with guaranteed monotonicity. Second, driving the T-line by a current source consumes less power than by a voltage source, as the latter would require a stage having a sufficiently low output impedance (e.g., a source follower).

While simple, the structure in Fig. 1(a) demands a T-line having a high characteristic impedance, Z_0, so that the overall stage achieves a reasonable voltage gain, $g_{m1}R_L = g_{m1}Z_0$, with moderate input capacitance and power consumption. For this

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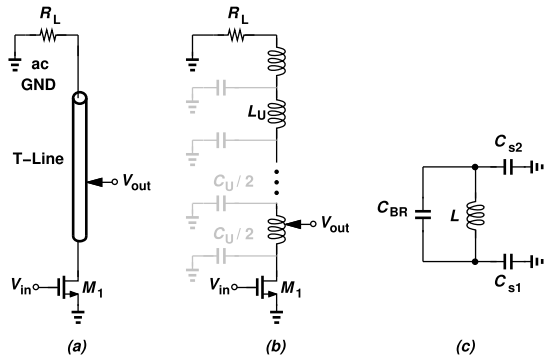


Fig. 1. (a) Basic proposed phase shift method, (b) T-line structure, and (c) lumped inductor model.

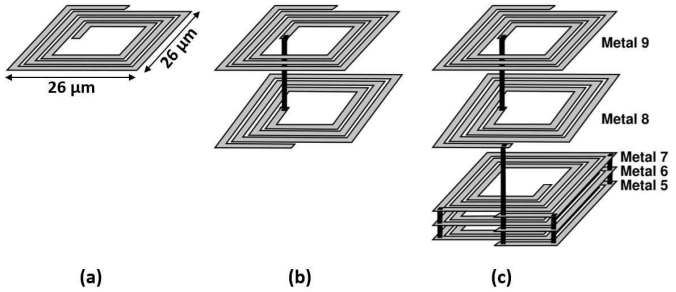


Fig. 2. (a) Single-layer inductor, (b) two-layer stacked inductor, and (c) three-layer stacked inductor.

reason, we seek a distributed LC approximation of the line, as practiced in [2] and [10], but targeting a higher Z_0 [Fig. 1(b)]. This aim requires that we increase the inductance per section, L_U, to the point where the parasitic capacitance of the inductor, C_U, yields a maximum for $Z_0 = \sqrt{L_U/C_U}$. For Z_0 and phase shift calculations, we model each inductor as shown in Fig. 1(c).

B. High-Impedance T-Line Design

Among various spiral inductor structures, the stacked geometry proves particularly useful in this regard as it affords an inductance increase proportional to the square of the number of layers [11]. Three spiral inductor structures, each having a footprint of 26 $\mu m \times 26$ μm and with different levels of stacking (Fig. 2), are simulated in Cadence's EMX at 28 GHz. The two-layer inductor is formed by stacking a metal-8 spiral below an identical metal-9 spiral and connecting the two in series. We also consider a three-layer stacked inductor where the third spiral is formed by connecting metal 7, metal 6, and metal 5 spirals in parallel to compensate for the higher sheet resistance of lower-level metals.

Shown in Table I, the results reveal several points. First, as the number of stacked spirals goes from one to three, L grows by a factor of 7 and Z_0 by a factor of 3. We note that Z_0 climbs by more than a factor of $\sqrt{7}$ because

$$Z_0 = \sqrt{\frac{L/\left(1-\omega^2/\omega_{\mathrm{BR}}^2\right)}{(C_{s1}+C_{s2})\cdot\left(1-\omega^2/\omega_0^2\right)}}, \qquad (1)$$

TABLE I
COMPARISON OF STACKED INDUCTOR STRUCTURES

	Single-layer inductor	Two-layer inductor	Three-layer inductor
L	219 pH	758 pH	1548 pH
C_{BR}	0.3 fF	7.0 fF	6.7 fF
C_{s1}	1.9 fF	2.5 fF	2.8 fF
C_{s2}	2.9 fF	3.2 fF	3.7 fF
Z_0	206 Ω	390 Ω	630 Ω
Phase shift	10.7°	23.5°	39.7°
f_B	283 GHz	63 GHz	44 GHz
Loss for 180° phase shift	4.0 dB	4.7 dB	6.9 dB
T-line area	11372 μm^2	5178 μm^2	3065 μm^2

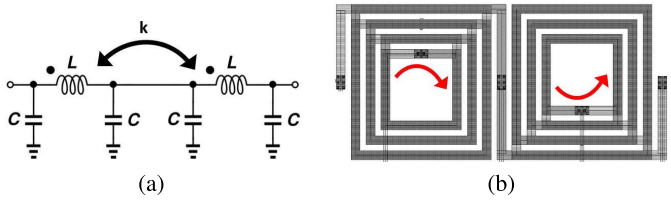


Fig. 3. (a) Adjacent stacked inductors exploiting magnetic coupling. (b) Resultant T-line section with direction of current flow.

where

$$\omega_{\mathrm{BR}} = \sqrt{\frac{1}{\mathrm{LC_{BR}}}} \text{ and } \omega_0 = \sqrt{\frac{\left(1-\omega^2/\omega_{\mathrm{BR}}^2\right)}{L\cdot\frac{C_{s1}C_{s2}}{C_{s1}+C_{s2}}}} \text{[12].}$$

Second, the phase shift per section increases from 10.7° to 39.7°, necessitating other means of improving the resolution (Section III-C). Third, the "Bragg frequency," f_B, i.e., the frequency at which the section in Fig. 1(c) resonates, falls to 44 GHz, still allowing the T-line to operate reasonably well at 28 GHz. A larger number of stacked spirals, on the other hand, would yield an excessively low f_B.

The foregoing analysis points to the three-layer stack as the optimum choice, but we must consider the loss of these geometries as well. To this end, we cascade a sufficient number of sections to obtain a 180° phase shift and evaluate the total loss at 28 GHz. Table I gives values of 4 dB, 4.7 dB, and 6.9 dB for one, two, and three layers, respectively. As a compromise between Z_0 and the loss, we select the two-layer inductor. A Z_0 of 390 Ω affords a bias current as low as 3.2 mA for M_1 in Fig. 1(b). We also note the twofold reduction in the T-line area compared to a single-layer design.

In our efforts toward a higher Z_0 without raising the loss, we propose one more idea. In a conventional artificial T-line, one may include enough spacing between adjacent sections to minimize magnetic coupling. However, we recognize that the polarity of the coupling can be chosen to increase the unit inductance. As illustrated in Fig. 3(a), such a polarity yields a greater Z_0 with no change in loss. For the stacked inductors shown in Fig. 3(b), we have $k \approx 0.06$, and Z_0 rises from 390 Ω to 470 Ω. To our knowledge, this is the highest characteristic impedance reported for an integrated T-line.

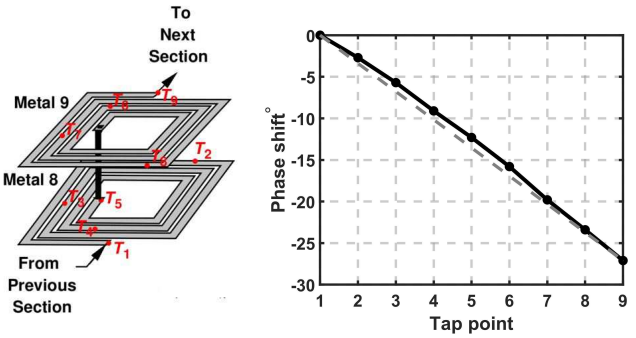


Fig. 4. (a) Tapping inductor at uniformly spaced points. (b) Phase shift versus tap point.

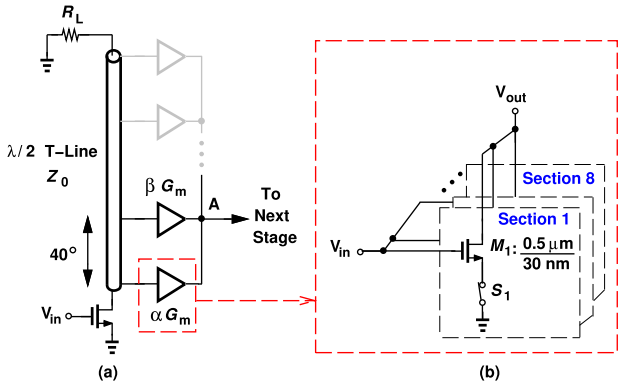


Fig. 5. (a) Tapping T-line with six interpolating G_m stages. (b) G_m stage segmented into eight slices.

C. High-Resolution Phase Shifter

As evident from Table I, T-line segments using two-layer inductors provide a phase resolution of about 24°, which results in about 1 dB degradation in the array gain for eight beamforming elements due to the limited beam steering resolution. Indeed, the T-line approach in [10] also faces this constraint as it senses only the end points of each inductor. We propose two methods that improve the resolution to 5.8°.

First, we view each stacked inductor as a "mini" T-line that can be tapped at any point [Fig. 4(a)]. As a first approximation, we select the taps T_1, T_2, etc., with equally-spaced points along the metal wires and use EMX simulations to evaluate their corresponding phase shifts. Plotted in Fig. 4(b), the results follow a somewhat linear characteristic with a resolution of about 5°. This approach thus proves promising, especially if the nonlinearity observed in Fig. 4(b) can be corrected (Section III-D).

Our thoughts thus far imply that one can simply cascade a number of sections and sense a large number of taps to achieve a high resolution. However, the sense transistors must exhibit a sufficiently high transconductance to negligibly degrade the RX noise figure. Consequently, the input capacitances of these devices, even when they are off, reduces Z_0. This point brings us to our second proposed method of improving the resolution, namely, phase interpolation. Illustrated in Fig. 5(a), the idea is to tap the T-line at only six points and allow [α β] to take on nine different values, thus realizing 8× interpolation. For example [α β] = [7/8 1/8] rotates the phase by about 5°. As shown in Fig. 5(b), each G_m stage is formed as eight

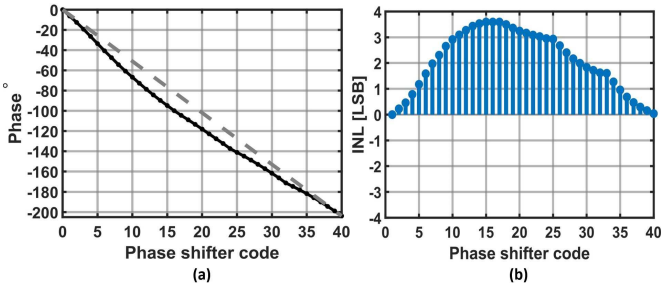


Fig. 6. (a) Phase shift characteristics. (b) INL plot for the phase shifter showing nonlinearity.

parallel common-source devices (M_j) that have a switch (S_j) connecting their source to ground. These switches can be individually turned on or off through a serial bus to realize the fractional coefficients α and β. Note that $\alpha G_m + \beta G_m$ is constant, maintaining the same NF and gain as α and β change.

We should remark that the circuit includes a cascode device at node A [Fig. 5(a)] that improves the backward isolation of the G_m stages as described in Section VI-B.

D. Phase Shifter Nonidealities

Plotted in Fig. 6 are the overall characteristics and integral nonlinearity (INL) of the proposed phase shifter. The INL arises primarily from two mechanisms: the unequal on and off input capacitances of the G_m stages, and the coupling through C_{GD} of the off-state G_m stages to the output node.

With a resolution of approximately 5° and a total range of 204°, the structure requires a 180° swap elsewhere to cover a range of 360°. This is readily accomplished with differential signals (Section V). Nonetheless, the INL reaches nearly 3.6 LSB (≈ 18°), a serious issue causing errors in the beam pointing direction. We correct this INL in Section III-E.

E. Phase Predistortion

Given the ease with which we can select the taps anywhere along the T-line, we surmise that they need not be evenly spaced and, in fact, can be positioned to correct the INL observed in Fig. 6(b). We call this method "phase predistortion." The optimum spacings are obtained through iterative EMX solutions and are shown in Fig. 7(a).[1,2] Depicted in Fig. 7(b), the peak INL now drops to 0.9 LSB and the range varies from 202° to 210° across process and temperature corners. Phase-mismatch simulations for different phase shifter codes predict a maximum standard deviation of 0.26°.

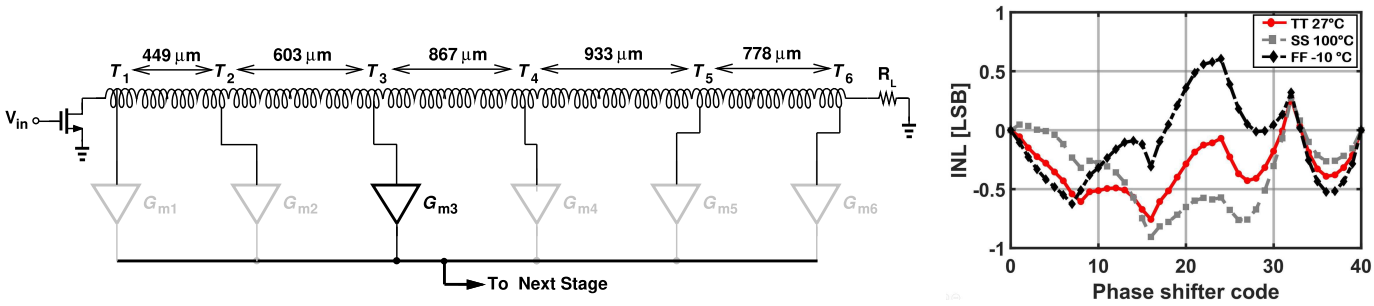
The phase shift characteristics for different frequencies and the associated INL are shown in Fig. 8(a) and (b), respectively. The peak INL remains within 1 LSB for a frequency range of 27.7 GHz to 29.5 GHz.

Fig. 9 displays the simulated loss of the proposed T-line as a function of the tapping points. To compensate for the loss beyond tap 4, we allow a programmable gain in the LNA (Section VI).

Phase predistortion is prone to some error owing to the inaccuracy of the electromagnetics modeling. Such discrepancies can be corrected by introducing an additional bit in

[1]The entire T-line is extracted in these iterations to account for mutual coupling between inductors.

[2]By spacing, we mean the length of the inductor wire between two taps.



(a) (b)

Fig. 7. (a) Phase shifter with predistorted T-line taps. (b) INL plot across process and temperature corners.

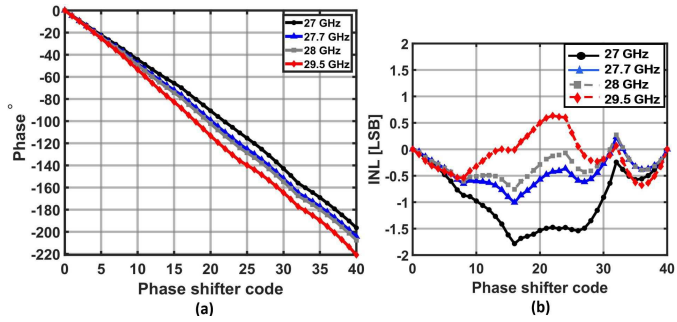


Fig. 8. (a) Phase shift and (b) INL variation with frequency.

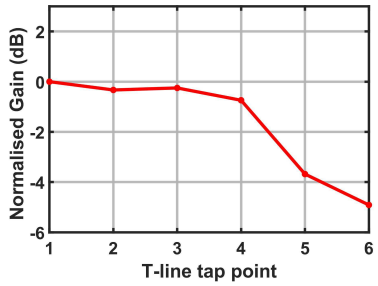


Fig. 9. T-line loss across tapping points.

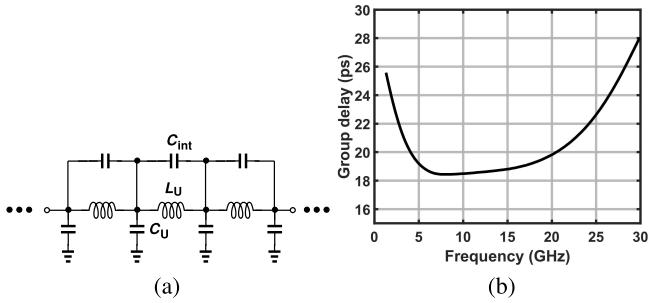


Fig. 10. (a) T-line with interwinding capacitance. (b) T-line group delay profile.

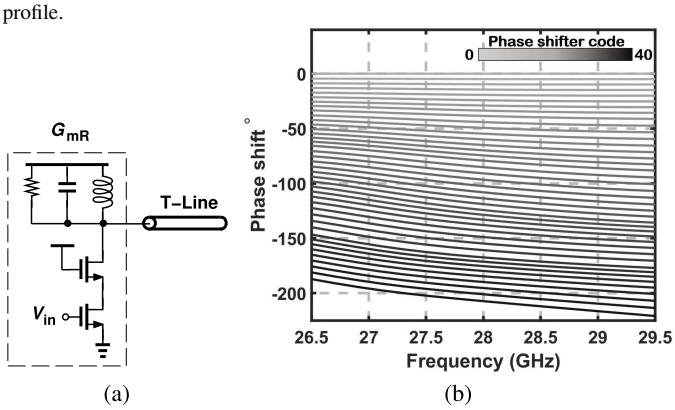


Fig. 11. (a) G_{mR} stage with resonant load. (b) Phase shift versus frequency profile.

the interpolation network and then performing code trimming based on measurements. We demonstrate such trimming to improve phase shift accuracy at the cost of sacrificing the resolution from 5.8° to 10° (Section VIII-C).

The principal advantage of the proposed technique is its low power consumption due to the high T-line impedance (as demonstrated in the experimental results).

IV. T-Lines as True Time Delays

In beamforming systems targeting wideband RF channels, it is desirable for the phase shift network in each element to provide a constant group delay and hence a "true time delay." In principle, a T-line satisfies this condition. However, two imperfections in our work lead to some departure from the ideal behavior.

First, the interwinding capacitance, C_{int}, of the inductors used in the phase shift network creates an additional path for current flow at sufficiently high frequencies [Fig. 10(a)], an effect absent in ideal T-lines. This leads to the gradual departure from T-line behavior as we approach closer to the Bragg frequency defined in Section III-B. The group delay of the T-line across frequency shows that the variation becomes prominent beyond 20 GHz [Fig. 10(b)].

Second, the G_m stage driving the T-line contains a *resonant* load [Fig. 11(a)]. This circuit's phase shift changes to some extent because the characteristic impedance of the T-line varies slightly with the phase shift code.[3]

The simulated phase shift profile across frequency is shown in Fig. 11(b). The reduction in the slope of the phase shift at higher frequencies is consistent with what we observe in the measurements and is mainly caused by the resonant load as described above. We report the measured phase shift characteristics in Section VIII.

V. Overall RX Architecture

The eight-element RX and its LO generation are shown in Fig. 12(a). Signal combining occurs in two steps: the outputs

[3]This occurs because of the unequal on and off input capacitances of the G_m stages in Fig. 5(a).

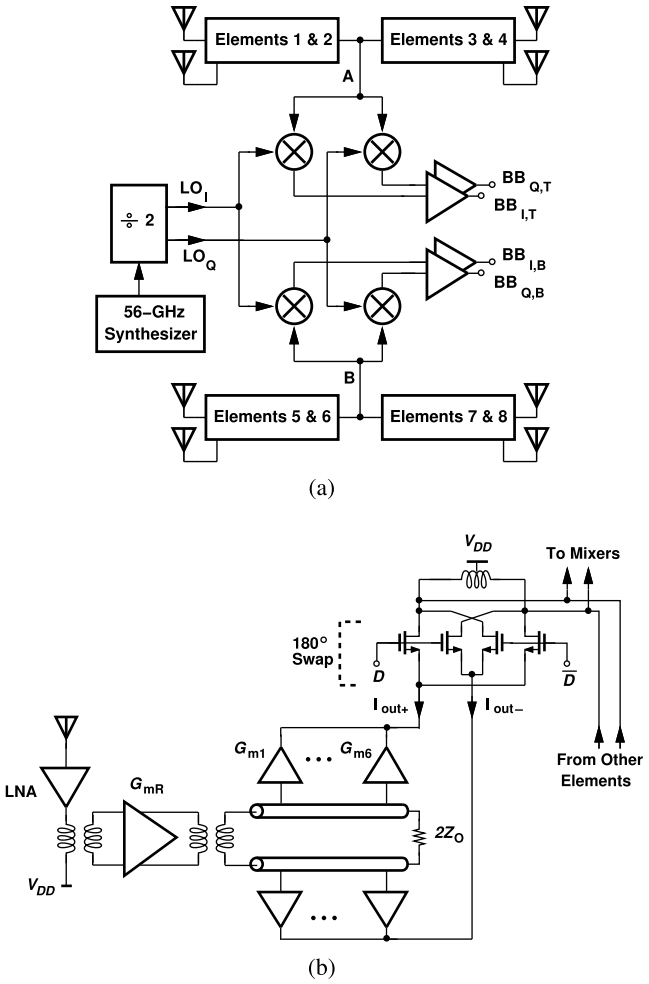


Fig. 12. (a) Overall architecture. (b) Front-end realization of one element.

of elements 1 to 4 are summed in the RF domain at point A. Similarly, the other four meet at B. Two sets of quadrature downconversion mixers yield four baseband (BB) outputs, which are then combined off-chip. This approach provides greater flexibility in test and characterization and also reduces the capacitance at A and B.

Rather than generate the LO at 28 GHz and deal with the difficult task of quadrature separation, we incorporate a 56-GHz synthesizer and a ÷2 circuit. The I and Q phases of the LO are then distributed to the four mixers.

The distribution of signals in Fig. 12(a) faces certain trade-offs. For the four mixers, both their RF inputs and their LO waveforms must travel a long distance (due to the physical dimensions of the beamforming elements). According to simulations, we prefer to maintain shorter interconnects for the RF path and must therefore manage LO distribution over a distance of about 600 μm. This is accomplished by means of self-biased inverters acting as repeaters in each of the four I and Q paths.

Shown in Fig. 12(b) are the implementation details of one element's front end. An LNA driving a transformer delivers differential signals to two T-lines, and the interpolated outputs travel through four cascode devices that can impart a 180° swap (based on the control signal D), extending the total phase shift to more than 360°. The outputs of four elements

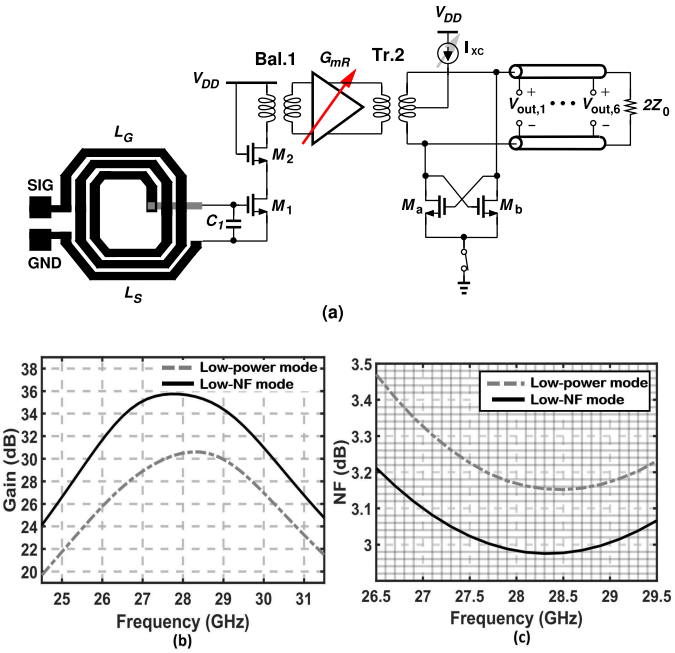


Fig. 13. (a) Front end circuit realization, (b) front-end gain, and (c) front-end NF.

are combined at the resonant load and propagate to the downconversion mixers.

Each element is designed to operate in one of two modes. In the low-power mode, the bias currents in the LNA and G_{mR} stage are reduced, yielding an RX NF of 6.8 dB for 13.6 mW/element. In the low-noise mode, the currents are higher, lowering the NF to 3.7 dB while leading to 19.5 mW/element.

VI. Building Blocks

A. Front End

Depicted in Fig. 13(a) is the realization of the front end. A critical issue at these frequencies relates to the return path for the RF current entering the LNA. That is, the impedance between the source of M_1 and the ground pad must be controlled well. To this end, we introduce interwined inductors L_G and L_S, which along with M_1 and C_1, create an input impedance given by

$$Z_{\text{in}} = \frac{1 + g_{m1} r_S}{(C_{GS} + C_1)\, s} + (L_G + L_S + 2M)\, s + \frac{g_{m1}\,(L_S + M)}{C_{GS}} + r_G + r_S\ , \tag{2}$$

where r_G and r_S denote the series resistances of L_G and L_S, respectively, and M is the mutual coupling between the two inductors. For the first two reactive terms to cancel each other, we add C_1 = 18 fF to C_{GS} = 8 fF. More importantly, we benefit from $2M$ = 123 pH, which raises the second reactance without contributing to r_G or r_S.

If only the noise of r_G, r_S, and M_1 in Fig. 13(a) is considered, the NF at the resonance frequency, ω_0, can be expressed as

$$\text{NF} = 1 + \frac{r_G + r_S}{R_S}$$

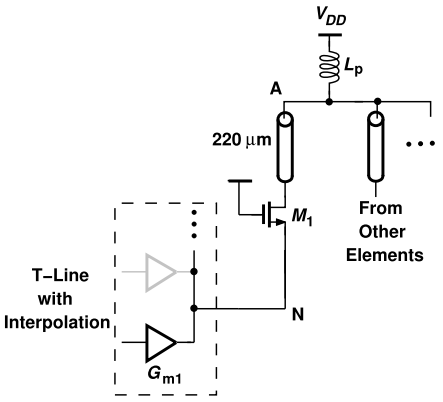


Fig. 14. RF combining network.

$$+\gamma \cdot g_{m1} \cdot R_S \cdot \left(1+\frac{r_G+r_S}{R_S}\right)^2 \left(\frac{\omega_0}{\omega_T}\right)^2, \qquad (3)$$

where ω_T denotes the transistor's transit frequency. The fraction $\beta = (r_G + r_S)/R_S$ is not negligible. With mutual coupling between L_G and L_S, we have $\beta = 0.15$. But without coupling, the inductors must be large, yielding $\beta = 0.19$, raising the second and third terms, and degrading the NF from 2.74 dB to 3.14 dB.

With a loss of about 4.9 dB, the T-lines in Fig. 13(a) yield an RX gain that depends on which G_m stages are enabled in Fig. 12(b). To alleviate this effect, we implement 3.6 dB of gain control in G_{mR}. It is essential that G_{mR} and the T-lines provide a reasonable gain, and hence minimize the noise contributed by the downconversion mixers. Rather than consume a high power in G_{mR}, we insert a cross-coupled pair, M_a and M_b, to increase the gain from 6.9 dB to 12.3 dB.

The LNA, G_{mR}, and the cross-coupled pair draw a total supply current of 12.6 mA in the low-noise mode and 6.6 mA in the low-power mode. Fig. 13(b) and (c) plot the simulated gain and NF, respectively, in the two modes.

The 3-dB bandwidth of the frontend is designed to be 3.3 GHz to cover the n257 (26.5 GHz–29.5 GHz) and n261 (27.5 GHz–28.35 GHz) bands in 5G NR standard [13].

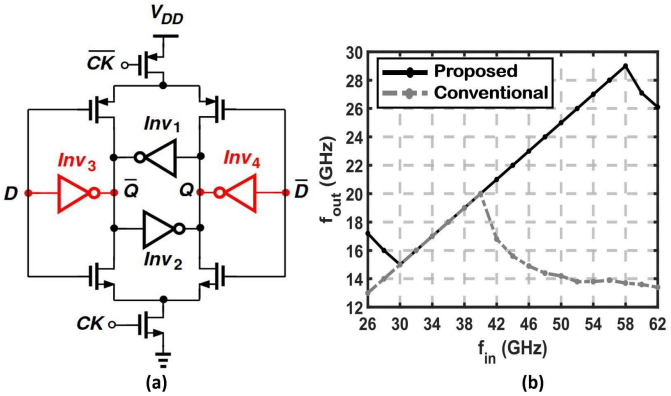
B. RF Combining

In the RX architecture of Fig. 12(a), the RF signals generated by each element must travel 220 μm before they can be combined. It is possible to simply short the outputs of the T-line interpolation networks of the elements, but the large capacitive loading would lead to a great loss. We instead realize the combiner as shown in Fig. 14, where a cascode device isolates the interpolated output from the long interconnects. The resonance at A produces an equivalent parallel resistance of about 430 Ω, negligibly contributing to the RX NF. Additionally, the cascode device improves the isolation from node A to the input of the G_m stages to −44 dB.

The downconversion mixers are realized as passive topologies that are driven directly by the combiner.

C. LO Generation and Distribution

As mentioned in Section V, we generate a 56-GHz LO and utilize a postdivider to obtain I and Q phases at 28 GHz. The synthesizer architecture is based on the work reported in [14] and [15] and draws 7.8 mW of power.



Process Corner	Supply Voltage	Temp.	Low Freq.	High Freq.
TT	1.0	27° C	34 GHz	68 GHz
SS	0.98	100° C	30 GHz	58 GHz
FF	1.02	-10° C	40 GHz	82 GHz

(c)

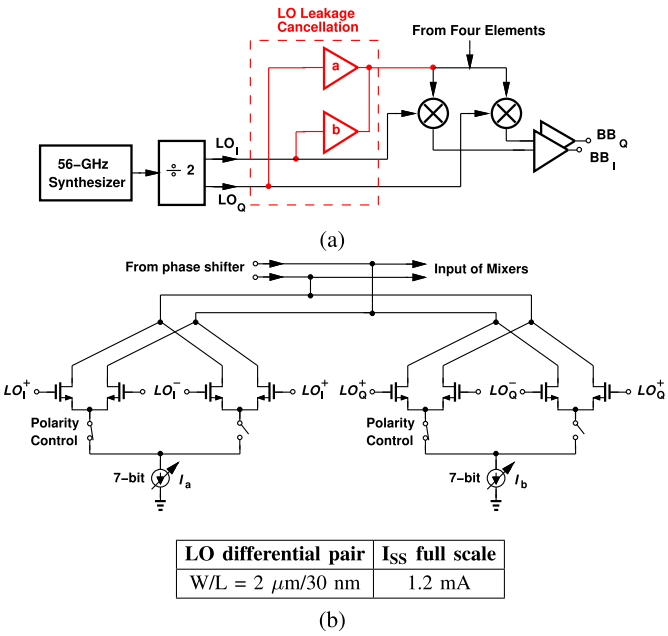
Fig. 15. (a) Latch topology, (b) divider output versus input frequency, and (c) divider input frequency range.

The postdivider poses significant challenges in 28-nm CMOS technology. First, it preferably avoids inductors so as to occupy a small footprint between the beamforming elements. Second, it should generate rail-to-rail swings to facilitate the distribution over a 600-μm distance. Third, it should present a reasonable power-speed trade-off. To address these points, we propose the latch topology shown in Fig. 15(a). Without Inv_3 and Inv_4, the latch resembles the structure in [16] and can be viewed as two clocked CMOS (C^2MOS) stages (one on the left, one on the right) whose clocked transistors are merged. The circuit, however, fails beyond 40 GHz in the slow-slow corner [Fig. 15(b)]. To improve the speed, we add feedforward paths Inv_3 and Inv_4, which, asynchronously, carry the inputs to the outputs. That is, these inverters begin to write the new state at Q and $\overline{Q}$ even before the clocked devices are enabled. As evident from Fig. 15(b), the maximum speed now climbs to 58 GHz. The unlocked path does pose a lower limit on the clock frequency, but the lock range is fairly wide. Fig. 15(c) summarizes the simulation results across corners, indicating a sufficient margin. The divider draws 4.7 mW at 56 GHz.

Each of the four 28-GHz LO phases produced by the postdivider travels through self-biased inverters acting as repeaters along a distance of 600 μm. These inverters collectively consume 25 mW, a significant fraction of the overall power, and a drawback of using a central synthesizer.

D. LO Leakage Cancellation

LO leakage can desensitize the mixers and BB chain in a direct-conversion RX. We introduce a leakage cancellation technique at RF that minimally affects the desired signal. As shown in Fig. 16(a), a weighted sum of LO_I and LO_Q is injected at the *input* of the mixers with scaling factors equal



LO differential pair	I_{SS} full scale
W/L = 2 μm/30 nm	1.2 mA

Fig. 16. (a) LO leakage cancellation implementation and (b) circuit realization.

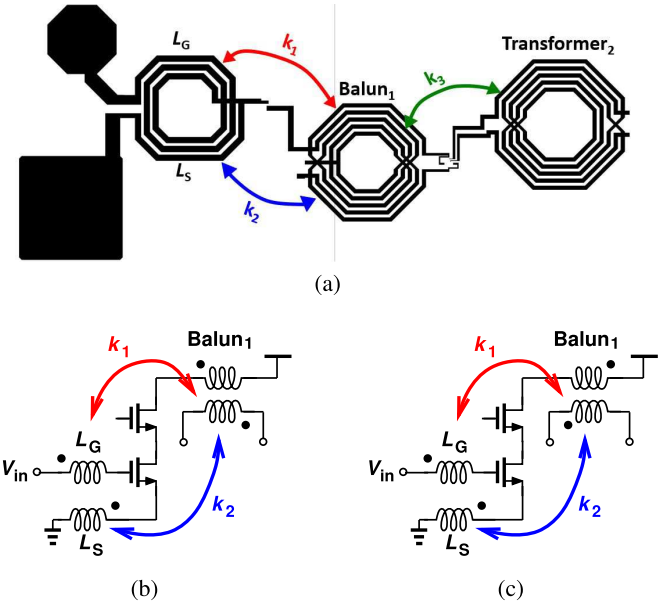


Fig. 17. (a) Single-element front end floorplan, (b) negative feedback case, and (c) positive feedback case.

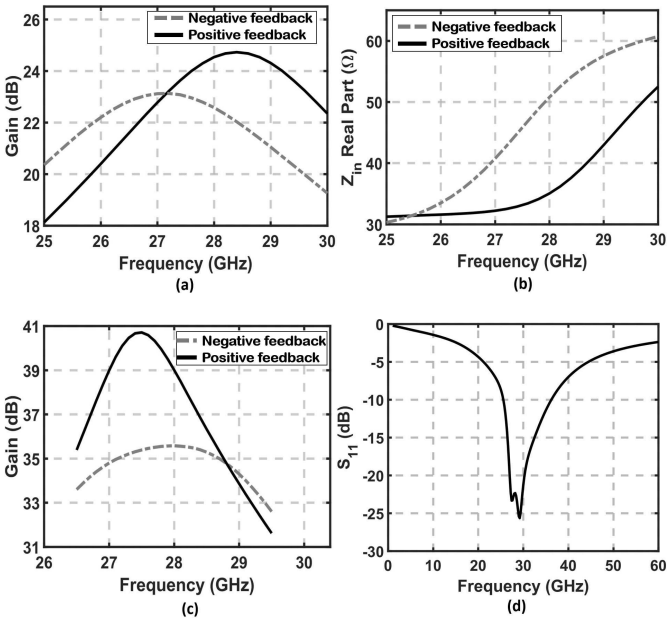


Fig. 18. (a) LNA gain and (b) LNA input impedance real part for different feedback polarities. (c) Front-end gain for different feedback polarities between Balun_1 and Transformer_2. (d) S_{11} of the RX.

to a and b. Depicted in Fig. 16(b), the circuit implementation consists of simple differential pairs whose programmable tail currents define a and b. The output currents merge with phase shifter outputs (e.g., at node A in Fig. 14).

The dc offsets at the output of the mixers can thus be changed by nearly ± 130 mV. According to simulations, this network raises the RX NF by about 0.1 dB when injecting full-scale LO_I and LO_Q currents.

VII. Magnetic Coupling Issues

A. Intraelement Coupling

The use of inductors and baluns in the front end of each element must deal with coupling among them at 28 GHz. Rather than view these effects as *undesirable*, and hence separate the devices by a long distance, we propose to investigate them closely.

Consider the floor plan shown in Fig. 17(a), where the most critical coupling factors are denoted by k_j. Depicted in Fig. 17(b) is the circuit representation, with the dot convention selected to provide *negative* feedback to both L_G and L_S. By swapping the terminals of both the primary and secondary of Balun_1, we can realize *positive* feedback instead [Fig. 17(c)]. The simulation results in Fig. 18(a) and (b) suggest that the LNA response shifts to a higher frequency while the real part of the input impedance falls to about 35 Ω (and $|S_{11}| = -15$ dB). The 3-dB bandwidth of the LNA falls from 4.6 GHz to 3.7 GHz by selecting positive feedback, but this does not have a significant impact on the overall front-end bandwidth, which is mainly limited by the following G_{mR} stage and polarity of k_3.

The foregoing thoughts reveal that, in fact, both types of feedback are tolerable in this case. But when we include Transformer_2 in Fig. 17(a) and its interaction with Balun_1, a clear choice emerges. Let us assume k_1 and k_2 provide positive feedback. Depending on the sign of k_3 in Fig. 17(a), we obtain the overall front-end performance plotted in Fig. 18(c), concluding that $k_3 < 0$ (negative feedbak case) leads to a flatter response. With this choice, $|S_{11}|$ is better than -10 dB across about 10 GHz.

We should remark that the T-lines used in each element exhibit negligible coupling to the front end owing to their quadropole structure. Since the adjacent inductors in the T-line carry current in opposite directions [Fig. 3(b)], their magnetic fields act in opposite directions in the area outside the two

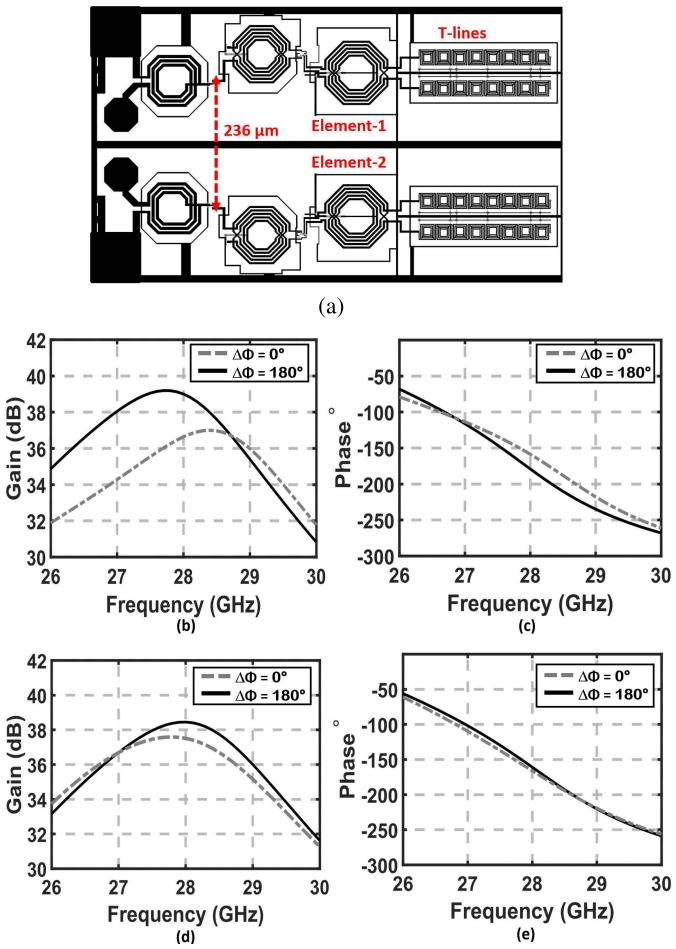


Fig. 19. (a) RX front end with guard rings, (b) front-end gain response without guard rings, (c) front-end phase response without guard rings, (d) gain response with guard rings, and (e) phase response with guard rings.

inductors. At sufficiently remote points from the two inductors, the two magnetic fields have similar strengths and almost cancel each other.

B. Interelement Coupling

The coupling between adjacent beamforming elements proves problematic, an issue evidently not recognized by the prior art. This effect manifests itself because the signal received by two elements can have an arbitrary phase difference. The coupling occurs primarily among the inductors.

Consider the floorplan shown in Fig. 19(a), where grounded guard rings have been added. Shown in Fig. 19(b) and (c) are the simulated gain and phase of one element, in the absence of guard rings, while the adjacent element receives a signal with the same phase ($\Delta\phi = 0°$) or opposite phase ($\Delta\phi = 180°$). The gain and the phase of the element change by 2.4 dB and 20.4°, respectively. Such dependencies can complicate the beamforming algorithm. With the guard rings present, on the other hand, Fig. 19(d) and (e) imply small changes (less than 1 dB and 6°).

VIII. Experimental Results

The proposed 8-element RX has been fabricated in TSMC's 28-nm CMOS technology. Shown in Fig. 20, the die occupies

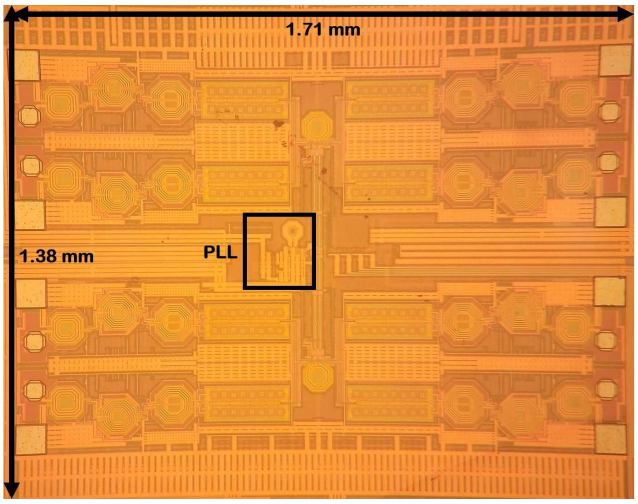


Fig. 20. Die photograph.

TABLE II
Measured Power Consumption Breakdown

	Low-NF Mode	Low-power Mode
Front end	8 × 13.75 mW	8 × 7.875 mW
LO generation and distribution	38 mW	38 mW
Baseband Amplifiers	8 mW	8 mW
Total	8 × 19.5 mW	8 × 13.625 mW

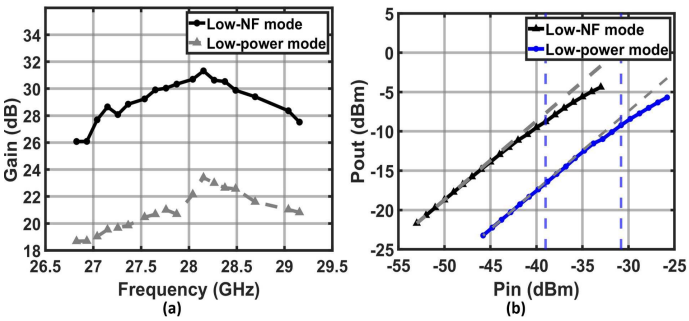


Fig. 21. (a) Single-element gain and (b) 1-dB compression characteristics.

an area of 1.71 *mm* × 1.38 *mm*. The RF inputs are applied through high-frequency probes. Table II depicts the power consumption breakdown of the overall chip, indicating the signal path values as $8 \times P_j$, where P_j is that consumed in one element.

A. NF Measurements

In a beamforming environment, all of the elements sense copies of the same signal and align them in phase. The definition and measurement of the NF must therefore represent this situation.

For N elements, such a definition has been proposed in [17] as

$$\mathrm{NF} = N\frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}}, \tag{4}$$

where $\mathrm{SNR_{in}}$ denotes the SNR at the input of a single element, but $\mathrm{SNR_{out}}$ represents the SNR at the output of the entire array. We show in the Appendix that by connecting N independent noise sources to the elements and performing a Y-factor NF

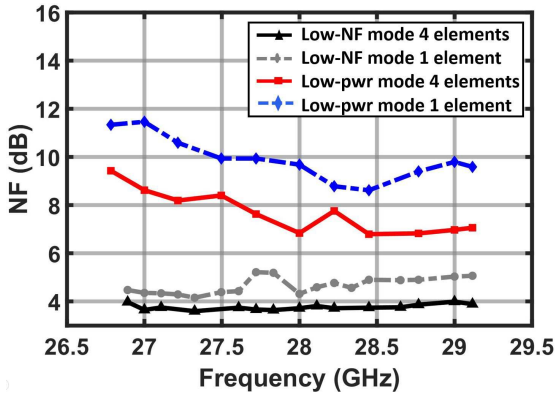


Fig. 22. Measured NF.

measurement, we can obtain the NF according to the above definition.

B. Gain and NF Measurements

Fig. 21(a) plots the measured voltage gain of a single element in the two modes of operation. The peak occurs at 28.2 GHz, and the 3-dB bandwidth is 1.7 GHz. While the gain results for both modes are close to the simulated values (31 dB and 26 dB for low-noise and low-power mode, respectively), the bandwidth is narrower. The bandwidth is limited by the load of G_{mR} and can be extended by switched-capacitor tuning. For the reported measurements, the switched-capacitor networks for the LNA and G_{mR} stages are tuned to center the response at 28 GHz.

Fig. 21(b) displays one element's input-output characteristics. The 1-dB compression point falls from −31 dBm to −39 dBm in the low-noise mode due to the high swing at the input of the phase interpolating G_m stages in Fig. 5.

The NF is first measured for a single element, while other elements are disabled and hence inject no noise into the signal path. Shown in Fig. 22, the results suggest that, at 28 GHz, the NF is equal to 4.3 dB and 9.7 dB in the low-NF and low-power modes, respectively.

We next characterize the noise behavior of the beamforming RX with four elements enabled and each driven by a Keysight 346C-K01 noise source. The combined outputs are then applied to an NF meter, which performs a Y-factor measurement. As depicted in Fig. 22, the NF at 28 GHz is now equal to 3.7 dB in the low-NF mode and 6.8 dB in the low-power mode.

We should remark that the improvement of the NF for the four-element enabled case over the single-element case can be explained through Eq. (5) and Eq. (6) in the Appendix.

C. Phase Shift Measurements

In order to measure the phase shift characteristics, an RF input is applied to two elements simultaneously, and one element's phase setting is frozen while the other's is varied.[4] Since the baseband outputs of the two selected elements are separate [$BB_{I,T}/BB_{Q,T}$ and $BB_{I,B}/BB_{Q,B}$ from Fig. 12(a)], one can be compared against the other. Plotted in Fig. 23(a) are the results for four elements on the same chip, covering about 200° with a resolution of 5.8° and an rms error of 5.4°. The measured phase variation between different elements ranges from 0.4° to 3.5° across all codes.

[4]This is accomplished by enabling the interpolation network in Fig. 5, changing α and β, and enabling different G_m stages through a serial bus.

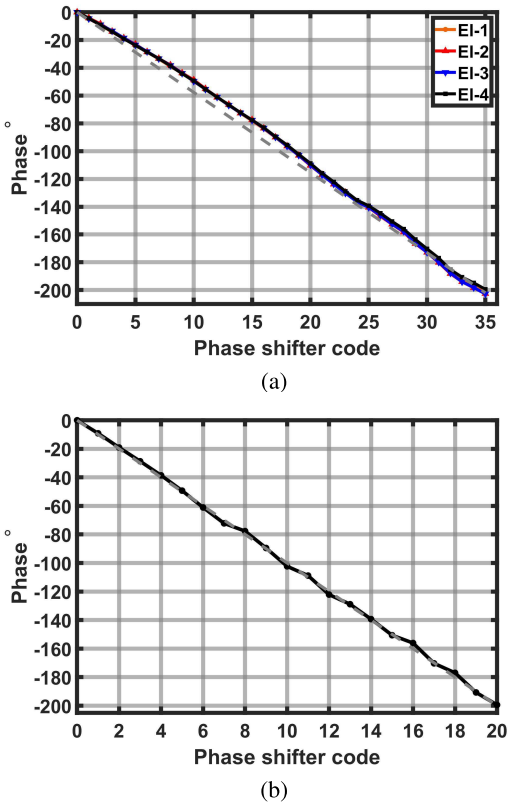


Fig. 23. (a) Phase shift characteristics at 28 GHz. (b) Phase shift characteristics for a subset of the codes.

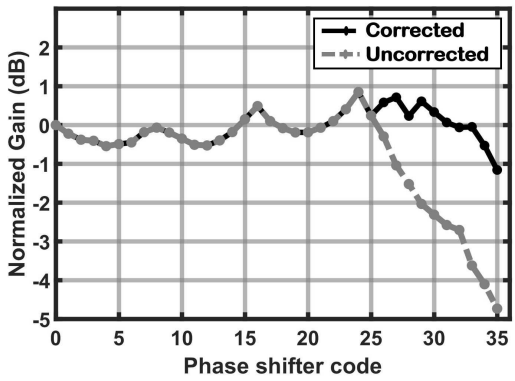


Fig. 24. Phase shifter gain characteristics.

It is possible to trade phase resolution for accuracy. To this end, we select only 21 codes [Fig. 23(b)], obtaining a resolution of 10° with an rms error of 1.6°.

Recall from Section VI that the phase-dependent loss of the T-lines is partially corrected by controlling the transconductance of G_{mR} in Fig. 13(a). Fig. 24 plots the measured results

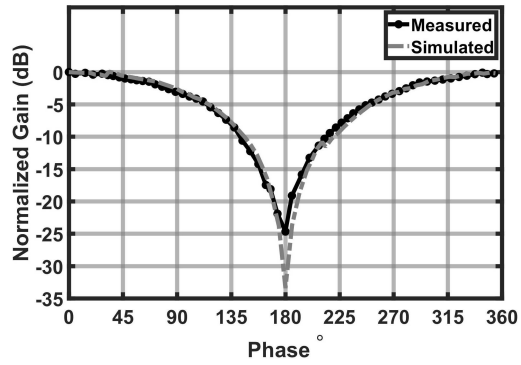


Fig. 25. Two-element pattern.

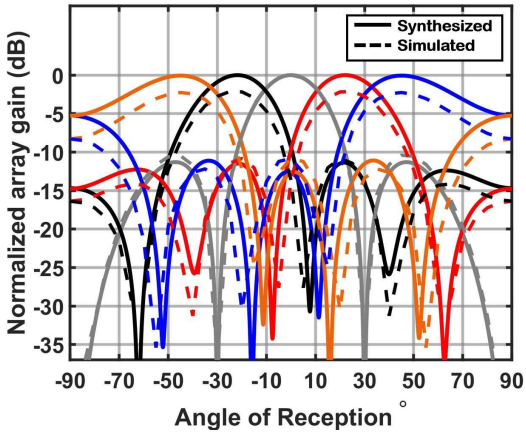


Fig. 26. Synthesized and simulated beam patterns.

with and without this correction. The maximum variation is reduced from 5.6 dB to about 2.0 dB for all phase settings.

To evaluate gain uniformity between elements, the foregoing two-element phase measurement is repeated; however, now we select two elements whose RF outputs are combined on-chip, and the amplitude of their combined baseband output is monitored.[5] This leads to the phased-array gain plotted in Fig. 25 as a function of the phase shift of one element. The large peak-to-null ratio of 24.5 dB results from the fine phase resolution and the small gain mismatch.

The four-element beam patterns are synthesized at 28 GHz using the phase shift profile of the four elements in Fig. 23(a) and the gain profile in Fig. 24. The results along with the simulated beam patterns for 0°, 22.5°, and 45° beam steering angles are plotted in Fig. 26.

As mentioned in Section IV, the behavior of the proposed phase shift method as a true time delay is also of interest, although the maximum RF channel bandwidth of 400 MHz in 5G radios does not pose a tight requirement on the group delay. Fig. 27 plots the measured phase shift as a function of frequency.

The phase shift versus frequency exhibits variations in slope due to the limitations described previously (Section IV).

[5]The inputs to the two elements are nominally matched but still exhibit about 15 ps mismatch. The resultant phase mismatch is compensated with the on-chip phase shifter.

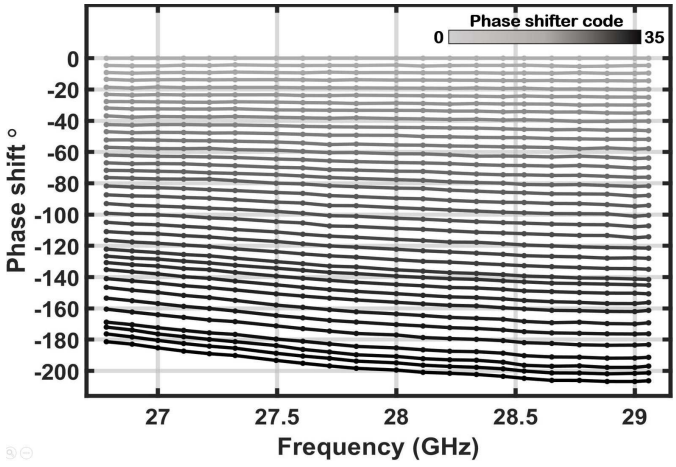


Fig. 27. Phase shift characteristics as a function of frequency.

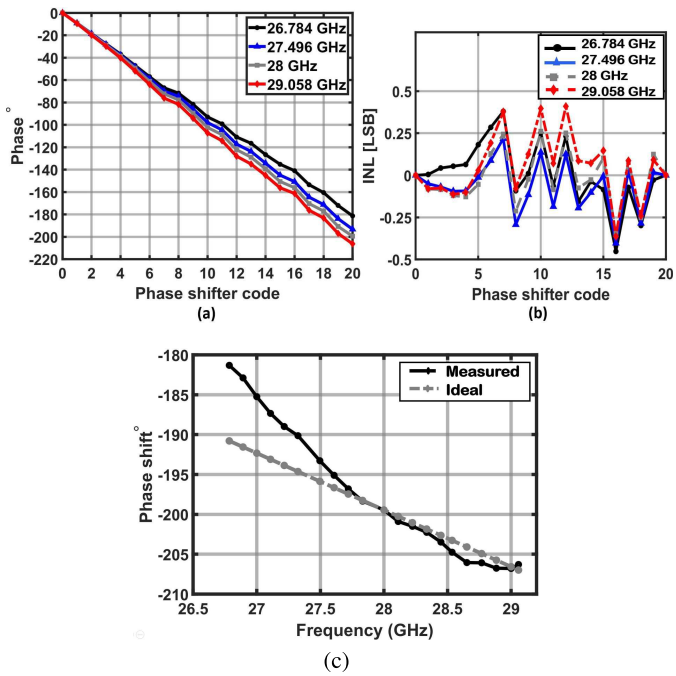


Fig. 28. (a) Phase shift, (b) INL, and (c) phase shift range variation with frequency.

However, we make two observations to illustrate its utility across the frequency range of interest.

1) Phase characteristics for the same subset of codes used in Fig. 23(b) are plotted for different frequencies in Fig. 28(a). The range increases from 181° for 26.784 GHz to 206° for 29.058 GHz. Their INL plots, shown in Fig. 28(b), show a peak value of −0.45 LSB, illustrating that the linearity of phase shift versus codes is maintained across frequency.
2) The total phase shift range of the phase shifter is plotted across frequency and compared with that of a true-time-delay based phase shifter in Fig. 28(c). We note that the system reasonably approximates true time delay behavior from 28 GHz to 29 GHz. However, at lower frequencies, the error becomes larger and would lead

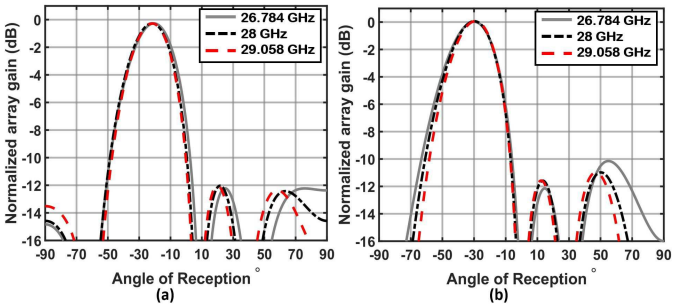
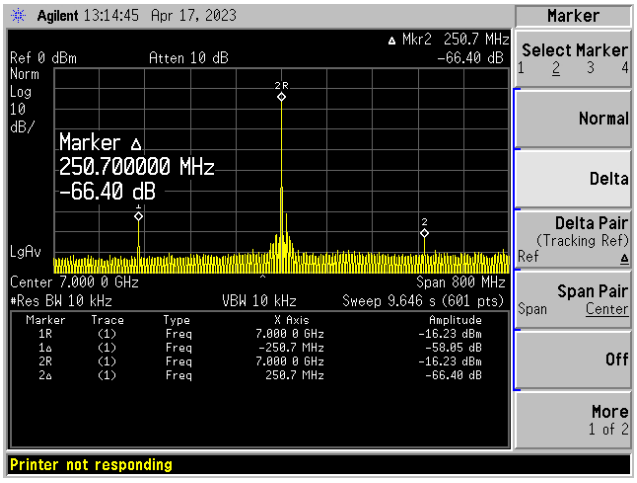
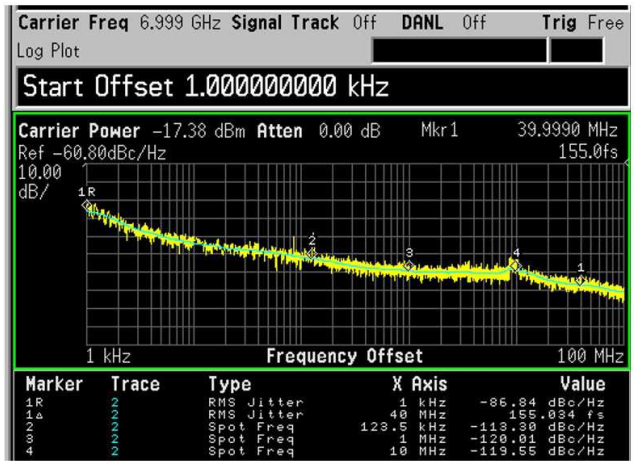


Fig. 29. Synthesized beam patterns across frequency for (a) 22.5° and (b) 30° beam steering angle.



(a)



(b)

Fig. 30. (a) Synthesizer output spectrum after ÷8. (b) Synthesizer output phase noise after ÷8.

to some beam squinting errors. The synthesized four-element beam patterns for 22.5° and 30° steering angles are plotted for different frequencies in Fig. 29. For the synthesis, each element's gain and phase characteristics are taken from Figs. 24 and 27, respectively. The beam-pointing direction incurs total deviation of 1.2° and 0.92° for 22.5° and 30° steering angles, respectively.

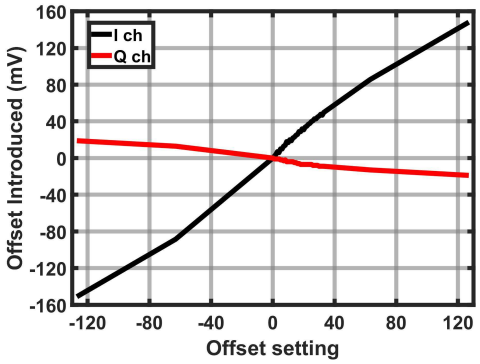


Fig. 31. Baseband offsets versus LO_Q injection code.

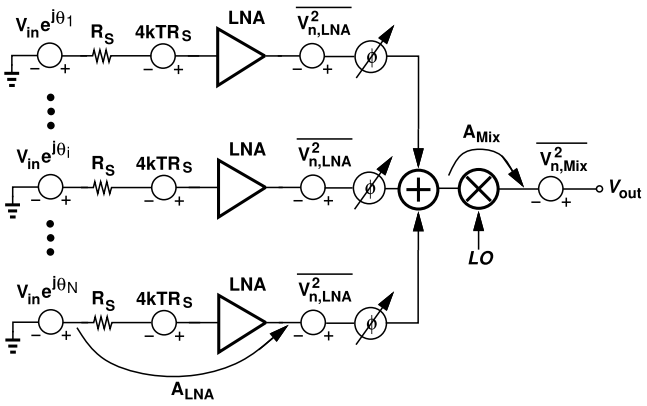


Fig. 32. Multi-element RX model.

D. Synthesizer Measurements

The output spectrum of the synthesizer is monitored after a ÷8 chain in its feedback path. Plotted in Fig. 30(a), the result reveals a reference spur level of −58 dBc, which translates to −40 dBc at the VCO output.

The phase noise profile at this divider output is depicted in Fig. 30(b), reaching −120 dBc/Hz at 10-MHz offset. The integrated jitter from 1 kHz to 40 MHz amounts to 155 fs_{rms}.

E. LO Leakage Cancellation Measurements

The LO leakage cancellation circuit is tested by observing the baseband dc offsets introduced as *a* or *b* in Fig. 16 are programmed in a given direction. Fig. 31 depicts the measured offset introduced in the I and Q channels as a function of the LO_Q injection code. Correction of one baseband output should ideally leave the other intact. The change in Q channel output, on the other hand, suggests the need for some iteration during offset calibration.

IX. Comparison With Prior Art

Table III summarizes the performance of the proposed RX and compares it to that of the prior art. Compared to [18], we achieve a comparable NF but with about half of the power consumption while delivering quadrature BB signals. Also, in the low-power mode, our prototype consumes 2.3× less power than [1] with 0.5 dB less NF.

TABLE III
PERFORMANCE SUMMARY AND COMPARISON

	This Work		[1] Mondal JSSC 18	[19] Sadhu ISSCC 22	[5] Dunworth ISSCC 18	[18] Pang ISSCC 22
	Low NF	Low Power				
Input Frequency (GHz)	27.3 - 29	27.5 - 29.2	25 - 30	24 - 30	25.8 - 30.2	24.25 - 44*
No. of RX Elements	8		8	16 per IC 256 in module	24	2
NF_{min} (dB)	3.7	6.8	7.3	3.92	4.4	3.6
Gain (dB)	31.3 (1 element)	23.4 (1 element)	34 (1 element)	23.5 (1 element)	34 (4 elements)	15 (1 element)
Input P_{1dB} (dBm)	−39 (1 element)	−31 (1 element)	-29^a / -21^b (1 element)	-30.8 (1 element)	N.A.	-17.6 (1 element)
External LO input frequency	f_{ext} = 250 MHz		f_{ext} = 20 - 24 GHz	f_{ext} = 21 - 27 GHz $(IF_{out}$ = 3 GHz)	N.A. $(IF_{out} = 6.5$ GHz)	f_{ext} = 16 - 26 GHz, $(IF_{out} = 8$ GHz)
Power per Element (excl. synth.)(mW)	17.9	12	27.9	90	N.A.	36
Power per Element (incl. synth.)(mW)	19.5	13.6	-	-	42	-
Phase Resolution	5.8° or 10°		N.A.	4° - 5.6°	45°	N.A.
Technology	28-nm CMOS		65-nm CMOS	130-nm SiGe BiCMOS	28-nm CMOS	65-nm CMOS

[a]High-gain mode [b]Low-gain mode *Low-band mode

APPENDIX

Consider only the top path in Fig. 32, where we have

$$\mathrm{NF}_1 = 1 + \frac{\overline{V_{n,\mathrm{LNA}}^2}}{4kTR_S \cdot A_{\mathrm{LNA}}^2} + \frac{\overline{V_{n,\mathrm{Mix}}^2}}{4kTR_S \cdot A_{\mathrm{LNA}}^2 A_{\mathrm{Mix}}^2}. \quad (5)$$

For the entire array, we write

$$\begin{aligned}\mathrm{NF}_N &= N \cdot \frac{\mathrm{SNR}_{\mathrm{in,single\,element}}}{\mathrm{SNR}_{\mathrm{out}}} \\ &= 1 + \frac{\overline{V_{n,\mathrm{LNA}}^2}}{4kTR_S \cdot A_{\mathrm{LNA}}^2} + \frac{\overline{V_{n,\mathrm{Mix}}^2}}{4kTR_S \cdot N \cdot A_{\mathrm{LNA}}^2 A_{\mathrm{Mix}}^2}. \quad (6)\end{aligned}$$

In a Y-factor NF measurement with N independent noise sources, we have

$$\begin{aligned}\mathrm{NF} &= \frac{N \cdot 4kT_C R_S \cdot A_{\mathrm{LNA}}^2 A_{\mathrm{Mix}}^2 + N \cdot \overline{V_{n,\mathrm{LNA}}^2} A_{\mathrm{Mix}}^2 + \overline{V_{n,\mathrm{Mix}}^2}}{N \cdot 4kT_C R_S \cdot A_{\mathrm{LNA}}^2 A_{\mathrm{Mix}}^2} \\ &= 1 + \frac{\overline{V_{n,\mathrm{LNA}}^2}}{4kT_C R_S \cdot A_{\mathrm{LNA}}^2} + \frac{\overline{V_{n,\mathrm{Mix}}^2}}{4kT_C R_S \cdot N \cdot A_{\mathrm{LNA}}^2 A_{\mathrm{Mix}}^2}, \quad (7)\end{aligned}$$

where T_C is the cold temperature of the noise sources.

ACKNOWLEDGMENT

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REFERENCES

[1] S. Mondal, R. Singh, A. I. Hussein, and J. Paramesh, "A 25–30 GHz fully-connected hybrid beamforming receiver for MIMO communication," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1275–1287, May 2018.

[2] H.-T. Kim et al., "A 28-GHz CMOS direct conversion transceiver with packaged 2 x 4 antenna array for 5G cellular system," *IEEE J. Solid-State Circuits*, vol. 53, no. 5, pp. 1245–1259, May 2018.

[3] B. Sadhu et al., "A 28-GHz 32-element TRX phased-array IC with concurrent dual-polarized operation and orthogonal phase and gain control for 5G communications," *IEEE J. Solid-State Circuits*, vol. 52, no. 12, pp. 3373–3391, Dec. 2017.

[4] Y. Yoon et al., "A highly linear 28GHz 16-element phased-array receiver with wide gain control for 5G NR application," in *Proc. IEEE Radio Freq. Integr. Circuits Symp. (RFIC)*, Jun. 2019, pp. 287–290.

[5] J. D. Dunworth et al., "A 28 GHz bulk-CMOS dual-polarization phased-array transceiver with 24 channels for 5G user and basestation equipment," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2018, pp. 70–72.

[6] J. Pang et al., "A 28-GHz CMOS phased-array transceiver based on LO phase-shifting architecture with gain invariant phase tuning for 5G new radio," *IEEE J. Solid-State Circuits*, vol. 54, no. 5, pp. 1228–1242, May 2019.

[7] R. Garg et al., "A 28-GHz beam-space MIMO RX with spatial filtering and frequency-division multiplexing-based single-wire IF interface," *IEEE J. Solid-State Circuits*, vol. 56, no. 8, pp. 2295–2307, Aug. 2021.

[8] R. Lu, C. Weston, D. Weyer, F. Buhler, D. Lambalot, and M. P. Flynn, "A 16-element fully integrated 28-GHz digital RX beamforming receiver," *IEEE J. Solid-State Circuits*, vol. 56, no. 5, pp. 1374–1386, May 2021.

[9] P. K. Khanna, Y. Zhao, M. Forghani, and B. Razavi, "A low-power 28-GHz beamforming receiver with on-chip LO synthesis," in *Proc. IEEE 49th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2023, pp. 501–504.

[10] D.-W. Kang and S. Hong, "A 4-bit CMOS phase shifter using distributed active switches," *IEEE Trans. Microw. Theory Techn.*, vol. 55, no. 7, pp. 1476–1483, Jul. 2007.

[11] A. Zolfaghari, A. Chan, and B. Razavi, "Stacked inductors and transformers in CMOS technology," *IEEE J. Solid-State Circuits*, vol. 36, no. 4, pp. 620–628, Apr. 2001.

[12] P. Khanna, "A Low-Power 28-GHz Beamforming Receiver with On-Chip Frequency Synthesizer," Ph.D. dissertation, Dept. Elect. Comput. Eng., UCLA, Los Angeles, CA, USA, 2023.

[13] 3GPP. (2019). *3GPP TR 21.915 V15.0.0 Release 15*. [Online]. Available: https://www.3gpp.org/ftp/Specs/archive/21series/21.915/

[14] Y. Zhao, M. Forghani, and B. Razavi, "A 20-GHz PLL With 20.9-fs Random jitter," *IEEE J. Solid-State Circuits*, vol. 58, no. 6, pp. 1597–1609, Jul. 2023.

[15] Y. Zhao, O. Memioglu, L. Kong, and B. Razavi, "A 56-GHz fractional-N PLL with 110-fs jitter," *IEEE J. Solid-State Circuits*, vol. 58, no. 1, pp. 57–67, Jan. 2023.

[16] Y. Chang, A. Manian, L. Kong, and B. Razavi, "An 80-Gb/s 44-mW wireline PAM4 transmitter," *IEEE J. Solid-State Circuits*, vol. 53, no. 8, pp. 2214–2226, Aug. 2018.

[17] A. Natarajan et al., "A fully-integrated 16-element phased-array receiver in SiGe BiCMOS for 60-GHz communications," *IEEE J. Solid-State Circuits*, vol. 46, no. 5, pp. 1059–1075, May 2011.

[18] J. Pang et al., "A power-efficient 24-to-71 GHz CMOS phased-array receiver utilizing harmonic-selection technique supporting 36dB inter-band blocker rejection for 5G NR," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2022, pp. 434–436.

[19] B. Sadhu et al., "A 24–30-GHz 256-element dual-polarized 5G phased array using fast on-chip beam calculators and magnetoelectric dipole antennas," *IEEE J. Solid-State Circuits*, vol. 57, no. 12, pp. 3599–3616, Dec. 2022.

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