A Millimeter-Wave CMOS Heterodyne Receiver With On-Chip LO and Divider

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***Abstract*—A heterodyne receiver performs frequency down-conversion in two steps to relax oscillator and divider speed requirements. The receiver incorporates new concepts such as a current-domain quadrature separation method, a broadband Miller divider based on a passive mixer, and an inductor nesting technique that significantly reduces the length of high-frequency interconnects. Fabricated in 90-nm CMOS technology, the circuit achieves a noise figure of 6.9 to 8.3 dB from 49 GHz to 53 GHz with a gain of 26 to 31.5 dB and I/Q mismatch of 1.6 dB/6.5°.**

***Index Terms*—Current-domain circuits, Miller divider, mm-wave communication, nested inductors, polyphase filter, RF receivers, 60-GHz transceivers.**

I. Introduction

THE unlicensed band around 60 GHz continues to present interesting prospects for high-data-rate applications such as high-definition video streaming. Furthermore, the short wavelength makes it possible to integrate one or more antennas along with the transceiver, thus obviating the need for expensive, millimeter-wave packaging and high-frequency electrostatic discharge (ESD) protection devices. Also, beamforming can considerably improve the link performance, thereby compensating for the poor radiation efficiency of on-chip antennas.

The heightened interest in this band for consumer applications has motivated research on the design of 60-GHz building blocks in CMOS technology. Examples include low-noise amplifiers (LNAs), mixers, oscillators, frequency dividers, and transmitter output stages [1]–[5]. As the next natural step, the building blocks must be integrated so as to form transceivers, a task that imposes many additional constraints on the design of both the building blocks and the architecture.

This paper describes the design of a millimeter-wave CMOS receiver that is architected so as to relax the performance required of the building blocks and ease the floor planning of the overall system [6]. Realized in 90-nm CMOS technology, the receiver includes an on-chip local oscillator (LO) and a frequency divider and achieves a noise figure of 6.9–8.3 dB with a power dissipation of 80 mW.

The next section of the paper reviews the device and architecture level challenges at these frequencies. Section III describes the receiver architecture and Section IV, the building blocks. Sections V and VI present the floor plan and the experimental results, respectively.

II. Device and Architecture Level Challenges

With the limited speed of MOSFETs, the use of inductors or transmission lines (T-lines) proves inevitable at millimeter-wave frequencies.[1] For example, simulations reveal that a resistively-loaded differential pair with a fanout of two exhibits a voltage gain of unity at roughly 15 GHz in 90-nm CMOS technology, suggesting that nodes running at higher frequencies must incorporate resonance. Unfortunately, the large footprint of inductors and T-lines leads to large dimensions for the building blocks and hence long high-frequency interconnects in the receiver.

It is interesting to contrast the present speed and interconnect issues at 60 GHz to those encountered in the late 1990s at 5 GHz. The nMOS f_T reaches 110 GHz in the 90-nm generation—about five times that of the 0.25-μm devices used in early 5-GHz designs [7], [8]. Also, the outer dimension of inductors for 60-GHz operation (50–100 μm) is only about a factor of two smaller than that of spirals used at 5 GHz 100–200 μm.[2] In other words, the frequency of operation has scaled by a factor of 12 but the transistor speed by roughly a factor of five and the interconnect lengths by roughly a factor of 0.5, making the design and floor planning of the receiver much more difficult.

Another point of contrast relates to the quality factor of inductors and varactors. Well-designed symmetric spiral inductors exhibit a Q of about 10 at 5 GHz, but, according to HFSS simulations, a Q of no more than 30 at 60 GHz. Attributed to substrate loss, this saturation of Q makes the design of millimeter-wave oscillators quite difficult. Since the Q does not scale by a factor of 12 from 5 GHz to 60 GHz, the tradeoffs between the phase noise, the tuning range, and the power dissipation become much more severe. Also, the Q of varactors appears to fall *below* that of inductors at millimeter-wave frequencies. For example, the measured data in [9] indicates $40 < Q < 160$ for 0.18-μm varactors at 2 GHz. Rough extrapolation therefore implies that $5 < Q < 20$ for 90-nm devices at 60 GHz.

The integration challenges that arise from limited transistor speeds and long interconnects manifest themselves in three critical tasks related to the local oscillator: 1) LO (I/Q) generation; 2) LO frequency division; and 3) LO distribution. To illustrate

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[1]Even if the speed of the transistors reaches sufficiently high levels, the limited voltage headroom still makes inductors and T-lines indispensable.

[2]At 5 GHz, stacked spirals with five to six turns were used [8] whereas at 60 GHz, it is preferable to have a single spiral with one or two turns. Thus, the outer dimensions differ by only a factor of two even the inductance values may bear a ratio of 10–15.

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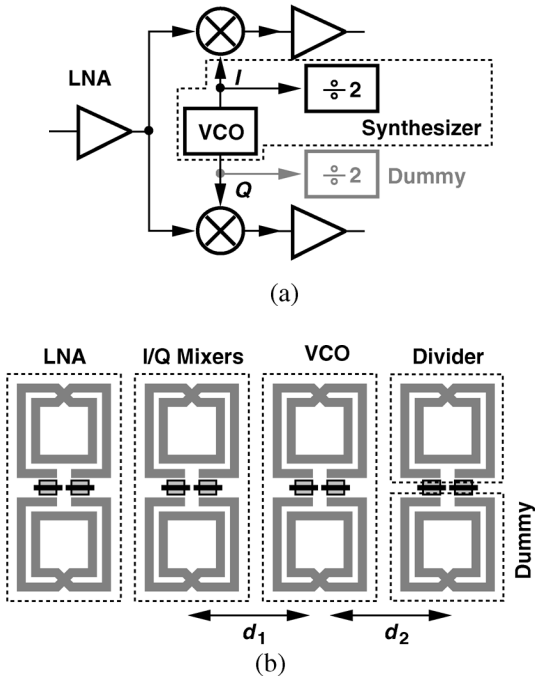


Fig. 1. (a) Direct-conversion receiver and (b) its floor plan.

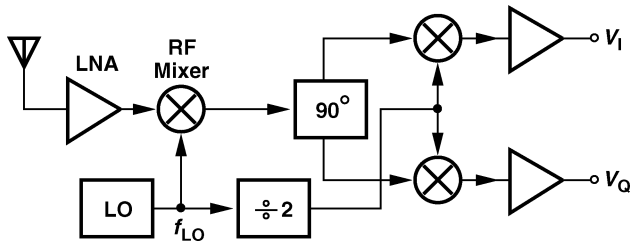


Fig. 2. Receiver architecture.

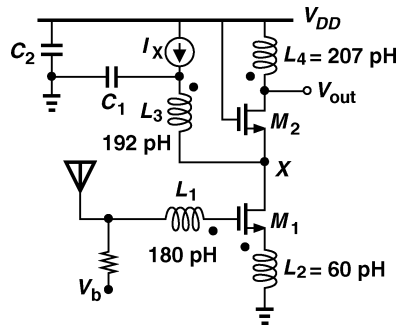


Fig. 3. LNA implementation.

these challenges, we consider a direct-conversion receiver architecture as a candidate. Shown in Fig. 1 along with its floor plan, such an architecture incorporates at least two inductors in the LNA, one in each mixer, two in the quadrature voltage-controlled oscillator (VCO), and at least one in the frequency divider. The dummy divider serves to retain the balance between the I and Q outputs. The generation of I and Q phases of the LO at 60 GHz entails two issues: (a) quadrature operation typically degrades the phase noise considerably (because *two* core oscillators consume power, they must operate away from resonance frequency of the tanks, and they do not improve each other's phase noise) and (b) for reasons mentioned above, the comparatively low tank Q results in serious design tradeoffs.

The second task, namely, LO frequency division, also proves problematic in this architecture. Injection-locked and Miller dividers typically suffer from a narrow lock range if designed for 60 GHz (Section IV).

The problem of LO distribution is also apparent from the floor plan of Fig. 1(b). The quadrature outputs of the VCO must travel a distance of d_1 to reach the I/Q mixer cores and d_2 to reach the divider cores, thus experiencing significant loss and mismatch. In fact, with no buffer following the VCO, the loss of these interconnects also degrades the phase noise.

One may wonder if these interconnects can be realized as low-loss T-lines having a controlled impedance and terminated properly at the destination. Since the characteristic impedance of on-chip T-lines hardly exceeds a few hundred ohms, such an approach would *load* the VCO with a low resistive component, drastically raising the noise floor or even prohibiting oscillation. A buffer must therefore follow the VCO in this case.

The use of a VCO buffer is also required by another effect: in a direct-conversion receiver, strong in-band interferers can leak from the RF to the LO port of the downconversion mixers, thus injection-pulling the LO in the absence of a buffer. However, the use of a quadrature buffer in the architecture of Fig. 1 translates to two additional inductors and much greater difficulty in floor planning.

III. Receiver Architecture

The issues described in Section II suggest that a receiver architecture operating with lower LO frequencies is more desirable. It is possible to choose the LO frequency, $f_{\rm LO}$, equal to $f_{\rm in}/2$ or $f_{\rm in}/3$, where $f_{\rm in}$ is the received signal frequency, and use frequency doublers or triplers to obtain the required value. Unfortunately, if realized in CMOS technology, this type of frequency multiplication suffers from small output swings and hence a phase noise much higher than a factor of two or three. Furthermore, I and Q separation after frequency multiplication proves quite difficult.

Fig. 2 depicts the receiver architecture used in this work. In a manner similar to that in [10], the receiver mixes the input with a nominal LO frequency of 40 GHz, generating an intermediate frequency (IF) of 20 GHz. The IF signal is then separated to quadrature phases and mixed with $f_{\rm LO}/2$ to produce the baseband outputs. With $f_{\rm LO} = (2/3)f_{\rm in}$, an input band of B requires an LO range of $(2/3)B$. Also, the image bandwidth is equal to $B/3$. (It can be proved that if $f_{\rm LO} = \alpha f_{\rm in}$, then the image bandwidth is equal to $(2\alpha - 1)B$.) (Due to device modeling inaccuracies, the fabricated prototype yields a maximum $f_{\rm LO} \approx 35$ GHz, allowing an input frequency of 53 GHz.)

The heterodyne architecture of Fig. 2 greatly simplifies the three LO-related tasks mentioned in Section II: 1) generation occurs at 40 GHz with no need for quadrature phases; 2) frequency division also occurs at 40 GHz, permitting a broadband design (Section IV); and 3) distribution of the differential 40-GHz LO is much simpler than that of quadrature 60-GHz components. Note that no LO buffer is necessary as interferers in the vicinity

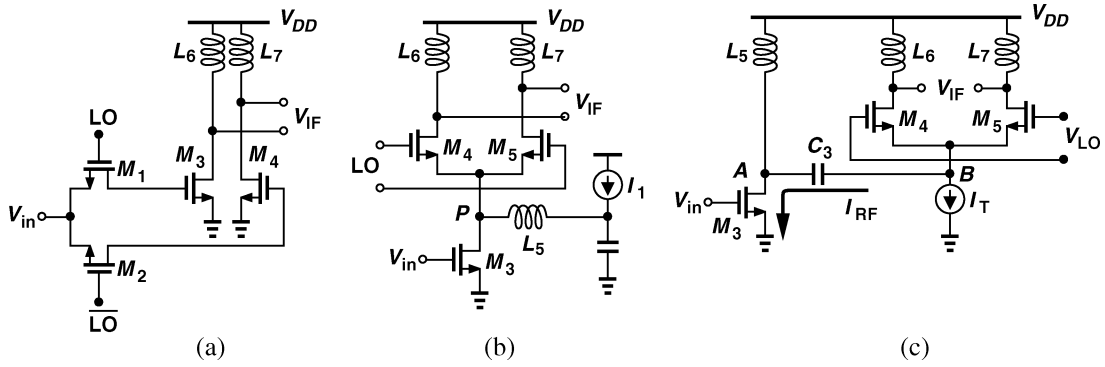


Fig. 4. (a) Passive mixer. (b) Active topology using auxiliary current path. (c) Active topology with capacitive coupling.

of 40 GHz are suppressed by the selectivity of the front-end (including the antenna).

Unlike typical designs, the receiver performs quadrature separation in the signal path rather than in the LO path. As explained in Section IV, this choice eases the design of the 40-GHz divide-by-two circuit, hence lowering the risk to the operation of the overall receiver.

It is possible to divide $f_{\rm LO}$ by four and drive the IF mixers with the resulting components [11]. This approach, however, places the image closer to the signal, yielding a lower image rejection ratio.

IV. Building Blocks

This section describes the design of the receiver building blocks. In the design process, inductors and critical interconnects are simulated in HFSS and ported as *RLC* models into circuit simulations. For transistors, the BSIM4 models provided by the foundry are used.

A. Low-Noise Amplifier

Fig. 3 shows the realization of the LNA. With the available f_T of 90-nm nMOS devices, an inductively-degenerated cascode provides a lower noise figure and higher gain than a common-gate stage [1]. However, the capacitances introduced by M_1 and M_2 create a pole on the order of $f_T/2$ at node X, thereby shunting the RF current to ground and raising the noise contribution of M_2. Thus, inductor L_3 is added to resonate with the capacitance at this node [12]. Also, in a manner similar to the mixer design in [1], current source I_X ($\approx 0.25 I_{D1}$) allows greater flexibility in the noise and gain optimization of the stage. The magnetic coupling factors indicated between L_1 and L_2 and between L_3 and L_4 result from "nesting" these structures and are explained in Section V. HFSS simulations predict Q values ranging from 15 to 20 for the LNA inductors.

Under resonance condition, L_3 exhibits an equivalent parallel resistance of 800 Ω, allowing M_2 to carry most of the RF drain current of M_1. Simulations indicate that the addition of L_3 and I_X reduces the LNA noise figure from 5.2 dB to 4.4 dB and raises the voltage gain from 11 dB to 13.8 dB. The circuit draws a supply current of 8 mA.

As a single-ended circuit, the LNA is quite sensitive to parasitics in series with the bypass capacitors C_1 and C_2. The return path through these capacitors to the ground must therefore exhibit a sufficiently small inductance (< 20 pH) to avoid shifting the resonance frequency or causing instability. This issue is addressed in Section V.

With $L_4 = 207$ pH in Fig. 3, the LNA can tolerate a total capacitance of 27 fF at its output node. Transistor M_2 contributes about 12 fF, leaving approximately 15 fF (corresponding to $W/L = 8\ \mu$m$/0.1\ \mu$m) for the input capacitance of the subsequent mixer.

B. RF Mixer

The RF mixer can be realized as either a passive structure followed by an amplifier or an active topology. Shown in Fig. 4(a) and simulated at $f_{\rm in} = 60$ GHz and $f_{\rm IF} = 20$ GHz, the former provides a noise figure of 12.7 dB and a voltage conversion gain of 10.5 dB. However, the circuit presents a low impedance to the LNA, lowering the gain of the LNA/mixer cascade by 5 dB.[3]

A candidate for active mixers operating at millimeter-wave frequencies is shown in Fig. 4(b) [1]. Here, inductor L_5 resonates with the capacitance at node P while providing about half of the bias current of M_3. As a result, M_4 and M_5 switch more abruptly, raising the conversion gain and lowering the noise figure. Unfortunately, due to its small dimensions, M_3 incurs a large mismatch with respect to I_1, thus creating large variations in the current flowing from the switching pair. The topology depicted in Fig. 4(c) [13] avoids this issue by isolating the bias current of $M_4 - M_5$ from that of the input transconductor. In this design, optimization of noise figure and gain yields $I_{D3} = 8.5$ mA whereas $I_T = 0.75$ mA, revealing that the conventional active mixer (with the switching pair carrying the same current as the input device) is far from optimum. The circuit achieves a noise figure of 12.5 dB and a voltage conversion gain of 10.2 dB, similar to those of its passive counterpart in Fig. 4(a), but with a higher input impedance. As a result, the LNA/mixer cascade exhibits a gain of 24 dB and a noise figure of 5.8 dB.

As a single-balanced mixer, the topology of Fig. 4(c) can produce a large LO component at the output, potentially desensitizing the IF mixers. The load inductors, however, create resonance at 20 GHz, attenuating the LO feedthrough to acceptably low levels. Also, the small ratio of I_T/I_{D3} reduces the LO feedthrough by the same factor.

[3]The capacitances of the transistors and the loss associated with the channel resistance of M_1 and M_2 lower the gain of the cascade.

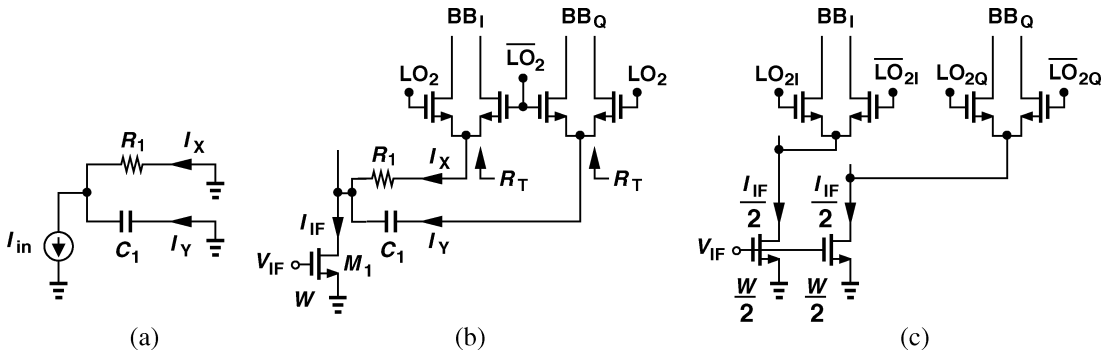


Fig. 5. (a) Current-domain quadrature separation. (b) Implementation in mixers. (c) Comparison with conventional quadrature mixers.

C. IF Mixers

As mentioned in Section III, the receiver performs quadrature separation in the IF path rather than in the LO path so as to simplify the design of the divider. Voltage-mode *RC-CR* networks are commonly used for quadrature generation, but they are fundamentally ill-suited to current-generating transistor stages and must often be preceded with voltage buffers. Furthermore, such networks introduce a loss of at least 3 dB and significant noise.

This paper presents the concept of current-mode quadrature separation as a technique that can readily follow voltage-to-current converter devices. Consider the network shown in Fig. 5(a), where

$$I_X = \frac{1}{R_1 C_1 s + 1} I_{\text{in}} \tag{1}$$

$$I_Y = \frac{R_1 C_1 s}{R_1 C_1 s + 1} I_{\text{in}}. \tag{2}$$

It follows that I_X and I_Y bear a phase difference of 90° at all frequencies and exhibit equal amplitudes at $s = j\omega_1 = j/(R_1 C_1)$. The IF mixers can thus be configured as depicted in Fig. 5(b), where the switching devices are simply driven by LO_2 and $\overline{\text{LO}_2}$ rather than by the quadrature phases of LO_2.[4]

In contrast to voltage-mode RC-CR networks, this configuration, in principle, suffers from no signal loss. This can be understood with the aid of the conventional topology shown in Fig. 5(c), which is constructed so as to exhibit the same input capacitance as the circuit in Fig. 5(b). We note that this topology too feeds a current of $I_{\text{IF}}/2$ to each switching pair. That is, notwithstanding the parasitics of R_1 and C_1, the addition of the current-mode phase separation circuit does not alter the conversion gain from V_{IF} to BB_I or BB_Q. (The parasitic capacitances of $R_1 \approx 400\ \Omega$ and $C_1 \approx 35$ fF amount to about 4 fF, introducing an impedance of 2 kΩ at 20 GHz and hence negligibly impacting the performance.)

Two issues in the circuit of Fig. 5(b) merit consideration. First, the thermal noise of R_1 does corrupt the IF current. It can be shown that the noise current of R_1 splits equally between I_X and I_Y at $\omega_1 = 1/(R_1 C_1)$. With $R_1 \approx 400\ \Omega$, the corruption reaches 3.2 pA/$\sqrt{\text{Hz}}$. Dividing this value by $g_{m1}/2 \approx (400\ \Omega)^{-1}$, we obtain an input-referred component equal to 1.3 nV/$\sqrt{\text{Hz}}$, which is negligible with respect to the output noise of the LNA/mixer cascade.

[4]LO_2 denotes the second LO, namely, the output of the divide-by-two circuit.

The second issue is that the right terminals of R_1 and C_1 terminate into a finite impedance R_T, thereby generating an imbalance between I_X and I_Y. It can be shown that such a termination resistance gives rise to a phase mismatch of $\tan^{-1}(R_T/R_1)$ and an amplitude mismatch of $R_T/(4R_1)$. This issue is addressed below.

Fig. 6(a) shows the complete realization of the IF mixers. As in the RF mixer, the bias currents of the input transconductance devices $M_1 - M_2$ are isolated from those of the switching devices. Capacitors C_3 and C_4 are added so as to suppress the imbalance resulting from R_T in Fig. 5(b). Illustrated in simplified form in Fig. 6(b), the idea is to rotate each component with the aid of the complement of its quadrature phase. For example, C_4 couples a fraction of I_X to $\overline{I_Y}$ and vice versa, rotating them toward each other. Simulations indicate that the baseband phase mismatch and gain mismatch drop by 25° and 2.5 dB, respectively, after C_3 and C_4 are inserted.

The quadrature balance in the IF mixer is somewhat process- and temperature-dependent, both because the product $R_1 C_1$ may vary (as in voltage-mode *RC-CR* networks) and because the correction provided by C_3 and C_4 assumes tracking between R_T and R_1. These dependencies as well as random mismatches dictate I/Q calibration for high-order modulation schemes such as 16QAM and 64QAM—a task necessary even in 5-GHz transceivers [14].

The circuit of Fig. 6(a) draws a total supply current of 13 mA while providing a voltage conversion gain of 12 dB with a noise figure of 14 dB.

D. Frequency Divider

The divide-by-two circuit in the architecture of Fig. 2 is driven by the 40-GHz LO while driving the two IF mixers. As such, the divider must satisfy difficult requirements: it must: 1) drive a total capacitance corresponding to $W/L = 40\ \mu\text{m}/0.1\ \mu\text{m}$ while presenting a small capacitance to the LO; 2) provide relatively large output swings to effect abrupt switching in the IF mixers; 3) employ no input or output buffers as such buffers would require additional inductors; and 4) use no more than one inductor to allow a reasonable floor plan. The last condition rules out the possibility of quadrature outputs.

Since injection-locked dividers suffer from a narrow lock range, posing a risk to the overall receiver, a Miller regenerative topology was adopted. Shown in Fig. 7 along with the LO, the

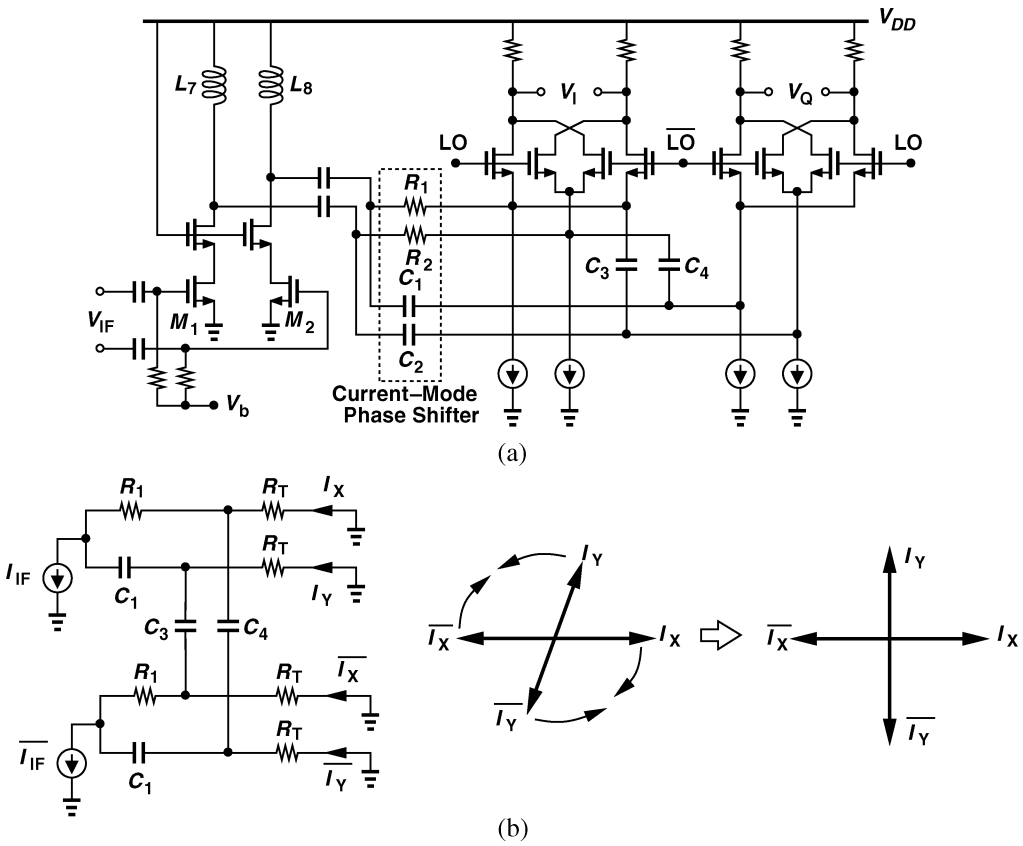


Fig. 6. (a) IF mixer implementation. (b) Imbalance correction.

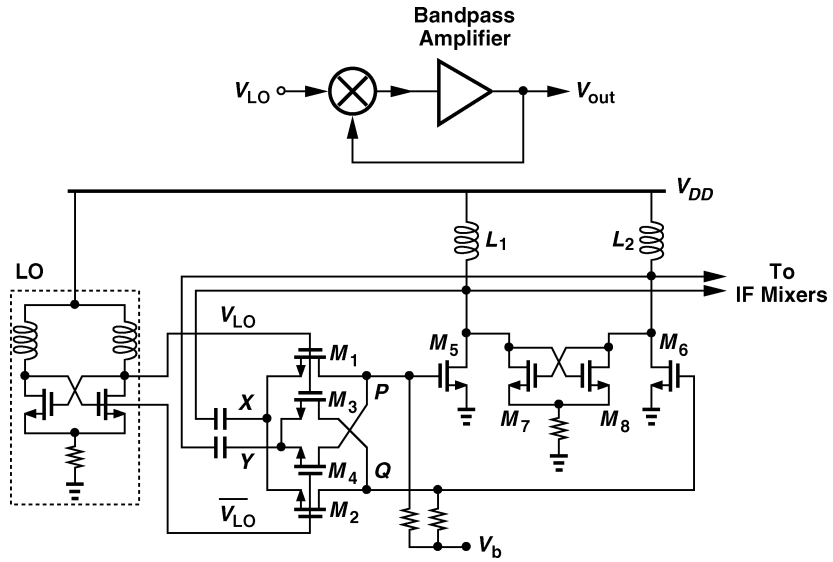
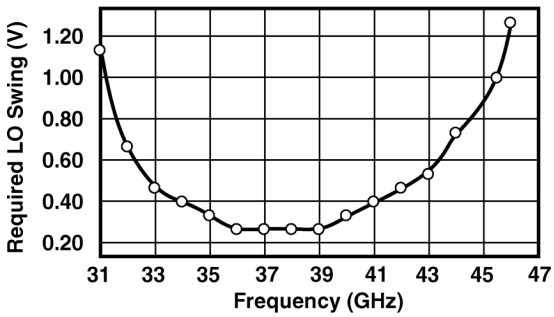


Fig. 7. Divider implementation along with LO.

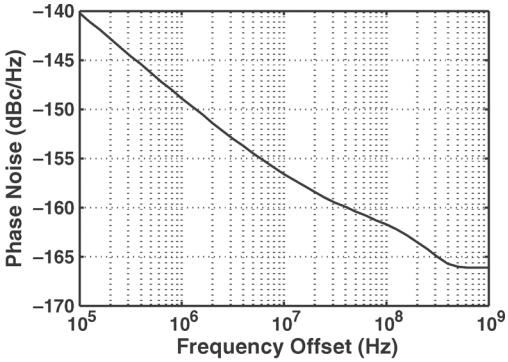
circuit incorporates a passive mixer, $M_1 - M_4$, followed by a bandpass amplifier consisting of $M_5 - M_8$ and inductors L_1 and L_2. For correct operation, the divider must exhibit a loop gain of unity or higher, proper suppression of the component at $3f_{\rm LO}/2$, and sufficient phase shift [15].[5] To minimize the loss of the passive mixer, the LO phases swing above the supply voltage so as to provide an overdrive voltage of about 900 mV for $M_1 - M_4$ even though their drains reside at a common-mode level equal to $V_{\rm GS5,6}$.

The passive mixer loads the bandpass amplifier both capacitively and resistively. As LO and $\overline{\rm LO}$ cross, a temporary resistive path is created between X and Y through the channel resistance of $M_1 - M_4$. Moreover, the capacitance at node P

[5]Early simulations showed that an active mixer with inductive loads [15] would suffer from a relatively narrow lock range because of the small phase shift around the loop.



(a)



(b)

Fig. 8. Simulated (a) lock range, and (b) phase noise of divider.

(and at node Q) is periodically switched between X and Y, introducing an equivalent resistance between these nodes. Due to the resistive loading, the basic amplifier consisting of $M_5 - M_6$ and $L_1 - L_2$ provides only a moderate gain and hence a narrow lock range. The addition of the cross-coupled pair raises the gain by 8 dB while avoiding self-oscillation. (The robustness of this approach was later assessed by varying the supply voltage of the fabricated receiver from 1.2 V to 1.8 V and observing no failure.)

Producing a differential peak-to-peak output swing of 2.5 V with a supply current of 14 mA, the divider drives a load of $W/L = 40\ \mu$m$/0.1\ \mu$m while presenting a capacitance equivalent to $W/L = 12\ \mu$m$/0.1\ \mu$m to each phase of the LO. Note that, even if more inductors are allowed, Miller dividers cannot easily generate quadrature outputs—especially if a wide lock range is desired. The LO draws 8 mA.

Fig. 8(a) plots the required peak-to-peak single-ended LO swing for proper divider operation as a function of the LO frequency. With a swing of about 1 V_{pp} provided by the on-chip oscillator, the divider achieves a lock range of 31.5 to 45.5 GHz.

Fig. 8(b) depicts the simulated phase noise of the divider with an ideal input sinusoid at 40 GHz, revealing values well below the phase noise of oscillators. This profile rises by about 7 dB as the circuit operates near the edges of the lock range. It is interesting to note that the output phase noise is dominated by the flicker noise contribution of the passive mixer switches for offset frequencies up to 100 MHz. Owing to the large signal excursions at their drain and source terminals, these transistors remain in the saturation region for about 30% of the LO cycle, thus generating significant flicker noise. Also, the 10-dB/dec roll-off suggests a simple upconversion of this noise rather than frequency modulation by it. Indeed, a hard limiter following the divider shifts the profile down by about 5 dB, confirming that the flicker noise introduces mostly amplitude modulation.

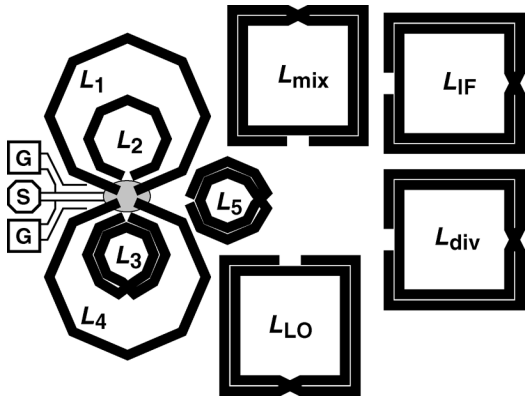


Fig. 9. Receiver floor plan.

V. Receiver Floor Plan

While affording lower operation frequencies for the LO and the divider, the heterodyne architecture used in this work still incorporates nine inductors. The floor plan of the receiver must therefore be designed carefully so as to minimize the length of 60-GHz interconnects, possibly sacrificing those at 40 GHz, and the length of 40-GHz interconnects, possibly sacrificing those at 20 GHz. The critical interconnects include both signal lines and ground return paths, especially for the single-ended front end.

The LNA of Fig. 3 employs four inductors whose outer dimensions lie in the range of 40 μm to 100 μm. If placed side by side, these structures result in 60-GHz interconnects as long as 70 μm. This length should be compared, e.g., to the total length of the degeneration inductor L_2 ($\approx 125\ \mu$m) to appreciate its relative significance.

This paper introduces "nested inductors" [16] as a means of shortening high-frequency interconnects. Illustrated in the floor plan of Fig. 9, the idea is to place L_2 inside L_1, and L_3 inside L_4, thereby confining all but one of the 60-GHz interconnects to the gray region. (The input signal is applied through a GSG pad frame on the left-hand side and carried over a microstrip to the LNA input.) The magnetic coupling that results from nesting gives rise to a mutual coupling factor of about 0.2, altering the input match and the transfer function slightly if the polarity of the coupling is chosen properly. The inductor values are then adjusted to recenter the matching and resonance characteristics. Fig. 10 quantifies these concepts by plotting the simulated S_{11} with no coupling and original choice of L_1 and L_2, and with a coupling factor of 0.17 and adjusted values of the two inductors. (Field simulations suggest negligible change in the Q as a result of nesting.)

The only 60-GHz line that travels outside the gray region in Fig. 9 corresponds to the connection to L_5 in the mixer of Fig. 4(c). Operating as a high impedance, L_5 plays a less critical role than L_1, L_2, and L_4 in the LNA. Nevertheless, the value of L_5 is chosen less than the required amount to account for the interconnect inductance.

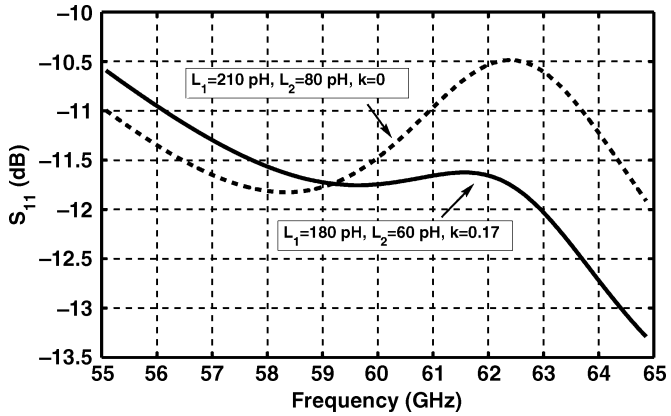


Fig. 10. Simulated S_{11} for $k = 0$ and $k = 0.17$.

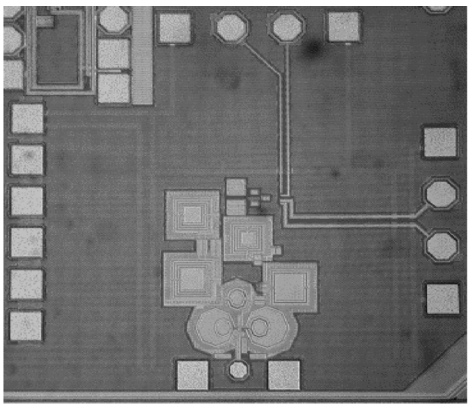


Fig. 11. Receiver die photograph.

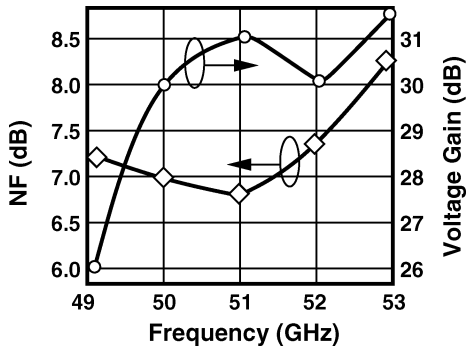


Fig. 12. Measured noise figure and voltage gain.

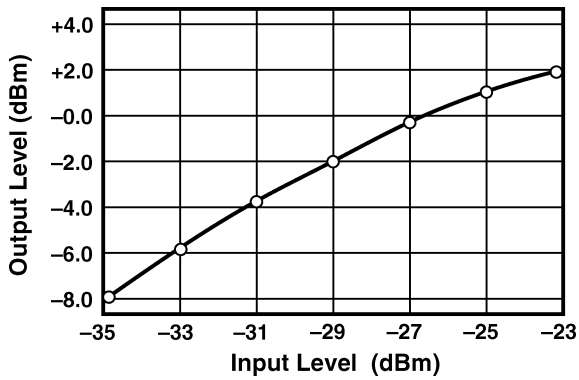


Fig. 13. Measured compression behavior of the receiver.

The ground return paths for the LNA and the input stage of the mixer are provided through the gray region in Fig. 9. With lengths and widths of about 20 μm and 5 μm, respectively, these paths incur a parasitic inductance of approximately 10 pH. The bypass capacitors (C_1 and C_2 in Fig. 3) are placed atop the input ground plane to minimize their series inductance.

The remaining inductors naturally fall into the places depicted in Fig. 9. Worth mentioning is that $L_{\rm LO}$ must be located far from the LNA input inductors so that the LO coupling does not desensitize the LNA.

VI. Experimental Results

The receiver has been fabricated in 90-nm digital CMOS technology and tested on a high-frequency probe station. Fig. 11 shows the die photograph, indicating an active area of approximately 300 μm $\times$ 500 μm. Due to modeling inaccuracies of the LO inductor and possibly transistor capacitances, the LO operates at a maximum frequency of 35 GHz. The receiver has thus been characterized for an input frequency range of 49 to 53 GHz. The LO does not incorporate varactors. Thus, to allow characterization of the receiver for a meaningful input frequency range, the LO frequency is varied by varying its supply voltage and also placing an external conductive plate atop the LO inductor [17].

Constructed around a probe station, the test setup applies an input through a coplanar waveguide probe from either an Agilent V-band signal generator (85100V) or a Noisecom V-band noise source to the device under test. The baseband output is monitored on a spectrum analyzer (for gain and image measurements), an oscilloscope (for phase/gain mismatch measurements), or an Agilent noise figure meter (8970B). The loss of the input probe (≈ 1 dB) is taken into account.

Fig. 12 plots the measured noise figure and voltage gain of the circuit. The maximum noise figure is about 2 dB higher than expected and the gain about 5 dB lower than expected. This is attributed to the lower-than-expected Q of the inductors used in the LNA. Fig. 13 plots the compression behavior of the receiver, revealing a 1-dB compression point of about -25.5 dBm. Simulations indicate that the compression occurs at the output of the IF mixers.

Shown in Fig. 14 is the image rejection ratio (IRR) across the image band. (As explained in Section III, the image band is 1/3 as wide as the signal band in this architecture.)

Fig. 15(a) plots the gain and phase mismatch measured in the baseband and Fig. 15(b) shows typical waveforms in response to a sinusoidal RF signal. It is observed that the current-mode quadrature separation and the additional correction technique illustrated in Fig. 6(b) provide reasonable I/Q balance.

Fig. 16 shows the measured phase noise of the divider as observed at the baseband output. The phase noise reaches -101 dBc/Hz at 1-MHz offset, indicating an LO phase noise of about -95 dBc/Hz.

TABLE I
RECEIVER PERFORMANCE SUMMARY

	Receiver in [17]	Receiver in [18]	This Work
Noise Figure	5−6.7 dB	10.4 dB	6.9−8.3 dB
Voltage Gain	38−40 dB	11.8 dB	26−31.5 dB
Frequency Range	58−64 GHz	57−63 GHz	49−53 GHz
1−dB Compression Point	−36 dBm	−15 dBm	−25.5 dBm
LO Leakage to Input	NA	NA	−47 dBm
Image Rejection ratio	30 dB	NA	44.5 dB
I/Q Mismatch	1 dB/4°	NA	1.6 dB/6.5°
LO Phase Noise @ 1−MHz Offset	−90 dBc/Hz	−86 dBc/Hz	−95 dBc/Hz
Power Dissipation	450 mW *	77 mW	80 mW
Supply Voltage	2.7 V	1.2 V	1.8 V
Active Chip Area	NA	~3 mm^2	0.15 mm^2
Technology	200−GHz BiCMOS	0.13−um CMOS	90−nm CMOS

* This value excludes the synthesizer power dissipation.

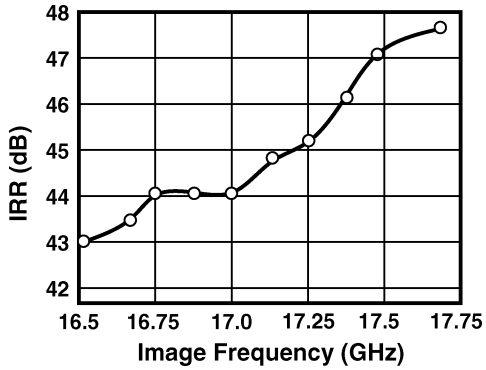
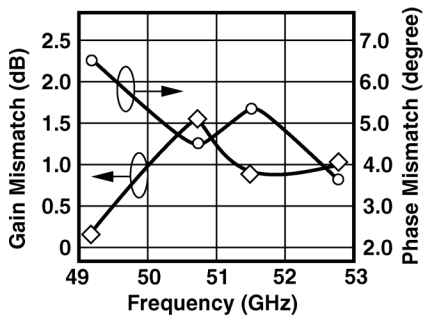
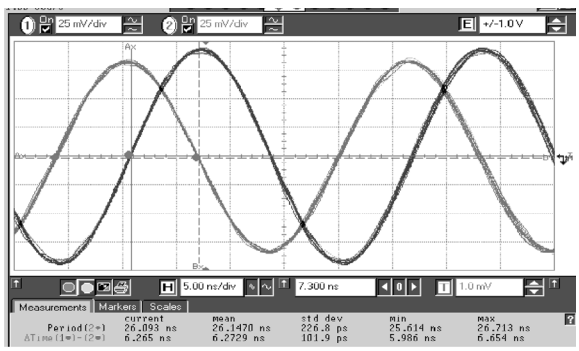


Fig. 14. Measured image rejection ratio.



(a)



(b)

Fig. 15. (a) Gain and phase mismatch. (b) Typical baseband waveforms (horizontal scale: 5 ns/div., vertical scale: 25 mV/div.).

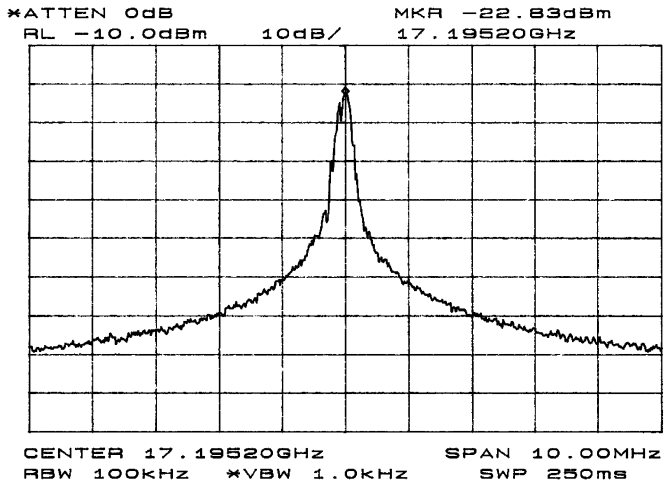


Fig. 16. Measured output spectrum of divider while it is driven by LO.

Table I compares the performance of this receiver with the 60-GHz BiCMOS receiver reported in [18] and the 60-GHz CMOS receiver described in [19].[6]

VII. CONCLUSION

Today's development of 60-GHz CMOS transceivers is reminiscent of the challenges that faced 5-GHz wireless LAN circuits in the late 1990 s: the intrinsic speed of the then-available transistors was inadequate, and no significant commercial value had been identified. Nonetheless, if 60-GHz transceivers follow the fate of their 5-GHz counterparts, both of these issues will be resolved in the near future.

This paper contends that heterodyne transceivers better lend themselves to integration at millimeter-wave frequencies than direct-conversion architectures do. Proposing various circuit techniques such as capacitively coupled active mixers, current-domain quadrature separation, and a Miller frequency divider

[6]While designed for a supply voltage of 1.2 V, the prototype had to be tested with $V_{DD} = 1.8$ V because the IF mixer loads resistors had erroneously been laid out with twice the nominal value and hence would drive the mixer transistors into the triode region at the nominal supply voltage.

using a passive mixer, this work demonstrates the highest level of integration for CMOS millimeter-wave receivers.

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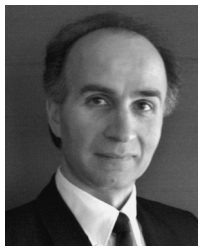

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