

Relation Between INL and ACPR of RF DACs

Seyed-Mehrdad Babamir^{1b}, *Member, IEEE*, and Behzad Razavi^{1b}, *Fellow, IEEE*

Abstract—The integral nonlinearity of digital-to-analog converters manifests itself as adjacent-channel power in RF transmitters. This paper derives compact equations relating these two quantities and verifies the results by simulations. Both current-steering and switched-mode architectures are analyzed.

Index Terms—RF DAC nonlinearity, phase distortion, AM/AM and AM/PM conversion, ACPR relation, INL.

I. INTRODUCTION

DIGITAL RF transmitters have become popular for their numerous advantages over their analog counterparts [1], [2], [3], [4], [5], [6], [7], [8], [9]. A digital transmitter (TX) dispenses with most of the analog functions and contains only one analog port, namely, its output. Of course, such an approach relies on a high-speed, high-linearity digital-to-analog converters (DACs). The DAC's output settling must be commensurate with the carrier frequency, and its linearity is dictated by the tolerable distortion of the desired signal and/or the adjacent-channel power ratio (ACPR). The latter proves particularly challenging in cellular applications such as the Long-Term Evolution (LTE) standard.

The nonlinearity and spurious-free dynamic range (SFDR) of DACs have been studied extensively [10], [11], [12], [13], [14], [15]. This paper focuses on the relation between the DAC nonlinearity and ACPR. The objective is to provide compact equations that help the designer decide how to select the DAC unit cells and how much residual integral nonlinearity (INL) can be tolerated after correction techniques such as predistortion are applied.

Section II deals with the nonlinearity analysis of current-steering DACs and Section III relates their INL and ACPR. Section IV studies these DACs' behavior if the input is approximated by white noise, and Section V examines the effect of phase distortion. Section VI repeats the computation for switched-mode architectures.

II. NONLINEARITY OF CURRENT-MODE RF DACS

In this section, we focus on RF DACs that employ current steering so as to deliver a high power to the antenna [5], [6], [7], [8]. Figure 1 shows a common topology for a unit cell of the DAC [7] where the cascode transistors allow large output voltage swings without stressing M_1 and M_2 . The principal

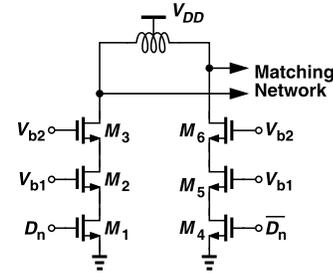


Fig. 1. Typical unit cell used in RF DACs.

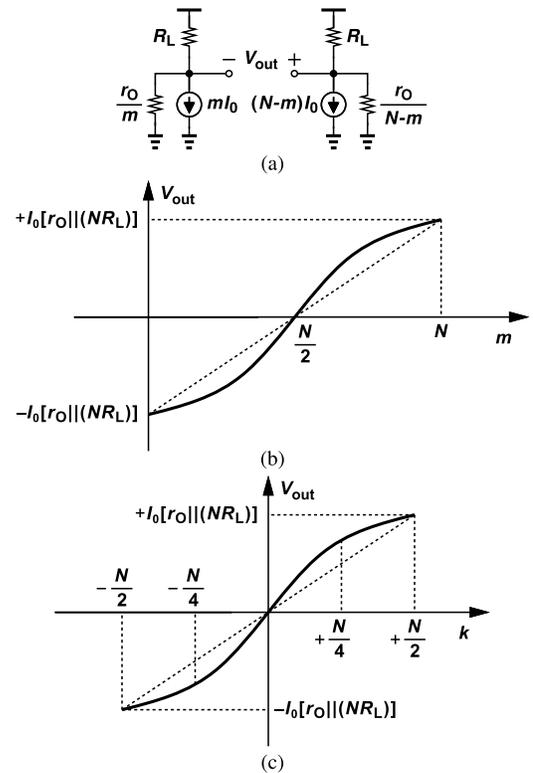


Fig. 2. (a) Baseband equivalent of a DAC, (b) its characteristic, and (c) the characteristic shifted by $N/2$.

source of INL in this arrangement is the finite output resistance of each unit. The resulting nonlinearity is typically excessive, requiring some form of correction, e.g., predistortion [16].

As a design example, we choose 256 unit cells each having a current of 1.54 mA and an output resistance of 1.2 k Ω . We also assume the matching network transforms the 50- Ω antenna resistance to 3.5 Ω . Such a design delivers a peak power of about 20 dBm.

For our analysis in subsequent sections, we wish to approximate the RF DAC static characteristic by a polynomial. To this end, we first consider a baseband DAC (without upconversion). The INL is simulated by applying a digital ramp to the input,

Manuscript received 29 April 2022; revised 14 July 2022 and 5 August 2022; accepted 20 August 2022. Date of publication 5 September 2022; date of current version 29 September 2022. This article was recommended by Associate Editor J. Zhao. (Corresponding author: Seyed-Mehrdad Babamir.) Seyed-Mehrdad Babamir is with Broadcom Inc., San Diego, CA 92127 USA (e-mail: smbabamir@ucla.edu).

Behzad Razavi is with the Department of Electrical Engineering, University of California, Los Angeles, Los Angeles, CA 90095 USA. (e-mail: razavi@ee.ucla.edu).

Color versions of one or more figures in this article are available at <https://doi.org/10.1109/TCSI.2022.3201491>.

Digital Object Identifier 10.1109/TCSI.2022.3201491

1549-8328 © 2022 IEEE. Personal use is permitted, but republication/redistribution requires IEEE permission.

See <https://www.ieee.org/publications/rights/index.html> for more information.

finding the output values, passing a straight line between the end points of the characteristic, and computing the difference between the two.

A. Baseband Model

Assuming that the DAC employs N identical units and that N is an even number, let us begin with the equivalent circuit depicted in Fig. 2(a), where each unit is modeled by a current source equal to I_0 and an output resistance equal to r_O . The total differential load resistance presented by the output matching network is $2R_L$. We assume m current switches are active on the left and $N - m$ on the right. Since this DAC is differential, V_{out} is an odd function of m around $N/2$, a reasonable assumption in view of the small mismatches between the two sides. It can be shown that

$$V_{out} = -I_0 R_L \frac{(N - 2m)r_O^2}{(mR_L + r_O)[(N - m)R_L + r_O]}, \quad (1)$$

hence

$$V_{out}(m = 0) = -I_0 R_L \frac{Nr_O^2}{r_O(NR_L + r_O)} \quad (2)$$

$$= -I_0 \frac{(NR_L) \times r_O}{nR_L + r_O} \quad (3)$$

$$= -I_0[r_O || (NR_L)], \quad (4)$$

and $V_{out}(m = N) = I_0[r_O || (NR_L)]$ due to the odd symmetry around $m = N/2$ [Fig. 2(b)]. Since the INL and the slope of this characteristic are invariant to m , we shift the plot to the left by $N/2$ and introduce a new variable $k = m - N/2$ [Fig. 2(c)].

We surmise that this symmetric characteristic can be approximated by a third-order polynomial of the form

$$V_{out} = \alpha_1 k + \alpha_3 k^3. \quad (5)$$

For $k = \pm N/2$, we have

$$\pm \alpha_1 \frac{N}{2} \pm \alpha_3 \frac{N^3}{8} = \pm I_0[r_O || (NR_L)]. \quad (6)$$

We must impose one more constraint, e.g., the value of the polynomial must be equal to that of the actual characteristic at $m = N/4$ and $m = 3N/4$ in Fig. 2(b) or, equivalently, at $k = -N/4$ and $k = +N/4$ in Fig. 2(c). It follows that

$$\alpha_1 \left(\frac{N}{4}\right) + \alpha_3 \left(\frac{N}{4}\right)^3 = \frac{-I_0 R_L (N/2) r_O^2}{\left(\frac{N}{4} R_L + r_O\right) \left(\frac{3N}{4} R_L + r_O\right)}. \quad (7)$$

Equations (6) and (7) must be solved to obtain α_1 and α_3 .

The polynomial approximation readily allows us to calculate the maximum INL. For an input range from $k = -N/2$ to $+N/2$, we pass a straight line through the end points, subtract it from the polynomial, and differentiate the result with respect to k . It follows that $\text{INL}_{max} = |\alpha_3| N^3 / 12\sqrt{3}$. The maximum differential output voltage is equal to $\pm \alpha_3 (N/2)^3 \pm \alpha_1 (N/2)$, which is close to $\pm \alpha_1 (N/2)$ if the peak INL is less than about 4%. We normalize INL_{max} to this value:

$$\text{INL}_{max,n} = \frac{1}{6\sqrt{3}} \left| \frac{\alpha_3}{\alpha_1} \right| N^2. \quad (8)$$

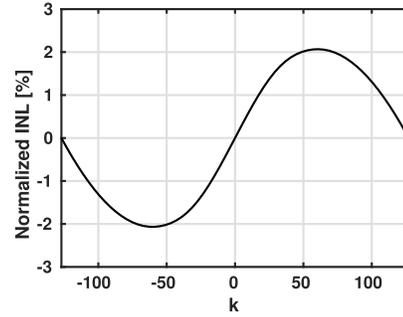


Fig. 3. Normalized INL as a function of k .

For the assumption $|\alpha_3| (N/2)^3 \ll |\alpha_1| (N/2)$ to be valid, we have $|\alpha_3/\alpha_1| N^2 / (6\sqrt{3}) \ll 4 / (6\sqrt{3}) \approx 0.38$, concluding that $\text{INL}_{max,n}$ should be less than about 3.8%. For the unit cell design values mentioned above, we have $\alpha_1 = 5.3 \times 10^{-3}$ V and $\alpha_3 = -1.7 \times 10^{-8}$ V for $N = 256$. In this case, the peak INL is about 2.1%. These values are computed by first finding the unit cell's r_O ($= 1.2$ k Ω) and then using Eqs. (6) and (7). Figure 3 plots the normalized INL of this DAC.

The effect of random mismatches within the DAC typically falls well below that due to the output impedance. Since large widths must be chosen for the unit output resistance so as to deliver the desired power, the matching among them (which is proportional to the transistors' channel area) is generally precise. As an example, an 8-bit design in 28-nm technology providing a +20-dBm output requires a unit width of roughly 45 μm , which exhibits a threshold voltage mismatch, $\Delta V_{TH} = A_{V_{TH}} / \sqrt{WL}$ [17], of 3.5 mV with $A_{V_{TH}} = 4$ mV \cdot μm . We have designed an 8-bit DAC using the cell shown in Fig. 1 for an output power of +20-dBm. We have $W_{1,4} = 45$ μm , $W_{2,5} = 14$ μm . Figure 3 plots the simulated INL profile of the circuit, revealing a maximum value of 2.1%. Moreover, Monte Carlo simulations indicate that the INL rises to 2.3% when the mismatches are included. The above transistor-level simulations have been carried out with transition times of 20 ps for D_n and \overline{D}_n . No glitches are observed at the output.

According to transistor-level simulations, the memoryless model of Fig. 2(a) is fairly accurate for carrier frequencies up to several gigahertz in 28-nm technology. Beyond this range, it is necessary to proceed with the AM/AM and AM/PM models described in Section V.

B. Band-Pass Model

The INL results obtained in the previous section must be revised for a band-pass DAC. The principal difference between baseband and band-pass DAC designs is that the latter turns the unit current sources on and off at the LO frequency. Thus, the output conductance of each unit toggles between $1/r_O$ and zero, presenting an "average" conductance equal to $1/(2r_O)$. We therefore expect that the r_O terms in Eq. (1) must be replaced with $2r_O$ so as to model the band-pass DAC. We prove this point in Appendix I.

With the aid of these observations, we now rewrite (6) and (7) as

$$\alpha_1 \frac{N}{2} + \alpha_3 \frac{N^3}{8} = \pm I_0 [(2r_O) || (NR_L)] \quad (9)$$

$$\alpha_1 \left(\frac{N}{4}\right) + \alpha_3 \left(\frac{N}{4}\right)^3 = \frac{-I_0 R_L (N/2)(2r_o)^2}{\left(\frac{N}{4} R_L + 2r_o\right) \left(\frac{3N}{4} R_L + 2r_o\right)}. \quad (10)$$

These equations are readily solved to obtain α_1 and α_3 for the band-pass DAC.

III. INL-ACPR RELATION FOR CURRENT-MODE RF DACS

To derive compact equations for the relation between $\text{INL}_{\max,n}$ and ACPR, we wish to approximate the band-pass modulated RF signal by simpler functions. We surmise that a two-tone or four-tone representation may suffice.

Let us consider a two-tone model of the signal:

$$x(t) = A \cos \omega_1 t + A \cos \omega_2 t, \quad (11)$$

where ω_1 and ω_2 lie in the desired channel, but $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ in the adjacent ones. We select $A = N/4$ to avoid DAC input overrange. At the output, the fundamental and third-order intermodulation components exhibit amplitudes equal to $\alpha_1 A + (9/4)\alpha_3 A^3$ and $(3/4)\alpha_3 A^3$, respectively. The ACPR is given by the ratio of their powers:

$$\text{ACPR} = \frac{(9/16)\alpha_3^2 A^6}{2[\alpha_1 A + (9/4)\alpha_3 A^3]^2} \quad (12)$$

$$= \frac{(9/16)(\alpha_3/\alpha_1)^2 A^4}{2[1 + (9/4)(\alpha_3/\alpha_1)A^2]^2}. \quad (13)$$

Also, with $A = N/4$, Eq. (8) yields

$$\text{INL}_{\max,n} = \frac{8}{3\sqrt{3}} \left| \frac{\alpha_3}{\alpha_1} \right| A^2, \quad (14)$$

which, upon substitution in Eq. (13), leads to

$$\text{ACPR} = \frac{(3^5/2^{10})\text{INL}_{\max,n}^2}{2[1 - (27\sqrt{3}/32)\text{INL}_{\max,n}]^2}. \quad (15)$$

For example, an ACPR of -33 dB for Wideband CDMA (WCDMA) [18] requires $\text{INL}_{\max,n} < 6.5\%$. This value reveals that $(27\sqrt{3}/32)\text{INL}_{\max,n}$ is typically much less than unity (after predistortion or other linearization techniques), allowing a simpler expression:

$$\text{ACPR} \approx 0.119 \text{INL}_{\max,n}^2. \quad (16)$$

Similarly, we can also obtain the gain compression at the maximum point, in terms of $\text{INL}_{\max,n}$. The gain compression at this point is given by

$$G_c = \frac{2(\alpha_1 A + (9/4)\alpha_3 A^3)^2}{2(\alpha_1 A)^2} \quad (17)$$

$$= \left(1 - \frac{27\sqrt{3}}{32}\text{INL}_{\max,n}\right)^2. \quad (18)$$

We now repeat the foregoing calculations with four tones spaced by $\Delta\omega$, each having an amplitude equal to $N/8$. As shown in Fig. 4, the tones are so chosen as to place their third-order intermodulation (IM) products in the adjacent channels. The output fundamentals and IM components have the following amplitudes: $a = \alpha_1 A + (15/2)\alpha_3 A^3$,

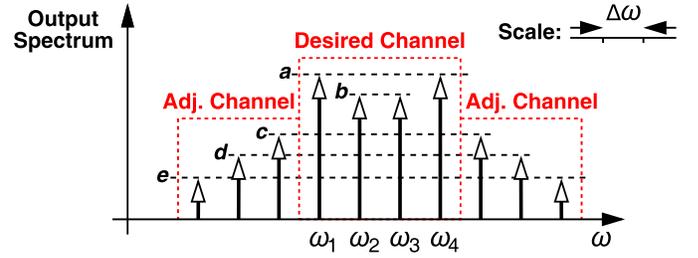


Fig. 4. Output spectrum in a four-tone test.

$b = \alpha_1 A + 9\alpha_3 A^3$, $c = (9/2)\alpha_3 A^3$, $d = (9/4)\alpha_3 A^3$, and $e = (3/4)\alpha_3 A^3$. Adding the powers of the last three, we obtain the adjacent-channel power, which should then be normalized to the sum of the fundamental powers:

$$\text{ACPR} = \frac{[(9/2)^2 + (9/4)^2 + (3/4)^2]\alpha_3^2 A^6}{2[\alpha_1 A + (15/2)\alpha_3 A^3]^2 + 2[\alpha_1 A + 9\alpha_3 A^3]^2}. \quad (19)$$

Since $A = N/8$, Eq. (8) yields

$$\text{INL}_{\max,n} = \frac{32}{3\sqrt{3}} \left| \frac{\alpha_3}{\alpha_1} \right| A^2, \quad (20)$$

and hence

$$\text{ACPR} = \frac{23 \times 3^5}{2^{14}} \times \frac{\text{INL}_{\max,n}^2}{\left(1 - \frac{45\sqrt{3}}{64}\text{INL}_{\max,n}\right)^2 + \left(1 - \frac{27\sqrt{3}}{32}\text{INL}_{\max,n}\right)^2}. \quad (21)$$

In a typical design, the denominator simplifies to approximately $2 - 5.36 \text{INL}_{\max,n}$, and

$$\text{ACPR} \approx \frac{23 \times 3^5}{2^{15}} \text{INL}_{\max,n}^2 (1 + 2.7 \text{INL}_{\max,n}) \quad (22)$$

$$\approx 0.171 \text{INL}_{\max,n}^2 (1 + 2.7 \text{INL}_{\max,n}). \quad (23)$$

For $\text{INL}_{\max,n} \approx 10\%$ (25.6 LSBs for an 8-bit DAC), we observe from Eq. (23) that the four-tone test predicts an ACPR of -26.6 dB, about 2.6 dB higher than that of the two-tone test.

Figure 5 plots the ACPR for different tests using $\alpha_1 = 1.95 \times 10^{-2}$ and $\alpha_3 = 3.1 \times 10^{-7}$ and a progressively larger number of tones, where for n tones, the input amplitude of each is chosen equal to $N/(2n)$. Here, $\text{INL}_{\max,n} = 10\%$. We infer that $n = 4$ and hence Eqs. (21) and (23) provide a reasonable approximation of the ACPR. In other words, the ACPR is a function of the maximum input swing and INL_{\max} , but relatively independent of the peak-to-average power ratio ($\text{PAPR} = 2n$), or the input power [$P_{in} = 1/(2n)$].

According to transistor-level simulations, the results shown in Fig. 5 change negligibly if the data transition times are varied from 10 ps to 20 ps or if random mismatches are included.

For circuit design purposes, we may be interested in the ACPR as a function of the output resistance of the unit current cell and the DAC resolution. Equations (9), (10), (20), and (23) readily afford such expression (Appendix II).

The foregoing derivations can be repeated if the DAC input does not reach its full scale. For $A = \gamma(N/2)$, Eq. (23)

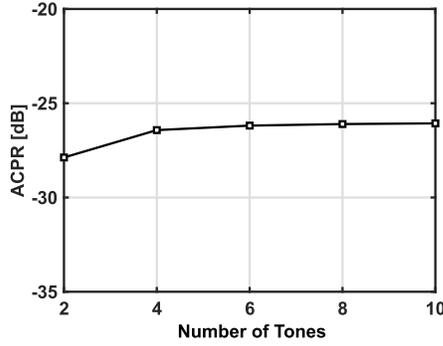


Fig. 5. ACPR as a function of number of tones for $\text{INL}_{\max,n} = 10\%$.

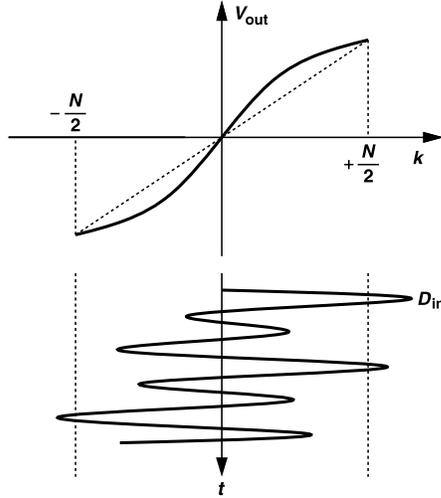


Fig. 6. Illustration of DAC overrange.

assumes the form

$$\text{ACPR} = 0.171(16\gamma^2)\text{INL}_{\max,n}^2(1 + 2.7\text{INL}_{\max,n}), \quad (24)$$

where $\gamma \leq 1/4$ for four tones.

IV. WHITE-NOISE INPUT TEST

The multi-tone input signal representation in the previous section readily leads to simple expressions relating the ACPR to the DAC INL. Nonetheless, we must verify the validity of Eqs. (21) and (23) for more realistic inputs. In this section, we assume a band-limited white-noise input and use simulations to check the accuracy of these equations.

Equations (21) and (23) have been derived for the case where the DAC's full scale is exercised. This scenario is straightforward for a multi-tone signal but not for a white Gaussian input as the latter can assume arbitrarily large amplitudes with a finite probability. We expect intuitively that "occasional" DAC overrange does not affect the ACPR significantly. We must therefore select the noise variance (or its rms value, σ) such that the noise amplitude reaches the full scale but exceeds it only infrequently. For example, as conceptually illustrated in Fig. 6, with $\sigma = N/2$, DAC overrange occurs 32% of the time, causing substantial clipping of the waveform.

The foregoing thoughts indicate that the accuracy with which the four-tone model predicts the ACPR for a random

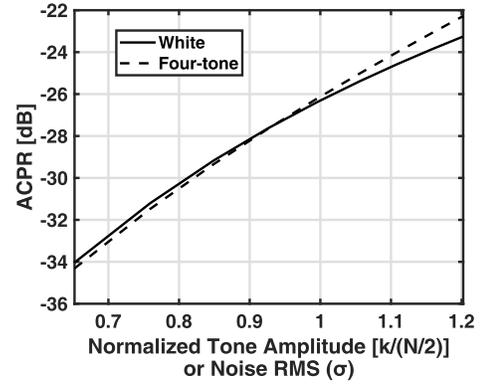


Fig. 7. Comparison of ACPR behavior for four-tone and white-noise inputs with $a_1 = 1.95 \times 10^{-2}$ and $a_3 = 3.1 \times 10^{-7}$.

signal depends, to some extent, on the signal's amplitude statistics. We return to this point below.

Representing the signal by band-limited white Gaussian noise, we proceed with our analysis by selecting the power of the noise equal to the total power of the four tones in Section III. For a DAC input range of $-N/2$ to $N/2$, the latter is equal to $N^2/32$ as each tone has a peak amplitude of $N/8$. The *upconverted* noise variance is thus chosen equal to $\sigma^2/2 = N^2/32$ and hence $\sigma = N/4$. Since σ is equal to 50% of the full scale in Fig. 2(c), the overrange probability is about 4.5%. We now simulate the DAC with four-tone and white-noise inputs and compare the resulting ACPRs. We wish to plot the ACPRs for different input levels. For an input level of k , we select (a) the peak amplitude of each tone equal to $k/4$, and (b) a noise standard deviation equal to $k/2$. Figure 7 shows the results, indicating an error of about 0.2 dB up to $k = N/2$. We conclude that, even though the white-noise input causes overrange 4.5% of the time, the equation $\text{ACPR} \approx 0.171(16\gamma^2)\text{INL}_{\max,n}^2(1 + 2.7\text{INL}_{\max,n})$ is relatively accurate.

In order to investigate the robustness of $\text{ACPR} \approx 0.171(16\gamma^2)\text{INL}_{\max,n}^2(1 + 2.7\text{INL}_{\max,n})$, we now allow the white-noise input variance to be *greater* than that of the four-tone test so that the DAC overranges more frequently. With $\sigma = 1.2N/4$, the overrange probability rises to 9.5%, but, as shown in Fig. 7, the disparity between the two types of tests still remains below 1 dB. We therefore conclude that for signals causing less than 10% overrange, the expression $\text{ACPR} \approx 0.171\gamma^2\text{INL}_{\max,n}^2$ is reasonably accurate.

V. EFFECT OF PHASE DISTORTION IN CURRENT-MODE RF DACS

The static nonlinearity effect formulated in the previous sections is the principal contributor to the adjacent channel power. However, phase distortion also has some impact on the ACPR. For example, the drain-substrate junction capacitance of M_3 and M_6 in Fig. 1 varies considerably as the output voltage swings from near zero to well above V_{DD} . In this section, we analyze this phenomenon.

For an intuitive understanding, we consider a DAC input of the form $x(t) = r(t)\cos(\omega_c t)$, where $r(t)$ denotes amplitude modulation (AM) and is the analog equivalent to k in Fig. 6. Since the bandwidth of $r(t)$ is roughly equal to that of the

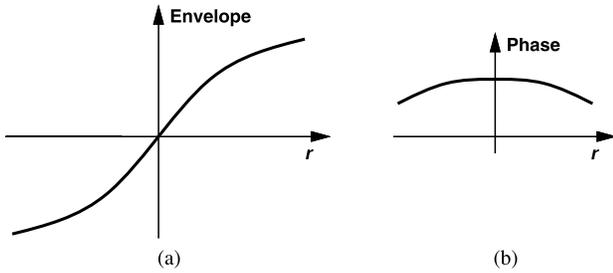


Fig. 8. (a) AM/AM, and (b) AM/PM characteristics in a differential DAC.

RF channel [19], we can assume that $r(t)$ varies much more slowly than the carrier does. The average value of the drain junction capacitance is a function of $r(t)$, causing the current-to-voltage transformation at the output node to experience a *phase shift* that depends on $r(t)$. That is, the signal incurs AM/PM conversion in addition to AM/AM conversion:

$$V_{out}(t) = \left[\alpha_1 r(t) + \frac{3}{4} \alpha_3 r^3(t) \right] \cos[\omega_c t + \theta(t)], \quad (25)$$

where $\theta(t)$ denotes the phase corruption. We wish to relate the ACPR to $\theta(t)$.

It is important to note that, in a fully-differential system, the envelope of Eq. (25) is an odd function of $r(t)$, but the phase is an *even* function (Fig. 8). The evenness of the phase can be intuitively explained by the fact that the signal's phase shift should be the same whether the differential input swing is $+r$ or $-r$.

For the DAC design example in Fig. 1, we can use simulations to construct the AM/AM and AM/PM characteristics. This is accomplished by transistor-level simulations in Keysight's ADS, where a harmonic balance simulation is run for every digital input. Here, we have $W/L = 5 \mu\text{m}/30 \text{ nm}$. Shown in Fig. 9, the plots provide the values of α_1 and α_3 , and the maximum phase excursions. The phase, $\theta(t)$, can be expressed as a "baseline" value of about 84° (not shown) plus a variable component, $\theta_1(t)$, that reaches approximately $\pm 6^\circ$: $\theta(t) = 84^\circ + \theta_1(t)$.

The baseline value does not play a role in the nonlinearity metrics, but $\theta_1(t)$ is small enough to allow the approximations $\cos \theta_1 \approx 1$ and $\sin \theta_1 \approx \theta_1$. For the input and output voltage range of interest, we can model θ_1 by an even function: $\theta_1 = \beta_0 + \beta_2 r^2$. For example, in the simulated AM/PM characteristic of Fig. 9(b), we have $\beta_0 = -0.1 \text{ rad} \approx -5.5^\circ$ and $\beta_2 = 0.2 \text{ rad} \approx 11^\circ$. While Fig. 9(b) implies that $y = 5.5 + 11r^2$ is not an accurate approximation, we see below that it still provides a good estimate of the ACPR. It is helpful for our subsequent derivations to associate the α_j terms to AM/AM conversion and the β_j terms to AM/PM conversion.

We should note that our formulation of phase distortion applies to different types of dynamic nonlinearity and even in the absence of static INL. As mentioned above, the nonlinear junction capacitance at the output nodes also lends itself to this analysis if memory effects are negligible, i.e. if the signal envelope does not contain rapid changes.

To calculate the ACPR, we first write the quadrature amplitudes of V_{out} in Eq. (25) as $V_{out,i} \cos(\omega_c t + 84^\circ) - V_{out,q} \sin(\omega_c t + 84^\circ)$, where

$$V_{out,i} = (\alpha_1 r + \frac{3}{4} \alpha_3 r^3) \cos \theta_1 \quad (26)$$

$$\approx \alpha_1 r + \frac{3}{4} \alpha_3 r^3 \quad (27)$$

$$V_{out,q} = (\alpha_1 r + \frac{3}{4} \alpha_3 r^3) \sin \theta_1 \quad (28)$$

$$\approx (\alpha_1 r + \frac{3}{4} \alpha_3 r^3) \theta_1 \quad (29)$$

$$\approx (\alpha_1 \beta_0) r + (\alpha_1 \beta_2 + \frac{3}{4} \alpha_3 \beta_0) r^3. \quad (30)$$

The ACPR is equal to the power in the adjacent channel, i.e., that due to terms such as r^n , $n \neq 1$, divided by the power in the desired channel, i.e., that due to terms containing r^1 :

$$\text{ACPR} = \frac{\sum P_n}{P_1} \approx \frac{P_3}{P_1}, \quad (31)$$

where

$$P_3 = P_{3,i} + P_{3,q} \quad (32)$$

$$= P_{3,i} \left\{ 1 + \left[\frac{\alpha_1 \beta_2 + (3/4) \alpha_3 \beta_0}{(3/4) \alpha_3} \right]^2 \right\} \quad (33)$$

$$\approx P_{3,i} \left[1 + \beta_0^2 + \frac{16}{9} \beta_2^2 \left(\frac{\alpha_1}{\alpha_3} \right)^2 \right], \quad (34)$$

and

$$P_1 = P_{1,i} + P_{1,q} \quad (35)$$

$$= P_{1,i} (1 + \beta_0^2). \quad (36)$$

Equation (31) yields

$$\text{ACPR} = \frac{P_{3,i}}{P_{1,i}} \left[1 + \left(\frac{4}{3} \frac{\alpha_1}{\alpha_3} \beta_2 \right)^2 \frac{1}{1 + \beta_0^2} \right] \quad (37)$$

$$= 0.171 \text{ INL}_{max,n}^2 \left[1 + \left(\frac{4}{3} \frac{\alpha_1}{\alpha_3} \beta_2 \right)^2 \frac{1}{1 + \beta_0^2} \right]. \quad (38)$$

The first and second terms in the square brackets on the right hand side of Eq. (38) represent AM/AM and AM/PM ACPR mechanisms, respectively. Thus,

$$\text{ACPR}_{PM} = 0.171 \left(\frac{1}{6\sqrt{3}} \left| \frac{\alpha_3}{\alpha_1} \right| N^2 \right)^2 \left[\left(\frac{4\alpha_1 \beta_2}{3\alpha_3} \right)^2 \frac{1}{1 + \beta_0^2} \right] \quad (39)$$

$$= 0.171 \left(\frac{2}{9\sqrt{3}} \frac{|\beta_2|}{\sqrt{1 + \beta_0^2}} N^2 \right)^2. \quad (40)$$

We can therefore define

$$\text{INL}_{max,n,PM} = \frac{1}{6\sqrt{3}} \left(\frac{4}{3} \frac{|\beta_2|}{\sqrt{1 + \beta_0^2}} \right) N^2, \quad (41)$$

which, upon substitution in Eq. (38), leads to

$$\text{ACPR} = 0.171 \text{ INL}_{max,n}^2 + 0.171 \text{ INL}_{max,n,PM}^2. \quad (42)$$

For the RF DAC of Fig. 9, Eq. (42) predicts an ACPR of -26.2 dB while transistor-level simulations show an ACPR of -26 dB , resulting in an error equal to 0.2 dB .

While the foregoing results are based on simulations, our methodology and formulation can be applied to each specific DAC design so as to determine how AM/PM conversion translates to ACPR.

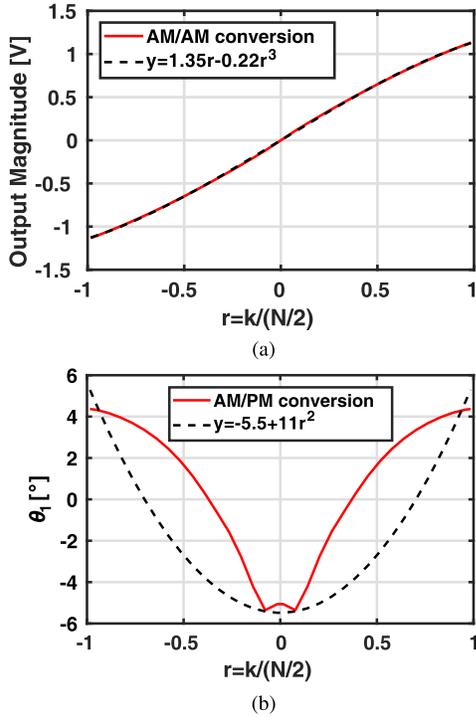


Fig. 9. (a) AM/AM, and (b) AM/PM conversion for an 8-bit DAC design along with approximations.

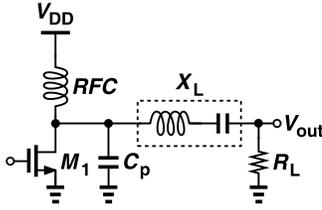


Fig. 10. Circuit diagram of a class-E RF DAC.

VI. SWITCHED-MODE RF DACS

In this section, we focus on switched-mode RF DACs, namely, those in which switching units act as resistors rather than as current sources. For example, Fig. 10 conceptually shows a class-E RF DAC in single-ended form. Here, the load components are so chosen as to ensure that both V_{DS1} and its derivative are close to zero just before M_1 turns on [20]. These conditions lead to

$$C_p = \frac{P_{sat}}{\pi \omega_0 V_{DD}^2}, \quad (43)$$

$$X_L = \frac{\pi}{2} \frac{\pi^2 - 4}{\pi^2 + 4} \frac{V_{DD}^2}{P_{sat}}, \quad (44)$$

$$R_L = \frac{8}{\pi^2 + 4} \frac{V_{DD}^2}{P_{sat}}, \quad (45)$$

for a given V_{DD} , a desired saturated power, P_{sat} , and a desired carrier frequency, ω_0 . If the radio-frequency choke (RFC) has a finite inductance, it can be absorbed in the C_p equation.

A class-E stage can accommodate a variable envelope either through the use of polar modulation, wherein V_{DD} is modulated by the envelope, or by modulating the on-resistance, R_{on} , of the output switch. In the latter case, the switch can be viewed as a DAC, and R_{on} varies according to

the digital input, m . To compute the ACPR and relate it to the INL, we first introduce a general model for class-E circuits.

A. Class-E RF DAC Model

Extensive efforts have been expended on modeling class-E stages [21], [22], [23], [24], [25], but the resulting equations are difficult to use for ACPR analysis. The lengthy expressions developed in the prior work arise due to the use of standard circuit analysis techniques such as Kirchhoff's laws. We propose a new model that leads to general results and serves our purpose well.

Modeling a class-E DAC by a polynomial presents certain challenges. From the component values shown in Fig. 10, we recognize that, to the first order, the output power, P_{out} , is independent of the total switch resistance. This means that P_{out} saturates as the DAC input reaches a certain level and the total on-resistance becomes sufficiently small. In other words, the output is saturated for a wide range of the digital input, making it difficult to approximate the behavior by a polynomial.

We begin by noting that the switch in Fig. 10 acts as a mixer, drawing a constant current from V_{DD} and upconverting it to the RF. We surmise that the switch, the RFC, and the supply voltage can be modeled by an RF Thevenin equivalent (Fig. 11). We must compute V_{Thev} , R_{Thev} , and the transfer function from V_{Thev} to V_{out} . With the class-E component values, the transfer function reduces to

$$\frac{V_{out}}{V_{Thev}} = \frac{0.43 - j0.5}{1 + Z_{Thev}(0.75 - j0.54)(P_{sat}/V_{DD}^2)} \quad (46)$$

in the vicinity of the desired carrier frequency.

In the next step, we determine Z_{Thev} . The time-variant nature of the network does not allow a direct analysis, but we can approach the problem as follows. We expect that Z_{Thev} is proportional to the switch resistance, R_{on} , and write $Z_{Thev} = \lambda R_{on}$. We then prove in Appendix III that the transfer function given by Eq. (46) is singular if $R_{on} \approx -0.4 \Omega$. That is,

$$1 + \lambda(-0.4 \Omega)(0.75 - j0.54)(P_{sat}/V_{DD}^2) = 0 \quad (47)$$

and hence $\lambda = 2.2 + j1.6$ if $P_{sat} = 1$ W and $V_{DD} = 1$ V. Thus,

$$Z_{Thev} = (2.2 + j1.6)R_{on}. \quad (48)$$

The complex value of Z_{Thev} is justified by noting that the time-variant circuit makes the Thevenin impedance a function of the load, as observed in N-path filters as well [26]. The transfer function then reduces to

$$\frac{V_{out}}{V_{Thev}} = \frac{0.43 - j0.5}{1 + 2.5R_{on}(P_{sat}/V_{DD}^2)}. \quad (49)$$

The last piece of this puzzle is V_{Thev} . Since the maximum power delivered to the load, P_{sat} , occurs with $R_{on} = 0$ and is given by $|V_{out}|^2/(2R_L)$, we have from Eq. (49):

$$\frac{|0.43 - j0.5|^2 |V_{Thev}|^2}{2R_L} = P_{sat}. \quad (50)$$

Replacing R_L with $[8/(\pi^2 + 4)]V_{DD}^2/P_{sat}$ gives

$$|V_{Thev}| \approx 1.64 V_{DD} \quad (51)$$

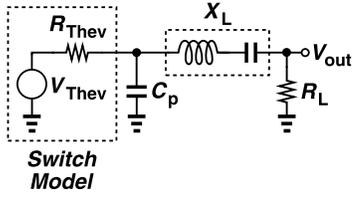
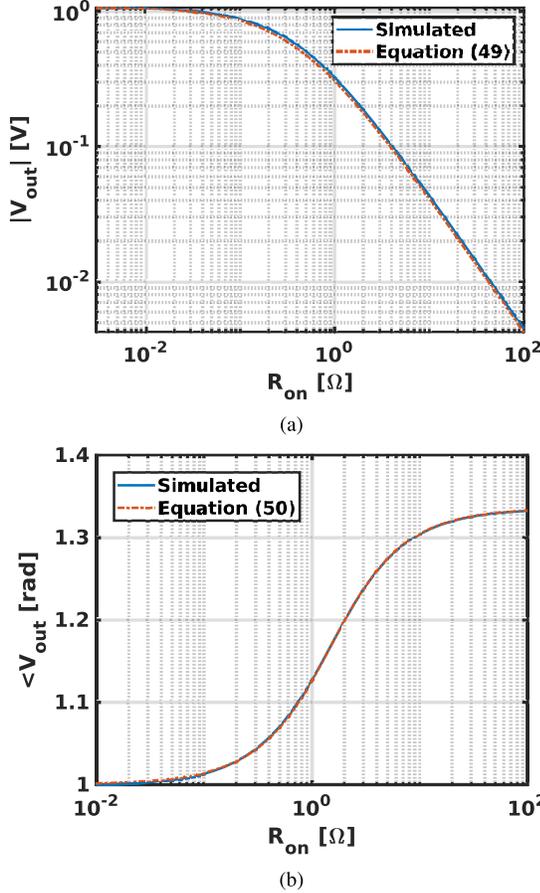

 Fig. 11. Model of a class-E RF DAC at f_c .


Fig. 12. (a) AM/AM, and (b) AM/PM conversion for a class-E RF DAC.

and

$$|V_{out}| = \frac{1.07 V_{DD}}{1 + 2.5 R_{on} (P_{sat} / V_{DD}^2)}. \quad (52)$$

We remark that this result holds for any class-E stage, but, emphasizing intuition rather than accuracy, our analysis of class-E operation assumes abrupt switching for the output transistor(s) and hence does not include their nonlinearity during transitions. Also, the nonlinearity of the output capacitance is neglected. Figure 12(a) plots this result against that of the actual class-E stage for the case of $P_{sat} = 1$ W and $V_{DD} = 1$ V. We observe a close agreement between the two.

The output phase of class-E stages is also of interest. Unfortunately, it does not lend itself to a closed-form expression, necessitating curve fitting [Fig. 12(b)]. We obtain

$$\angle V_{out} = 0.22 \arctan \left(\frac{R_{on} P_{sat}}{1.5 V_{DD}^2} \right) + 1 \text{ rad}. \quad (53)$$

B. INL of Switched-Mode Class-E DACs

Equation (52) permits us to compute the INL of class-E DACs as a function of the digital input, m . The net output resistance is $R_{on} = R_u/m$, where R_u denotes the resistance of a unit switching element. It follows that

$$|V_{out}| = \frac{1.07 V_{DD}}{1 + 2.5(R_u/m)(P_{sat}/V_{DD}^2)}. \quad (54)$$

In a manner similar to the calculation in Section II-A, we pass a straight line through the end points, subtract it from the characteristic, and differentiate the result with respect to m . The maximum INL thus emerges as

$$\text{INL}_{max} = \frac{1.07 V_{DD} \beta^2 N^2}{(\beta N + 1)(\sqrt{\beta N + 1} + 1)^2}, \quad (55)$$

where $\beta = 0.4 V_{DD}^2 / (R_u P_{sat})$ and N is the full-scale digital input. This value should be normalized to the maximum output voltage, $|V_{out}(m = N)|$:

$$\text{INL}_{max,n} = \frac{\beta N}{(\sqrt{\beta N + 1} + 1)^2}. \quad (56)$$

C. ACPR of Class-E RF DACs

For ACPR analysis, we consider a two-tone signal in the form of

$$x_{in}(t) = A \sin \omega_m t \cos \omega_c t. \quad (57)$$

The DAC can produce such an output if its overall switch conductance varies in proportion to the signal envelope while the phase of the LO switches between zero and π :

$$r_{on}(t) = \frac{R_{on}}{|\sin \omega_m t|}, \quad (58)$$

$$\phi_{LO} = \begin{cases} 0, & 0 < \omega_m t < \pi, \\ \pi, & \pi < \omega_m t < 2\pi, \end{cases} \quad (59)$$

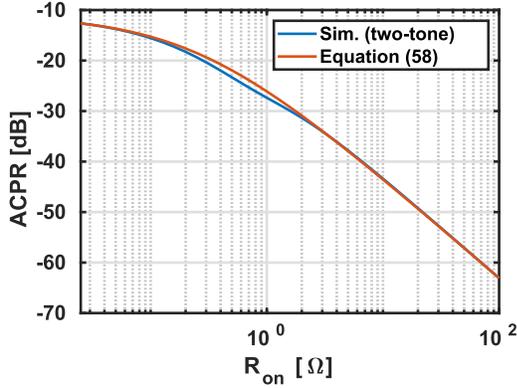
It follows from Eqs. (52) and (53) that

$$V_{out}(t) = \frac{1.07 V_{DD}}{1 + \frac{2.5 R_{on} P_{sat}}{|\sin \omega_m t| V_{DD}^2}} \times \cos \left[\omega_c t + 0.22 \arctan \left(\frac{R_{on} P_{sat}}{\sin \omega_m t 1.5 V_{DD}^2} \right) + 1 \right]. \quad (60)$$

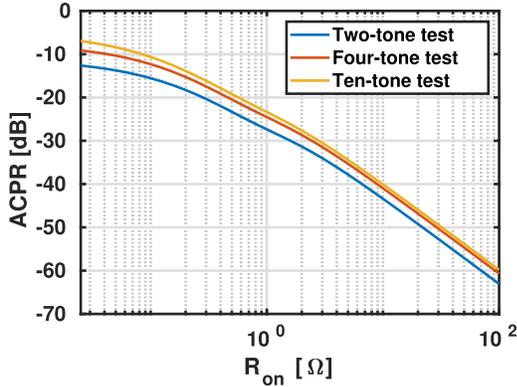
It is possible to obtain the intermodulation products from the Fourier expansion of this equation, but the results are too complex to lead to a relation between the ACPR and the INL. For this reason, we resort to curve fitting for the ACPR:

$$\text{ACPR} = \frac{0.28}{\left[3 \left(\frac{R_{on} P_{sat}}{V_{DD}^2} \right)^{0.8} + 1 \right]^{1.25}}. \quad (61)$$

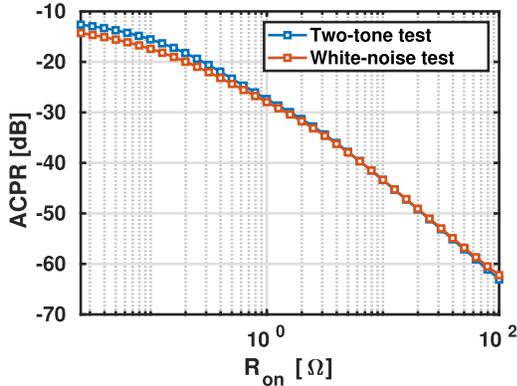
As shown in Fig. 13(a), the fit is fairly accurate for a wide range of R_{on} . Moreover, the simulation results depicted in Fig. 13(b) indicate that increasing the number of tones beyond four has little effect on the ACPR. Our approach allows the designer to relate the nonlinearity and the ACPR by means of simple simulations.



(a)



(b)



(c)

Fig. 13. (a) ACPR of a class-E RF DAC as a function of R_{on} , (b) different N -tone tests, and (c) two-tone and white-noise tests.

Figure 14 repeats the simulations with different LO rise and fall times (t_r and t_f , respectively), and with a sinusoidal LO. It is seen that the ACPR changes negligibly.

We repeat the white-noise test described in Section IV for switched-mode DACs as well, arriving at the behavior shown in Fig. 13(c). We conclude that white noise yields the same ACPR as an N -tone input if $\sigma_{in} = 1/(2R_{on})$ and

$$r_{on}(t) = \frac{2R_{on}}{|w(t)|}, \quad (62)$$

$$\phi_{LO} = \begin{cases} 0, & w(t) \geq 0, \\ \pi, & w(t) < 0, \end{cases} \quad (63)$$

where $w(t)$ denotes white noise with $\sigma_w = 1$.

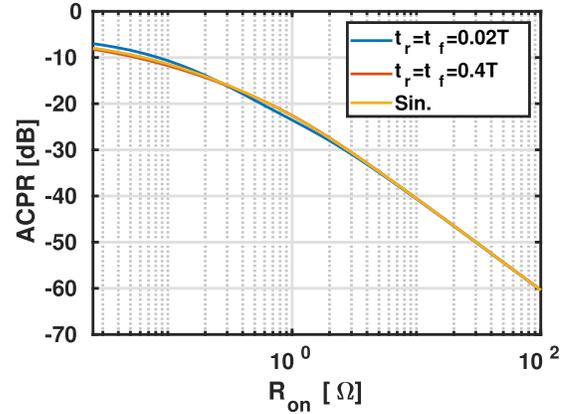


Fig. 14. ACPR of a class-E RF DAC as a function of R_{on} for different rise and fall times and a sinusoidal LO.

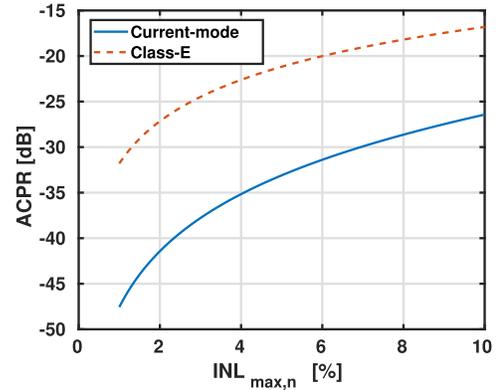


Fig. 15. ACPRs of a current-mode and a class-E RF DAC as a function of $INL_{max,n}$.

D. INL-ACPR Relation for Class-E RF DACs

With the aid of the $INL_{max,n}$ expression in Eq. (56) and the ACPR behavior predicted by Eq. (61), we write

$$ACPR = \frac{0.28}{\left[3 \left(\frac{0.4}{\beta N}\right)^{0.8} + 1\right]^2} \quad (64)$$

$$\approx \frac{0.28}{\left[\frac{(1 - INL_{max,n})^{1.6}}{2 INL_{max,n}^{0.8}} + 1\right]^2}. \quad (65)$$

It is interesting to compare this result to that obtained for current-steering DACs, namely, Eq. (23). As plotted in Fig. 15 for $INL_{max,n} < 10\%$, the two ACPRs differ by as much as 16 dB for a given $INL_{max,n}$ at low output power levels. The high ACPR arises because the switching action removes the amplitude variation due to baseband filtering.

This ACPR advantage of current steering accrues at the cost of power efficiency. In theory, class-A action yields a maximum efficiency of 50% for this architecture, whereas class-E operation, in principle, can approach an efficiency of 100% [20]. In practice, the former has been used in applications such as WCDMA [27], but the latter has also been embedded in linearity-correction loops with envelope tracking [28] or $\Delta\Sigma$ modulation [9].

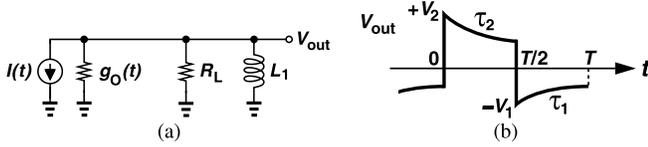


Fig. 16. (a) DAC model with time-variant output resistance, and (b) output waveform.

VII. CONCLUSION

This paper proposes simple expressions that allow the DAC designer to compute the ACPR from the INL. Both current-steering and switched-mode class-E DACs have been analyzed. The results have been studied by simulations that model the signal by multiple tones or white noise.

While our analysis has focused on current-steering (class-A) and switched-mode (class-E) architectures, other types of output stages can also be considered. For example, a class-D DAC design [29] can achieve a high efficiency with a nonlinearity similar to class-E. Another interesting candidate is the class-G stage [30], which deserves a thorough analysis and is beyond the scope of this paper.

APPENDIX I

Consider the simplified RF DAC model shown in Fig. 16(a), where the current source toggles between 0 and I_0 , and its output conductance, $g_O(t)$, between 0 and $g_1 = 1/r_O$. We wish to compute the amplitude of the first harmonic of V_{out} .

We note from Fig. 16(b) that, in the steady state, V_{out} jumps down to $-V_1$ when the current source turns on, discharges for half of the period, jumps up to V_2 when the current source turns off, and charges for the other half. The time constants are given by $\tau_1 = L_1/(R_L || g_1^{-1})$ and $\tau_2 = L_1/R_L$. We must compute $-V_1$ and $+V_2$ and then find the Fourier coefficient of the first harmonic of this waveform. We can readily predict that

$$V_{out} = -V_1 \exp\left(\frac{-t}{\tau_1}\right), \quad 0 < t < \frac{T}{2} \quad (66)$$

$$= V_2 \exp\left(\frac{-(t - T/2)}{\tau_2}\right), \quad \frac{T}{2} < t < T. \quad (67)$$

Writing a KCL at the output node in Fig. 16(a) yields

$$[g_L + g_O(t)] V_{out}(t) + I(t) + \frac{1}{L} \int_0^t V_{out}(\tau) d\tau = 0, \quad (68)$$

where $g_L = 1/R_L$. This equation must hold at $t = T^-/2$, $T^+/2$, T^- , and T^+ . Writing this equation at these times and combining the results, we obtain two equations in terms of $-V_1$ and V_2 , from which we have

$$V_1 = \frac{I_0}{g_1 + g_L} \frac{\exp[-T/(2\tau_2)] - 1}{\exp\left[-\frac{T}{2}\left(\frac{1}{\tau_1} + \frac{1}{\tau_2}\right)\right] - 1} \quad (69)$$

$$V_2 = \frac{I_0}{g_L} \frac{\exp[-T/(2\tau_1)] - 1}{\exp\left[-\frac{T}{2}\left(\frac{1}{\tau_1} + \frac{1}{\tau_2}\right)\right] - 1}. \quad (70)$$

If the clock period is much shorter than the time constants, we have $V_1 \approx V_2 \approx I_0/(g_1 + 2g_L)$. The amplitude of the

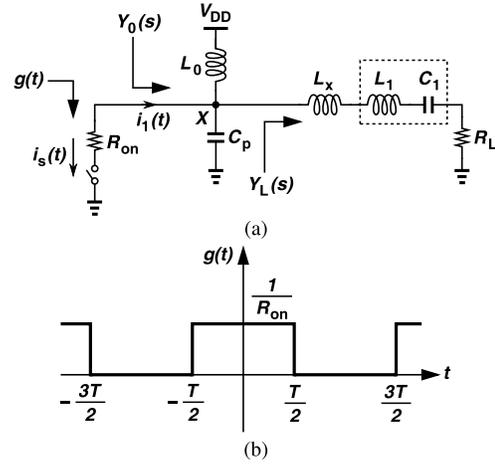


Fig. 17. (a) A model of a class-E stage, (b) waveform of the switch conductance, $g(t)$.

first harmonic of the waveform in Fig. 16(b) is $(4/\pi)V_1$ and is computed as follows.

$$\frac{4}{\pi} V_1 \approx \frac{4}{\pi} \frac{I_0}{g_1 + 2g_L} = \frac{2I_0}{\pi \left(\frac{1}{2r_O} + \frac{1}{R_L}\right)} \quad (71)$$

$$= \frac{2I_0}{\pi} [R_L || (2r_O)]. \quad (72)$$

APPENDIX II

We can obtain α_1 and α_3 from Eqs. (9) and (10) as follows:

$$\alpha_1 = \frac{2I_0 R_L r_O (-R_L^2 N^2 + 16R_L N r_O + 16r_O^2)}{(4r_O + R_L N)(4r_O + 3R_L N)(r_O + R_L N)} \quad (73)$$

$$\alpha_3 = \frac{32I_0 R_L^3 r_O}{(4r_O + R_L N)(4r_O + 3R_L N)(r_O + R_L N)} \quad (74)$$

Upon substitution in Eq. (20) and using the result in Eq. (23), we have

$$\text{ACPR} = 0.171 \left[\frac{8\sqrt{3}R_L^2 N^2}{9(-R_L^2 N^2 + 16R_L N r_O + 16r_O^2)} \right]^2 \times \left(1 + \frac{2.4\sqrt{3}R_L^2 N^2}{-R_L^2 N^2 + 16R_L N r_O + 16r_O^2} \right) \quad (75)$$

APPENDIX III

In this appendix, we determine under what condition the class-E transfer function expressed by Eq. (46) becomes singular. Considering the model shown in Fig. 17(a) and assuming normalized values $V_{DD} = 1$ V and $P_{sat} = 1$ W, we note that the high-Q resonator consisting of L_1 and C_1 is tuned to the carrier frequency, ω_0 , and rejects higher harmonics. We then approximate the admittance Y_L as

$$Y_L(\omega) = \begin{cases} (R_L + jL_x\omega)^{-1}, & \omega = \pm\omega_0, \\ 0, & \omega \neq \pm\omega_0. \end{cases} \quad (76)$$

The admittance Y_0 thus emerges as

$$Y_0(\omega) = \begin{cases} \infty, & \omega = 0, \\ jC_p\omega + (R_L + jL_x\omega)^{-1}, & \omega = \pm\omega_0, \\ jC_p\omega, & \omega \neq 0, \pm\omega_0. \end{cases} \quad (77)$$

$$\begin{bmatrix} g_0 + Y_{-N} & g_{-1} & \dots & g_{-2N} \\ g_1 & g_0 + Y_{-N+1} & \dots & g_{-2N+1} \\ \vdots & \vdots & \ddots & \vdots \\ g_{2N} & g_{2N-1} & \dots & g_0 + Y_N \end{bmatrix} \begin{bmatrix} a_{-N} \\ a_{-N+1} \\ \vdots \\ a_N \end{bmatrix} = -a_0 \begin{bmatrix} g_{-N} \\ g_{-N+1} \\ \vdots \\ g_N \end{bmatrix} \quad (89)$$

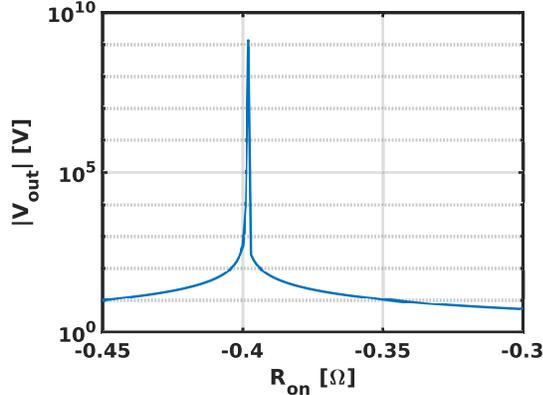


Fig. 18. Magnitude of V_{out} as a function of R_{on} for $P_{sat} = 1$ and $V_{DD} = 1$.

The circuit's periodic switching allows us to expand $g(t)$ and $v_x(t)$ in Fourier series. We assume the waveform shown in Fig. 17(b) for $g(t)$ and write

$$g(t) = \sum_{k=-\infty}^{+\infty} g_k e^{jk\omega_0 t}, \quad (78)$$

where

$$g_k = \begin{cases} \frac{1}{2R_{on}}, & k = 0, \\ \frac{1}{n\pi R_{on}} \sin\left(\frac{n\pi}{2}\right), & k \neq 0. \end{cases} \quad (79)$$

For $v_x(t)$, we have

$$v_x(t) = \sum_{k=-\infty}^{+\infty} a_k e^{jk\omega_0 t}, \quad (80)$$

where $a_0 = V_{DD}$. The current flowing through the switch is then obtained as

$$i_s(t) = g(t)v_s(t) = \sum_k a_k e^{jk\omega_0 t} \sum_k g_k e^{jk\omega_0 t} \quad (81)$$

$$= \sum_n \left(\sum_k a_k g_{n-k} \right) e^{jn\omega_0 t}, \quad (82)$$

Similarly, we have

$$i_1(t) = \sum_n a_n Y_0(n\omega_0) e^{jn\omega_0 t} \quad (83)$$

$$= -i_s(t). \quad (84)$$

It follows that

$$\begin{aligned} \sum_n \left(\sum_k a_k g_{n-k} \right) e^{jn\omega_0 t} + \sum_n a_n Y_0(n\omega_0) e^{jn\omega_0 t} &= 0 \\ \rightarrow \forall n \neq 0: \left(\sum_k a_k g_{n-k} \right) + a_n Y_0(n\omega_0) &= 0. \end{aligned} \quad (85)$$

Limiting the Fourier series in Eqs. (78) and (80) to N terms, we observe that Eq. (85) is valid for $-N \leq n \leq +N$, $n \neq 0$. Now, we rewrite this system of $2N$ equations and $2N$ unknowns in a matrix form [Eq. (89)], as shown at the top of the page, or as

$$MA = -V_{DD}G, \quad (86)$$

where M denotes the admittance matrix, and A the vector of a_k 's, and G the vector of g_k 's. Here, A is the unknown quantity. The transfer function is singular if the determinant of M is zero. Taking $N = 4$ as an example, we set the determinant of M to zero, obtaining

$$R_{on} \approx \frac{R_L^2 + L_x^2 \omega_0^2}{-2C_p L_x^2 \omega_0^3 + 2(L_x - C_p R_L^2) \omega_0 + 2R_L} \quad (87)$$

$$\approx -0.4 \Omega. \quad (88)$$

Higher values of N yield $R_{on} \approx -0.4 \Omega$ as well. This result is confirmed by extending our circuit simulation to negative values of R_{on} (Fig. 18). For other values of V_{DD} and P_{sat} , this critical R_{on} is simply scaled.

REFERENCES

- [1] V. K. Parikh, P. T. Balsara, and O. E. Eliezer, "All digital-quadrature-modulator based wideband wireless transmitters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 56, no. 11, pp. 2487–2497, Nov. 2009.
- [2] R. F. Cordeiro, A. S. R. Oliveira, and J. M. N. Vieira, "All-digital transmitter with a mixed-domain combination filter," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 1, pp. 4–8, Sep. 2016.
- [3] R. Bhat and H. Krishnaswamy, "Design tradeoffs and predistortion of digital Cartesian RF-power-DAC transmitters," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 63, no. 11, pp. 1039–1043, Mar. 2016.
- [4] T. Buckel *et al.*, "A novel digital-intensive hybrid polar-I/Q RF transmitter architecture," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 65, no. 12, pp. 4390–4403, Dec. 2018.
- [5] Z. Boos *et al.*, "A fully digital multimode polar transmitter employing 17b RF DAC in 3G mode," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2011, pp. 376–378.
- [6] O. Wada *et al.*, "5 GHz-band CMOS direct digital RF modulator using current-mode DAC," in *Proc. Asia Pacific Microw. Conf.*, Dec. 2012, pp. 1118–1120.
- [7] M. Ingels *et al.*, "A linear 28 nm CMOS digital transmitter with 2×12 bit up to LO baseband sampling and -58 dBc C-IM3," in *Proc. 40th Eur. Solid State Circuits Conf. (ESSCIRC)*, Sep. 2014, pp. 379–382.
- [8] C. Erdmann *et al.*, "A 330 mW 14b 6.8 GS/s dual-mode RF DAC in 16 nm FinFET achieving -70.8 dBc ACPR in a 20 MHz channel at 5.2 GHz," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2017, pp. 280–281.
- [9] S.-M. Babamir and B. Razavi, "A digital RF transmitter with background nonlinearity correction," *IEEE J. Solid-State Circuits*, vol. 55, no. 6, pp. 1502–1515, Jun. 2020.
- [10] T. Chen and G. G. E. Gielen, "The analysis and improvement of a current-steering DACs dynamic SFDR-I: The cell-dependent delay differences," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 53, no. 1, pp. 3–15, Jan. 2006.
- [11] T. Chen and G. Gielen, "The analysis and improvement of a current-steering DAC's dynamic SFDR-II: The output-dependent delay differences," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 54, no. 2, pp. 268–279, Feb. 2007.
- [12] E. Bechthum, G. Radulov, J. Briaire, G. Geelen, and A. van Roermund, "Systematic analysis of the impact of mixing locality on mixing-DAC linearity for multicarrier GSM," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2012, pp. 241–244.

- [13] Y. Tang, H. Hegt, A. van Roermund, K. Doris, and J. Briaire, "Statistical analysis of mapping technique for timing error correction in current-steering DACs," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2007, pp. 1225–1228.
- [14] A. van den Bosch, M. Steyaert, and W. Sansen, "SFDR-bandwidth limitations for high speed high resolution current steering CMOS D/A converters," in *Proc. 6th IEEE Int. Conf. Electron., Circuits Syst.*, Sep. 1999, pp. 1193–1196.
- [15] F.-T. Chou and C.-C. Hung, "Glitch energy reduction and SFDR enhancement techniques for low-power binary-weighted current-steering DAC," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 6, pp. 2407–2411, Jun. 2016.
- [16] F. Roger, "A 200 mW 100 MHz-to-4 GHz 11th-order complex analog memory polynomial predistorter for wireless infrastructure RF amplifiers," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, Feb. 2013, pp. 94–95.
- [17] M. J. M. Pelgrom, A. C. J. Duinmaijer, and A. P. G. Welbers, "Matching properties of MOS transistors," *IEEE J. Solid-State Circuits*, vol. 24, no. 5, pp. 1433–1439, Oct. 1989.
- [18] *User Equipment (UE) Radio Transmission and Reception (FDD) (Release 16)*, document 3GPP TS 25.101 V16.0.0, 3rd Generation Partnership Project; Technical Specification Group Radio Access Network, Valbonne, France, 1999.
- [19] M. R. Elliott *et al.*, "A polar modulator transmitter for GSM/EDGE," *IEEE J. Solid-State Circuits*, vol. 39, no. 12, pp. 2190–2199, Dec. 2004.
- [20] N. O. Sokal and A. D. Sokal, "Class-E—a new class of high-efficiency tuned single-ended switching power amplifiers," *IEEE J. Solid-State Circuits*, vol. SSC-10, no. 3, pp. 168–176, Jun. 1975.
- [21] J. C. Mandojana *et al.*, "A discrete/continuous time-domain analysis of a generalized class E amplifier," *IEEE Trans. Circuits Syst.*, vol. 37, no. 8, pp. 1057–1064, Aug. 1990.
- [22] P. Alinikula, "Optimum component values for a lossy class E power amplifier," in *IEEE MTT-S Int. Microw. Symp. Dig.*, vol. 3, Jun. 2003, pp. 2145–2148.
- [23] C. Wang *et al.*, "Improved design technique of a microwave class-E power amplifier with finite switching-on resistance," in *Proc. IEEE Radio and Wireless*, Aug. 2002, pp. 241–244.
- [24] M. Acar *et al.*, "Analytical design equations for class-E power amplifiers with finite DC-feed inductance and switch on-resistance," in *Proc. IEEE Int. Symp. Circuits Syst.*, May 2007, pp. 2818–2821.
- [25] C. P. Avratoglou, N. C. Voulgaris, and F. I. Ioannidou, "Analysis and design of a generalized class-E tuned power amplifier," *IEEE Trans. Circuits Syst.*, vol. 36, no. 8, pp. 1068–1079, Aug. 1989.
- [26] A. Mirzaei and H. Darabi, "Analysis of imperfections on performance of 4-phase passive-mixer-based high-Q bandpass filters in SAW-less receivers," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 58, no. 5, pp. 879–892, May 2011.
- [27] H. Choi, Y. Lee, and S. Hong, "A digital polar CMOS power amplifier with a 102-dB power dynamic range using a digitally controlled bias generator," *IEEE Trans. Microw. Theory Techn.*, vol. 62, no. 3, pp. 579–589, Mar. 2014.
- [28] C.-T. Chen, C.-J. Li, T.-S. Horng, J.-K. Jau, and J.-Y. Li, "High efficiency dual-mode RF transmitter using envelope-tracking dual-band class-E power amplifier for W-CDMA/WiMAX systems," in *IEEE MTT-S Int. Microw. Symp. Dig.*, Jun. 2009, pp. 417–420.
- [29] H. Kobayashi, J. M. Hinrichs, and P. M. Asbeck, "Current-mode class-D power amplifiers for high-efficiency RF applications," *IEEE Trans. Microw. Theory Techn.*, vol. 49, no. 12, pp. 2480–2485, Dec. 2001.
- [30] F. H. Raab, "Average efficiency of class-G power amplifiers," *IEEE Trans. Consum. Electron.*, vol. CE-32, no. 2, pp. 145–150, May 1986.



Seyed-Mehrdad Babamir (Member, IEEE) received the B.Sc. and M.Sc. degrees from the Sharif University of Technology, Tehran, Iran, in 2013 and 2015, respectively, and the Ph.D. degree from the University of California, Los Angeles (UCLA), CA, USA in 2019, all in electrical engineering.

He was a Post-Doctoral Scholar at the Communication Circuits Laboratory, UCLA. He has been with Broadcom Inc., San Diego, CA, USA, since 2019. His research interests include analog, RF, and millimeter-wave integrated circuit design for wireless transceivers and frequency synthesizers.

Dr. Babamir was a recipient of the Broadcom Foundation Fellowship from 2017 to 2018. He has served as a Reviewer for the IEEE JOURNAL OF SOLID-STATE CIRCUITS (JSSC), the IEEE TRANSACTIONS ON MICROWAVE THEORY AND TECHNIQUES (TMTT), and the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS (TCAS-I).



Behzad Razavi (Fellow, IEEE) received the B.S.E.E. degree from the Sharif University of Technology in 1985 and the M.S.E.E. and Ph.D.E.E. degrees from Stanford University, in 1988 and 1992, respectively.

He was an Adjunct Professor at Princeton University from 1992 to 1994 and at Stanford University in 1995. He was at the AT&T Bell Laboratories and the Hewlett-Packard Laboratories until 1996. Since 1996, he has been an Associate Professor and subsequently a Professor of electrical engineering with the University of California, Los Angeles. He is the author of *Principles of Data Conversion System Design* (IEEE Press, 1995), *RF Microelectronics* (Prentice Hall, 1998, 2012) (translated to Chinese, Japanese, and Korean), *Design of Analog CMOS Integrated Circuits* (McGraw-Hill, 2001, 2016) (translated to Chinese, Japanese, and Korean), *Design of Integrated Circuits for Optical Communications* (McGraw-Hill, 2003, Wiley, 2012), *Design of CMOS Phase-Locked Loops* (Cambridge University Press, 2020), and *Fundamentals of Microelectronics* (Wiley, 2006, 2014, 2021) (translated to Korean, Portuguese, and Turkish). His current research interests include wireless and wireline transceivers and data converters.

Prof. Razavi is a member of the US National Academy of Engineering and a fellow of U.S. National Academy of Inventors. He served on the Technical Program Committees of the International Solid-State Circuits Conference (ISSCC) from 1993 to 2002 and VLSI Circuits Symposium from 1998 to 2002. He has served as an IEEE Distinguished Lecturer. He received the Beatrice Winner Award for Editorial Excellence from the 1994 ISSCC, the Best Paper Award from the 1994 European Solid-State Circuits Conference, the Best Panel Award from the 1995 and 1997 ISSCC, the TRW Innovative Teaching Award in 1997, the Best Paper Award from the IEEE Custom Integrated Circuits Conference in 1998, and the McGraw-Hill First Edition of the Year Award in 2001. He was the co-recipient of both the Jack Kilby Outstanding Student Paper Award and the Beatrice Winner Award for Editorial Excellence from the 2001 ISSCC. He received the Lockheed Martin Excellence in Teaching Award in 2006, the UCLA Faculty Senate Teaching Award in 2007, the CICC Best Invited Paper Award in 2009 and in 2012, and the IEEE CAS Darlington Best Paper Award in 2021. He was the co-recipient of the 2012 and the 2015 VLSI Circuits Symposium Best Student Paper Awards and the 2013 CICC Best Paper Award. He was also recognized as one of the top ten authors in the 50-year history of ISSCC. He received the 2012 Donald Pederson Award in Solid-State Circuits. He was also the recipient of the 2014 American Society for Engineering Education PSW Teaching Award, the 2017 IEEE CAS John Choma Education Award, and the 2022 IEEE Solid-State Circuits Society Innovative Education Award. He has also served as Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS, and International Journal of High Speed Electronics. He was the Founding Editor-in-Chief of the IEEE SOLID-STATE CIRCUITS LETTERS. He was the Editor of *Monolithic Phase-Locked Loops and Clock Recovery Circuits* (IEEE Press, 1996) and *Phase-Locking in High-Performance Systems* (IEEE Press, 2003).