# A 900-MHz/1.8-GHz CMOS Receiver for Dual-Band Applications

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***Abstract*— A dual-band receiver employs the Weaver architecture with two tuned radio-frequency stages and a common intermediate-frequency stage to allow operation with 900-MHz and 1.8-GHz standards while using only two oscillators. Fabricated in a digital 0.6-$\mu$m CMOS technology, the receiver achieves an overall noise figure of 4.7 dB and input third intercept point of −8 dBm at 900 MHz, and 4.9 dB and −6 dBm at 1.8 GHz. The voltage gain is 23 dB with a power dissipation of 75 mW from a 3-V supply.**

***Index Terms*— Low-noise amplifiers (LNA's), mixers, RF receivers, wireless communications.**

## I. Introduction

MULTISTANDARD radio-frequency (RF) transceivers are predicted to play a critical role in wireless communications in the 900–5200-MHz range. With cellular and cordless phone standards operating in the 900-MHz and 1.8-GHz bands, the Global Positioning System in the 1.5-GHz band, and wireless local area networks in the 2.4-GHz band, it is desirable to combine two or more standards in one mobile unit [1]. The principal challenge in this task arises from the stringent cost and form-factor requirements, making it necessary to limit the additional hardware, particularly, filters, resonators, oscillators, and frequency synthesizers. Thus, both the architecture design and the frequency planning of a multistandard transceiver demand careful studies and numerous iterations.

This paper describes the design of a dual-band CMOS receiver for 900-MHz and 1.8-GHz standards [2]. Based on the Weaver image-reject architecture, the receiver has been designed and fabricated in a 0.6-$\mu$m digital CMOS technology. Section II of this paper reviews the global system for mobile communication (GSM) and DCS1800 standards and discusses some of the difficulties in combining the two in one transceiver. Section III deals with image-reject receiver architectures and their tradeoffs, and Section IV presents the dual-band receiver architecture. The design of the building blocks in CMOS technology is the subject of Section V, and spurious components are studied in Section VI. The experimental results are summarized in Section VII.

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TABLE I
System Characteristics of the GSM and DCS1800 Wireless Standards

| | GSM | DCS1800 |
|---|---|---|
| Modulation | Gaussian Minimum Shift Keying | Gaussian Minimum Shift Keying |
| Multiple Access Technique | Time Division Multiple Access | Time Division Multiple Access |
| Duplexing | Frequency Division Duplexing | Frequency Division Duplexing |
| Receive Frequency Band | 935-960 MHz | 1805-1880 MHz |
| Channel Spacing | 200 kHz | 200 kHz |
| Number of Channels | 124 | 350 |

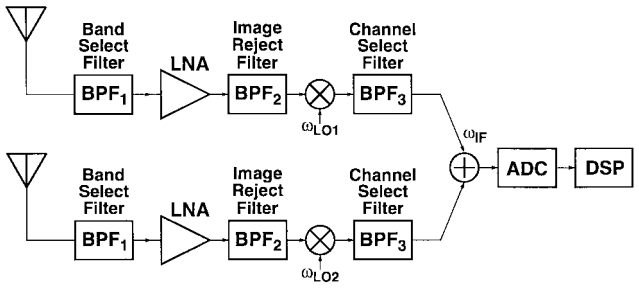



Fig. 1. Conceptual example of a dual-band receiver.

## II. General Considerations

To target realistic specifications, this design uses two cellular standards, namely, GSM and Digital Communication System at 1800 MHz (DCS1800) as the framework. The two standards incorporate identical multiple access and duplexing techniques, channel bandwidths, and modulation formats. Table I summarizes the characteristics of GSM and DCS1800 pertaining to receiver design. The common properties suggest that the two standards can be accommodated in a dual-band receiver while sharing some of the components.

Fig. 1 illustrates a conceptual example, where two heterodyne receivers translate the input bands to a common intermediate frequency (IF), with the signal paths merged after channel selection is performed. Sharing the analog-to-digital (A/D) converter and the digital signal processor between the two bands, this architecture nonetheless requires a large number of external, costly components as well as driving and sensing compliance with standard impedance levels. In addition, tradeoffs between image rejection and channel selection often mandate a second downconversion mixing in each path, further increasing the complexity.

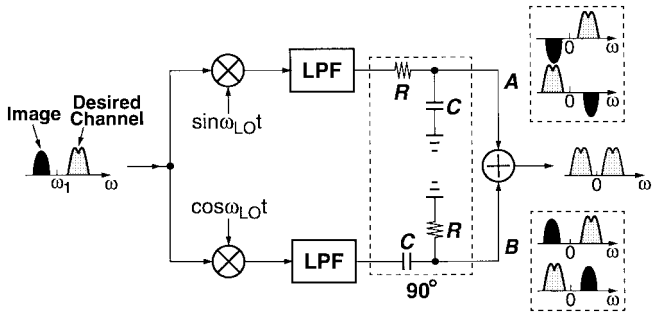



Fig. 2. Hartley image-reject receiver.

The objective of this work is to eliminate the image-reject filters and move the channel-selection filtering to the baseband or its vicinity. We therefore briefly study image-reject receivers here.

## III. Image-Reject Receiver Architectures

### A. Hartley Architecture

A commonly used image-reject architecture originates from a single-sideband modulator introduced by Hartley [3]. Illustrated in Fig. 2, Hartley's circuit mixes the RF input with the quadrature outputs of the local oscillator (LO) and low-pass filters and shifts the results by 90° before adding them together. It can be shown that the spectra at points $A$ and $B$ contain the desired channel with the same polarity and the image with opposite polarity. The summed output is therefore free from the image.

The principal drawback of the Hartley architecture is its sensitivity to mismatches: with phase and gain imbalance, the image is only partially cancelled. The influence of gain and phase mismatch on image rejection can be studied by lumping the mismatches of the mixers, the low-pass filters, the two ports of the adder, and the 90° phase-shift network into the error terms $\Delta A$ and $\theta$ for the gain and phase mismatches, respectively, between the two paths in the Hartley architecture. It can be proved that if $\Delta A \ll A$ and $\theta \ll 1$ radian, where $A$ is the nominal gain of each path in the architecture, the image-rejection ratio (IRR) can be approximated by the expression [4]

$$\text{IRR}^{-1} \approx \frac{\theta^2 + (\Delta A/A)^2}{4}.$$

In typical integrated circuits, an IRR in the range of 30–40 dB may be achieved, which corresponds to a gain mismatch in the range of 0.2–0.6 dB along with phase imbalance between 1° and 5°.

In addition to random mismatches, the upper and lower paths in Fig. 2 suffer from gain error if the absolute value of $R$ and $C$ varies with process and temperature. A variation of 20% in $RC$ limits IRR to only 20 dB [4], pointing to a severe difficulty in integrated-circuit implementations, especially if high-quality resistors and capacitors are not available.

Other drawbacks of the Hartley topology include the loss and noise of the shift-by-90° stage and the linearity and noise of the adder.

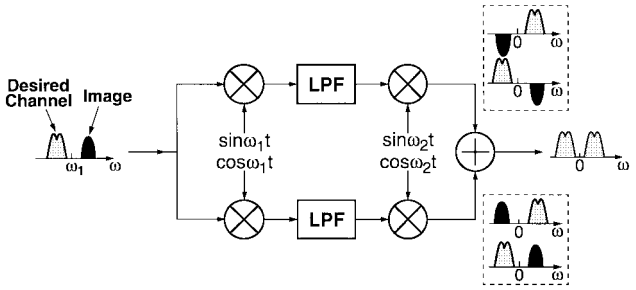



Fig. 3. Weaver image-reject architecture.

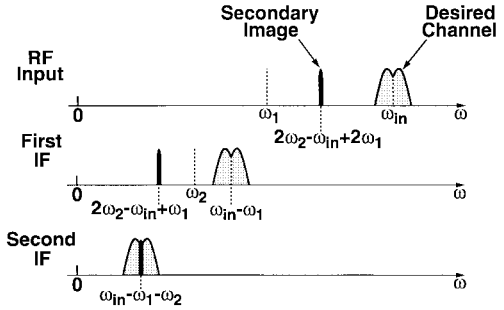



Fig. 4. Problem of secondary image in Weaver architecture.

### B. Weaver Architecture

The Weaver architecture [5], originally invented as an alternative to Hartley's single-sideband modulator, can also serve as an image-reject receiver. Recently utilized in [6] and [7], the architecture is shown in Fig. 3 in simplified form. The circuit performs two consecutive quadrature downconversion operations on the signal and the image such that if the final outputs are subtracted, the signal is obtained and the image is suppressed; and if they are added, the reverse occurs.

The Weaver approach is also sensitive to mismatches, but it avoids the use of an $RC$-$CR$ network, thereby achieving greater image rejection despite process and temperature variations.

An important issue in the Weaver architecture is the "secondary image" [4]. If the second downconversion translates the signal spectrum to a nonzero center frequency, an unwanted band may fall into the desired channel. Illustrated in Fig. 4, this effect constrains the choice of the second LO frequency. For example, in [7], the IF spectrum is translated to dc so as to eliminate the problem. We return to this issue in Section IV.

## IV. Dual-Band Receiver Architecture

Recall from Section III that the Weaver architecture (and also the Hartley architecture) can yield the signal or the image depending on whether the final results are added or subtracted (Fig. 5). The fact that addition or subtraction of the outputs in Fig. 5 can select or reject two bands symmetrically located around $\omega_1$ provides the foundation for this work.

Fig. 6 depicts the dual-band receiver architecture. The signal received by the antenna in each band is applied to a duplexer filter to perform band selection. Subsequently, a low-noise amplifier (LNA) and two quadrature mixers boost and translate the signal to an IF of 450 MHz. The results of the two bands

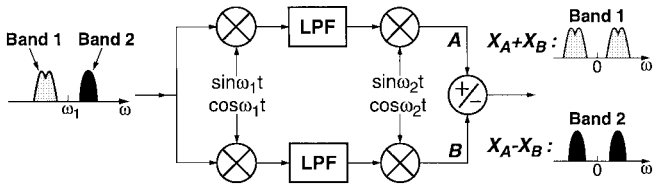



Fig. 5. Addition/subtraction of outputs in Weaver architecture.

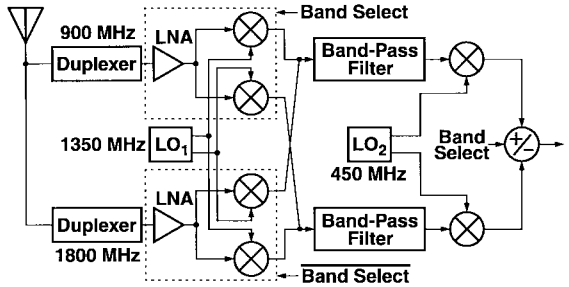



Fig. 6. Dual-band implementation of the Weaver architecture.

are combined at this IF and undergo a second quadrature downconversion operation as in Fig. 3. The LNA and RF mixers of the two bands are separate to allow flexibility in the choice of device dimensions and bias currents, thus optimizing the performance of each path independently. For the second downconversion, two sets of quadrature downconversion mixers have been used to provide both $I$ and $Q$ baseband outputs [7]. The bandpass filters are formed by means of on-chip inductors and parasitic capacitances, but they do not perform channel selection.

In the receiver of Fig. 6, the first LO frequency is set midway between the GSM and DCS1800 bands, making the two bands images of each other. That is, the RF mixing uses high-side injection for GSM and low-side injection for DCS1800. The band-select input switches the receiver between the two operating modes (GSM or DCS1800), shutting off the RF path of the idle band to save power consumption. Also, the band-select switch controls the addition or subtraction at the receiver output in order to generate the desired signal and reject the image component.

While the Weaver architecture by itself does not provide sufficient image rejection, the 900-MHz spacing between the signal and the image allows substantial image filtering in the front-end duplexers. Fig. 7 shows an example: the measured insertion characteristics of a 900-MHz Murata duplexer (DFC5R881), exhibiting 3 dB of in-band loss and 41.7 dB of rejection at 1.8 GHz. As a result, the overall IRR exceeds 70 dB.

The distribution of gain, noise, and nonlinearity in the receiver chain plays a key role in the overall performance, necessitating iterations between architecture design and circuit design. Since channel-selection filtering is postponed to the stages following the IF mixers, the third intercept point ($IP_3$) of each stage must scale according to the total gain preceding that stage. With the initial estimate of the $IP_3$, the corresponding circuit is then designed so as to minimize its noise contribution.

As mentioned in Section III-B, the problem of secondary image constrains the choice of the second IF in the Weaver topology. As shown in Fig. 8, the present design provides quadrature downconversions to allow translation to the baseband. This approach, however, suffers from some of the difficulties encountered in direct-conversion receivers. For example, dc offsets due to the self-mixing of the second LO, flicker noise in the analog baseband circuits, and $I$ and $Q$ mismatch corrupt the downconverted signals [8], [9].

## V. Building Blocks

The design of the building blocks of the receiver is governed by various tradeoffs among noise, linearity, and power consumption. Issues related to the interface between the LNA and the RF mixers mandate that these two circuits be designed as one entity.

### A. LNA and RF Mixer

To achieve a relatively low noise figure and a reasonable input match, the LNA employs a common-source cascode stage with inductive degeneration [10] (Fig. 9). To avoid uncertainties due to bondwire inductance, both the source inductor and the drain inductor are integrated on the chip. Drawing approximately 5 mA from the supply, the LNA exhibits a noise figure of less than 2.5 dB and an $IP_3$ of greater than $-2$ dBm in each band. The parasitic capacitance of $L_2$, the drain junction and overlap capacitance of $M_2$, and the input capacitance of the mixers resonate with $L_2$ at the frequency of interest. With a $Q$ of about three, this resonance lowers the image signal by approximately 10 dB.

The LNA directly drives the quadrature RF mixers, which are configured as single-balanced circuits. Employing inductive loads to minimize thermal noise, each mixer drains 2 mA to achieve a reasonable tradeoff between noise and nonlinearity. With 22 dB of voltage gain in the LNA, it is desirable to realize an $IP_3$ of greater than 1.26 $V_{rms}$ (equivalent to $+15$ dBm in a 50-$\Omega$ interface) in the mixer, while maintaining its input-referred noise voltage below roughly 5 nV/$\sqrt{\text{Hz}}$.

The dimensions of $M_7$–$M_9$ in Fig. 9 strongly affect the performance of the RF mixer. Transistor $M_7$ is sized such that its overdrive voltage is sufficiently large to guarantee the required $IP_3$. This is in contrast to bipolar implementations, where enormous emitter degeneration would be necessary to achieve an $IP_3$ greater than 1.26 $V_{rms}$. The key point here is that for a given bias current and $IP_3$, a properly sized MOS transistor exhibits much *higher* transconductance than a degenerated bipolar structure.

Transistors $M_8$ and $M_9$ in Fig. 9 also influence the noise and conversion gain of the mixer. The choice of the width of these devices is governed by a tradeoff between their switching time and the parasitic capacitances they introduce at node $P$. For a given (sinusoidal) LO swing, $M_8$ and $M_9$ are simultaneously on for a shorter period of time as their width increases. A compromise is thus reached by choosing $(W/L)_{8,9} = 400\,\mu\text{m}/0.6\,\mu\text{m}$, allowing the pair to turn off with a differential swing of 100 mV while degrading the conversion gain by less than 1 dB.

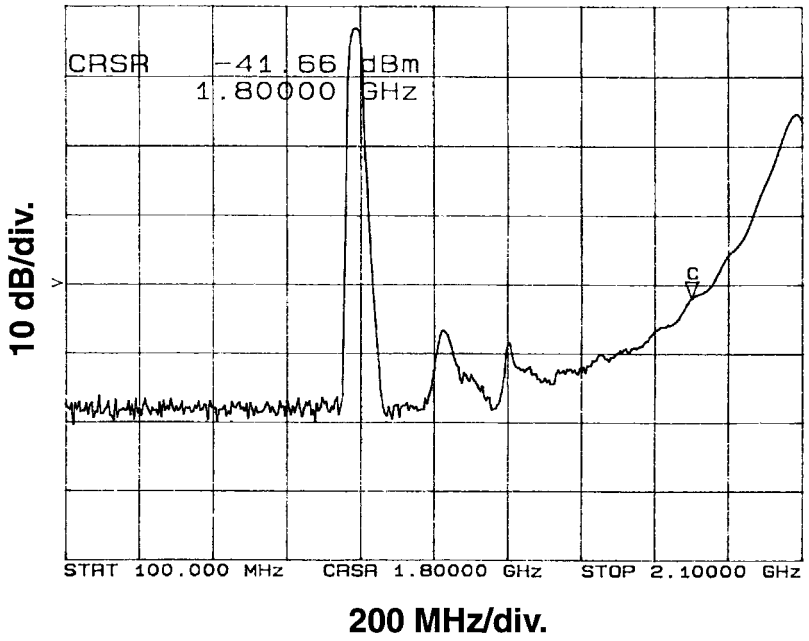



Fig. 7. Murata DFC5R881: 900-MHz duplexer receiver path.

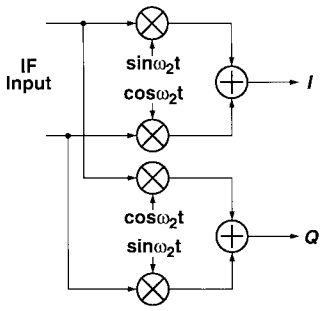



Fig. 8. In-phase and quadrature baseband outputs from IF mixers.

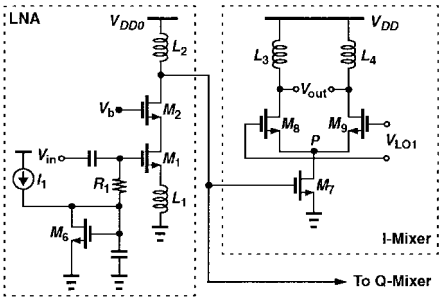



Fig. 9. LNA and RF mixer.

## B. LNA/Mixer Interface

The interface between the LNA and the mixer merits particular attention. As shown in Fig. 10, to achieve a well-defined bias current in the mixer, the LNA incorporates the dc load $M_3$ with diode-connected devices $M_4$ and $M_5$. Neglecting the dc drop across $L_2$, we note that $V_{GS4}+V_{GS5} = V_{GS3}+V_{GS7}$. Thus, proper ratioing of $M_3$ and $M_7$ with respect to $M_4$ and $M_5$ defines $I_{D7}$ as a multiple of $I_2$. Capacitor $C_1$ provides an ac ground at the source of $M_3$ so that the output resistance of $M_3[= 1/(g_{m3} + g_{mb3})]$ does not degrade the

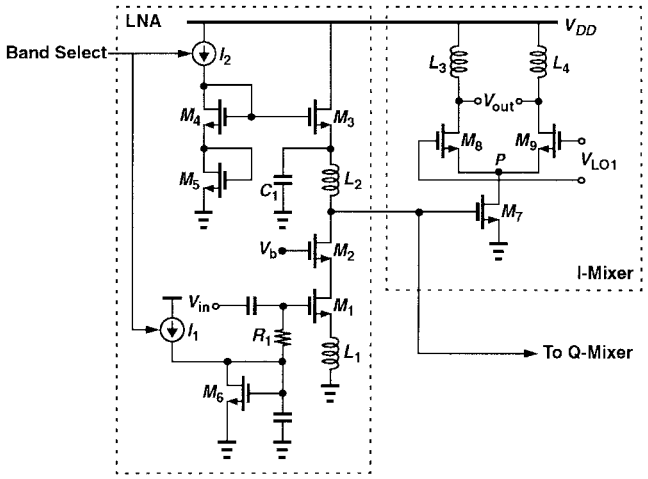


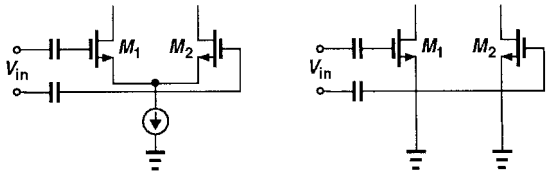

Fig. 10. RF stage.

$Q$ of $L_2$. Realized as an NMOS transistor, $C_1$ consists of a large number of gate fingers to reduce the channel resistance, achieving a $Q$ of greater than 30 at the frequency of interest.

In contrast to ac coupling techniques, the above approach incurs no signal loss, but it consumes some voltage headroom. Interestingly, $M_3$ can serve as the current source for another circuit, e.g., an oscillator, thus reusing the bias current of the LNA.

## C. IF Mixer

The differential output of the RF mixers in Fig. 10 is capacitively coupled to the input port of the IF mixers, allowing independent biasing. With an overall voltage gain of about 26 dB in the LNA and the RF mixers, the nonlinearity of the IF mixers tends to limit the performance of the receiver. To this end, we note that a differential pair with a constant tail current [Fig. 11(a)] exhibits higher third-order nonlinearity




(a) (b)

Fig. 11. Differential pairs with (a) constant tail current and (b) grounded sources.

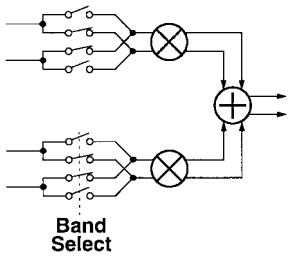



Fig. 12. Band switching in IF mixers.

than a grounded-source pair biased at the same current and device dimensions [Fig. 11(b)] [12]. For example, for square-law devices

$$I_{D1}I_{D2} = (1/2)\mu_n C_{\rm ox}(W/L)(V_{\rm in}) \cdot \sqrt{\{2I_{SS}/[(1/2)\mu_n C_{\rm ox}(W/L)]\} - (V_{\rm in})^2}$$

in Fig. 11(a), whereas

$$\begin{aligned} I_{D1} - I_{D2} &= (1/2)\mu_n C_{\rm ox}(W/L) \cdot [(V_{\rm GS1} - V_{\rm TH})^2 - (V_{\rm GS2} - V_{\rm TH})^2] \\ &= (1/2)\mu_n C_{\rm ox}(W/L)(V_{\rm GS1} - V_{\rm GS2}) \cdot (V_{\rm GS1} + V_{\rm GS2} - 2V_{\rm TH}) \end{aligned}$$

in Fig. 11(b). That is, the grounded-source pair output contains *no* third-order intermodulation products. In practice, short-channel effects such as nonlinear channel-length modulation and mobility degradation with the vertical field in the channel give rise to third-order distortion, but this calculation points to the potentially higher linearity of the grounded-source pair. The tradeoff is somewhat greater sensitivity to supply noise, as expressed by $V_{\rm GS1} + V_{\rm GS2} - 2V_{\rm TH}$ in the above equation.

We should also note that the addition/subtraction function in Fig. 6 must be incorporated in the IF mixer. To avoid voltage headroom limitations at the output of the mixer, this function is implemented by switching the polarity of one of the differential signals generated by the RF mixers (Fig. 12). The switching network is inserted in both signal paths to equalize the delays, but only one of the paths is controlled by the band-select input and the other is hard-wired.

Shown in Fig. 13, the IF mixer is configured as a double-balanced circuit consisting of an input pair $M_1$–$M_2$, a current multiplexer $S_1$–$S_4$, and a switching quad $M_3$–$M_6$. Drawing a drain current of 1 mA, $M_1$ and $M_2$ are sized to sustain an overdrive voltage of 500 mV, thereby achieving an $IP_3$ of approximately 1.77 $V_{\rm rms}$ (equivalent to +18 dBm in a 50-$\Omega$ interface). The low transconductance of $M_1$ and $M_2$ together with voltage headroom limitations ultimately results in a slight voltage conversion loss (about −2 dB) in the IF mixer.

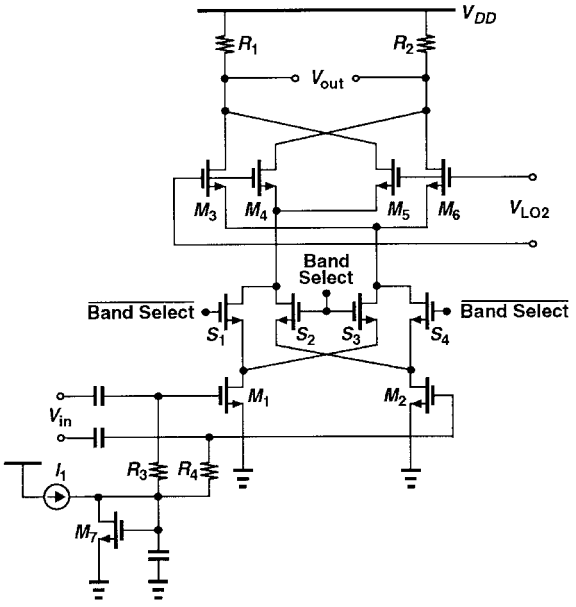
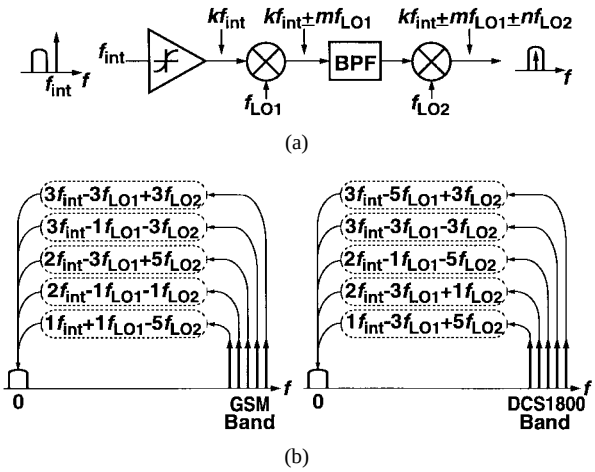



Fig. 13. IF mixer.




(a)

(b)

Fig. 14. Spurious components downconverted to baseband. (a) Effect of in-band interference and (b) most significant spur combinations.

The current multiplexer performs the switching function illustrated in Fig. 12. The switches negate the signal current according to the logical state of band select while sustaining a drain-source voltage of approximately 35 mV.

## VI. Spurious Response

An important concern in heterodyne and image-reject receivers is the translation of various interferers to the desired channel frequency after downconversion. Owing to nonlinearities and switching operations in each mixer, an interferer at $f_{\rm int}$ results in components at $kf_{\rm int} + mf_{\rm LO}$. With two downconversions using $f_{\rm LO1}$ and $f_{\rm LO2}$, the downconverted spurs appear at $kf_{\rm int} \pm mf_{\rm LO1} \pm nf_{\rm LO2}$, many of which may fall in the desired baseband channel [Fig. 14(a)]. Since in-band interferers are not filtered before channel selection and since they are located on the same side of $f_{\rm LO1}$ as the desired signal, they are not suppressed by the image-rejection technique used in the receiver.

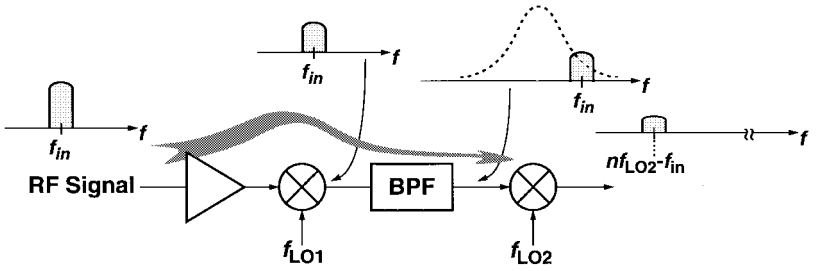



Fig. 15. RF signal feedthrough to IF port.

It is also important to note that the spurious response is not exercised in a simple noise-figure measurement, but it reveals the performance of the receiver in a realistic environment.

The spurious response of the dual-band receiver has been examined with the aid of a spreadsheet program. Five interference frequencies in each band were found to be the most significant sources of downconverted spurs. Fig. 14(b) illustrates the mixing mechanisms that generate in-channel components. Section VII presents the measured spurious response for the fabricated prototype.

Random mismatches in the RF mixers together with the finite bandwidth of the IF bandpass filter yield another type of spur that results from mixing of the RF input and harmonics of the *second* LO. As illustrated in Fig. 15, random asymmetry in the RF mixer allows a fraction of the RF signal to appear at the IF port without frequency translation [4]. Since the bandpass filter (BPF) suffers from a low $Q$, this component is attenuated by a small amount and subsequently multiplied by the second LO signal and its harmonics. In the present design, only the component given by $f_{\rm in}-2f_{\rm LO2}$ becomes noticeable in the GSM mode. Note that the second harmonic of $f_{\rm LO2}$ is nonzero because of mismatches in the LO and the mixer.

In addition to input-dependent spurious response, some other tones are observed that result from mixing of the LO signals themselves. The most significant of these is given by $f_{\rm LO1}-3f_{\rm LO2}$.

Another effect that arises in the DCS1800 mode of the receiver is signal corruption by the image *before* the first downconversion. As illustrated in Fig. 16, if a strong image component at 900 MHz accompanies the desired signal, second-order distortion in the LNA creates the second harmonic of the image, thereby degrading the signal-to-noise ratio (SNR) in the DCS1800 band. Nevertheless, since the duplexer suppresses the image considerably, the corruption is negligible. Simulations indicate that if a $-98$-dBm DCS1800 signal and a $-30$-dBm 900-MHz image are applied to the receiver, the output of the LNA exhibits an SNR of 50 dB provided the duplexer attenuates the image by 40 dB. With a fully differential LNA/mixer design, this effect would be even less critical.

Another interesting phenomenon that results from the choice of the two LO frequencies is the in-band leakage to the antenna. As shown in Fig. 17, the $\rm LO_1-IF_1$ feedthrough and the low $Q$ of the BPF give rise to a significant 1350-MHz component at the input of the IF mixer. Upon second mixing, this component is translated to both 900 and 1800 MHz, potentially appearing as in-band leakage to the antenna(s).

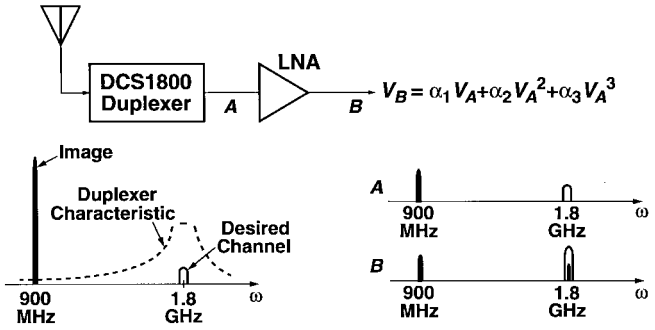



Fig. 16. Problem of second-order distortion in the DCS1800 band.

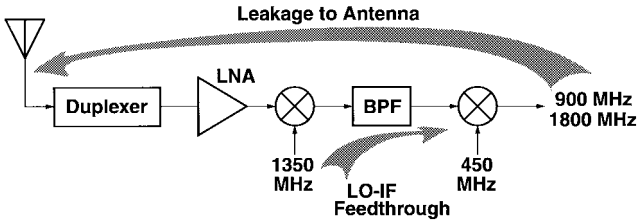



Fig. 17. In-band leakage to antenna.

However, by virtue of differential signaling from the first IF onward, and by proper low-pass filtering at the output, this type of leakage can be suppressed to acceptably low values.

## VII. Experimental Results

An experimental prototype of the dual-band receiver has been fabricated in a digital 0.6-$\mu$m CMOS technology. Fig. 18 shows a photograph of the die, which measures $1.54 \times 1.37$ mm$^2$. A number of precautions have been taken in the layout of the circuit. First, two pads are dedicated to the ground connection of $L_1$ in Fig. 10 so as to minimize the effect of bondwire inductance. Second, the RF input pad of each LNA is shielded from the resistive loss in the substrate by a grounded polysilicon square [12]. Third, the gate resistance of the LNA and mixer transistors is reduced to acceptably low levels by proper layout.

For inductor values greater than 10 nH, stacked structures have been used [11]. In particular, inductors $L_3$ and $L_4$ in the RF mixer of Fig. 10—each approximately equal to 100 nH—incorporate three metal layers (Fig. 19) to reduce the required area by a factor of about eight with respect to a single layer [11]. The polysilicon connection to the center of the metal-1 spiral must be wide enough to contribute negligible

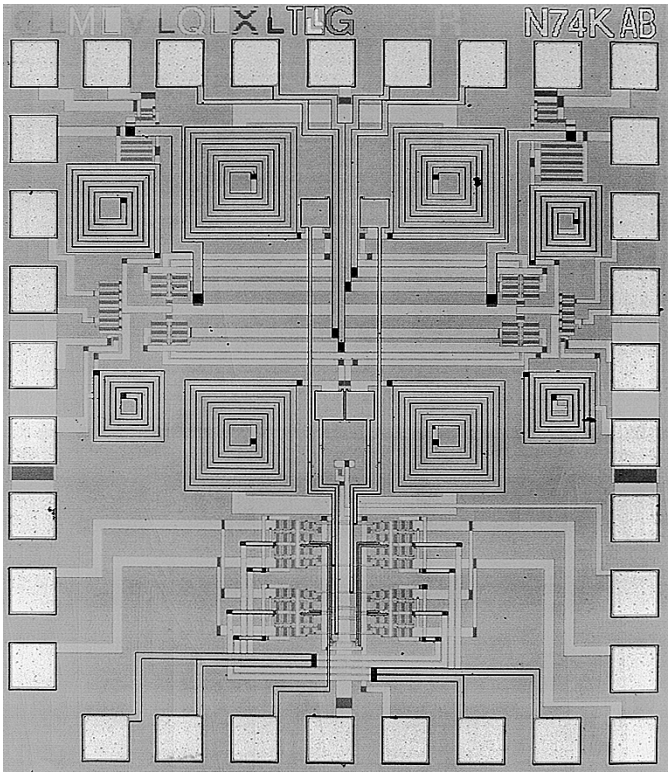


Fig. 18. Die photograph of dual-band receiver.

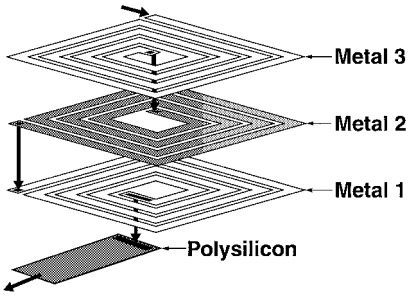



Fig. 19. Implementation of three-layer inductor.

resistance, but tying this side of the inductor to $V_{DD}$ lowers the effect of capacitance to the substrate.

The chip has been directly mounted on a printed-circuit board such that a ground plane lies under the die, providing a low-impedance connection to the backside and all of the ground pads. Various supply and bias decoupling techniques reduce the effect of both trace inductances and external sources of noise. The quadrature LO signals are generated by means of external transformers.

Plotted in Fig. 20 are the measured values of the intermodulation products in a two-tone test. The $IIP_3$ is equal to $-8$ dBm for the 900-MHz path and $-6$ dBm for the 1.8-GHz path. The corresponding noise figures are 4.5 and 4.9 dB, respectively. The image-rejection ratios are equal to 40 dB for 900 MHz and 36 dB for 1.8 GHz. Table II summarizes the measured performance of each receive path. Also shown are the quantities when front-end duplexers with an in-band loss of 3 dB and far-out rejection of 41 dB are used.

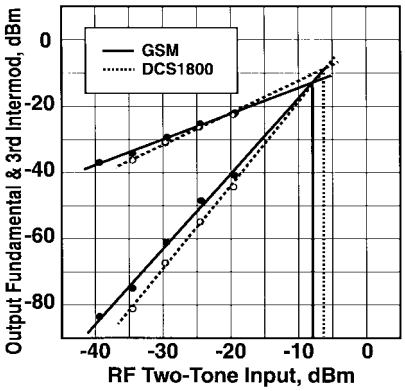



Fig. 20. Measured third-order intercept point.

TABLE II
EXPERIMENTAL RESULTS FOR DUAL-BAND RECEIVER

| | 900 MHz | | 1800 MHz | |
|---|---|---|---|---|
| | Rx alone | Rx w/ Duplexer | Rx alone | Rx w/ Duplexer |
| Noise Figure | 4.7 dB | 7.7 dB | 4.9 dB | 7.9 dB |
| $IIP_3$ | -8 dBm | -5 dBm | -6 dBm | -3 dBm |
| Image Rejection | 40 dB | 78 dB | 36 dB | 74 dB |
| Input Return Loss | -11 dB | N/A | -12 dB | N/A |
| Power Dissipation | 72 mW | 72 mW | 75 mW | 75 mW |
| Voltage Gain | 23 dB | 20 dB | 23 dB | 20 dB |
| Supply Voltage | 3 V | | | |
| Technology | 0.6-μm CMOS | | | |

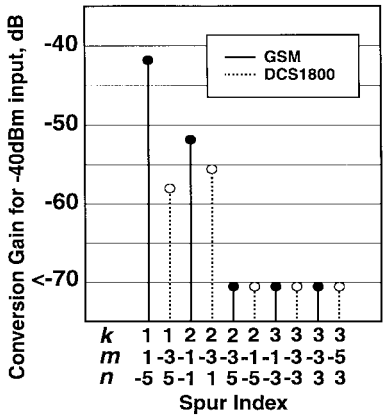



Fig. 21. Conversion gain of various spurs in each band.

The spurious response of the two receive paths has also been studied. Fig. 21 plots the conversion gain of a $-40$-dBm interferer after it undergoes the spur mechanisms illustrated in Fig. 14. We note that the interferer experiences a loss of at least $42 + 23 = 65$ dB with respect to the desired signal. Also, the most significant component, namely, that at $f_{\rm int} + f_{\rm LO1} - 5f_{\rm LO2}$, can be suppressed considerably by adding a parallel first-order LC notch filter at the IF with a resonance frequency of $f_{\rm int} + f_{\rm LO1} = 2.25$ GHz.

For an input level of $-30$ dBm, the spur at $f_{\rm in} - 2f_{\rm LO2}$ is equal to $-57$ dBm in the GSM mode. The discrete tone resulting from $f_{\rm LO1} - 3f_{\rm LO2}$ has a magnitude of $-40$ dBm,

and the in-band leakage illustrated in Fig. 17 is less than $-80$ dBm. In these tests, the first and second LO levels are $+8$ dBm.

We should also note that, while the receiver has been characterized by various measurements here, in practice, the GSM and DCS1800 standards require many more type-approval tests. Also, it is important that the *transmit* path use the same LO frequencies to minimize the number of oscillators and frequency synthesizers. A companion dual-band transmitter is described in [13].

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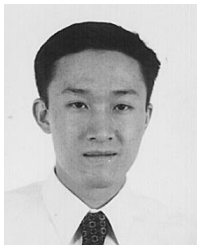

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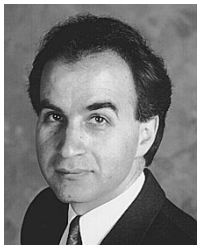

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Prof. Razavi is a member of the Technical Program Committees of the Symposium on VLSI Circuits and the International Solid-State Circuits Conference, of which he is the Chair of the Analog Subcommittee. He has also been a Guest Editor and Associate Editor of the IEEE JOURNAL OF SOLID-STATE CIRCUITS and *International Journal of High Speed Electronics*. He received the Beatrice Winner Award for Editorial Excellence at the 1994 ISSCC, the Best Paper Award at the 1994 European Solid-State Circuits Conference, the Best Panel Award at the 1995 and 1997 ISSCC, and the TRW Innovative Teaching Award in 1997.